

# HARMONIC CONTENT OF DIGITAL CMOS SWITCHING WAVEFORMS

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## ABSTRACT

We outline the influence of transistor model quality on estimates of harmonic content of switching waveforms. Accurate estimates are important in the design of highly-integrated wireless communication systems. Harmonic content can be included in the design of tapered buffer chains, but discontinuous device models can influence the design quality significantly.

## I. BACKGROUND

The increased level of integration places new requirements on the accuracy and efficiency of estimates of the coupling of digital switching noise into analog signals. Moreover, with on-chip radio circuitry, the estimation tools must be accurate also at high frequencies. The recently-presented Bluetooth system [2] provides an example: the radio works in an unlicensed band at 2.45 GHz, whereas the digital clocks may be between 10 MHz and 20 MHz. Designers of a future single-chip implementation of a Bluetooth transceiver might therefore require accurate estimates of the levels of harmonics 120 to 240 of the clock signal.

The coupling of switching noise in integrated circuits is a complex problem. It is beneficial to divide it into three parts: *generation* of the switching noise in an "aggressor" circuit, *coupling* of the noise from the aggressor circuit to the "victim" circuit, and *pickup* of the noise by the victim circuit. Pickup of switching noise can be addressed through conservative radio circuit design; an example would be the use of dual-rail, balanced signal paths. As another example, DC offsets caused by leakage of switching noise into a receiver chain may be compensated for if constant, or at least predictable. The coupling problem has been the topic of much recent work. A key issue is to derive macro-models which, although of much lower order than a detailed model, capture the essential coupling behavior from aggressor to victim [11]. However, such techniques are outside the scope of this paper.

In practical systems, the total switching noise received at any victim circuit would be a combination of noise from a very large number of aggressor circuits. Circuit reduction is therefore important also for noise generation: accurate simulation of large digital circuits would require enormous computer resources. It is finally also necessary to understand the harmonic content of the switching wave-

forms generated by the digital circuits, and how this spectrum is influenced by circuit design parameters. The work described in this paper focuses on this latter problem.

In Section II, we investigate the influence of transistor model quality on the estimates of the harmonic content of switching waveforms. Section III outlines how high harmonics are generated in an inverter. Section IV describe some results of tapered-buffer design with an industrial-grade device model. Our conclusions are in Section V.

## II. TRANSISTOR MODEL QUALITY

An initial set of experiments aimed at exploring the influence of transistor device parameters on the spectrum of a switching waveform. The experiments were very simple, though still quite informative: we computed the supply current and the output voltage waveform of a switching CMOS inverter with a linear capacitive load. The input voltage transition was set to exponentially approach the supply voltage with a tunable time constant [3].

The experiments were carried out in Matlab [7], a rich environment with a multitude of numerical tools which allow rapid exploration of algorithms and methods. Complete control over device models and parameters requires no extra effort in a script-based, interpreted system. Thus, the overall flexibility allows a straightforward experimental apparatus with few controls which have self-evident physical interpretations. A side benefit is that explicit output waveforms can be found for some simple transistor models [3] (explicit solutions for more complex and accurate models, in particular those which represent short-channel behavior, have eluded us). The solutions of the circuit equations provide transition edges which are then used to construct a pulse waveform. The spectrum of the pulse is evaluated with an FFT.

The output signal is a square wave with slower, rounded edges. Spectra of such signals follow that of an unadulterated square wave up to a "knee" frequency, which depends on the rise time of the edge. Beyond the knee frequency, the harmonic content falls off successively and eventually approaches an asymptote. As our main interest is with the harmonic content at high frequencies, at around the 100th harmonic and above, the asymptotic behavior is quite significant for the absolute level of the harmonic content in the frequency band of interest.

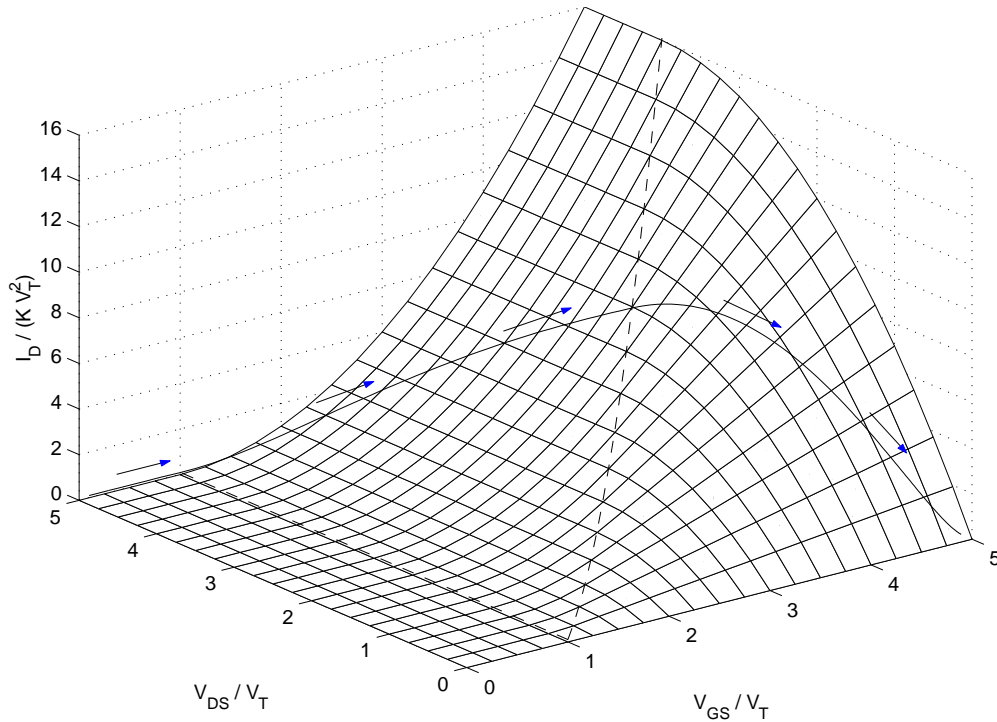


Figure 1. Current as function of terminal voltages for an n-channel device, as modelled according to Shichman and Hodges. A trajectory of a device which discharges a capacitive load has been superimposed on the diagram. The trajectory passes through both the major discontinuities (marked with dashed lines).

The accuracy of the numerical models of the MOS devices have proven to be decisive for the asymptotic behavior. Most MOS models suffer from discontinuities in some derivative of the drain current as function of the terminal voltages. It is important to realize that these discontinuities are artifacts of the model and do not appear in the physical device. We will exemplify the problem with a simplified version of the Shichman-Hodges model [10]:

$$\frac{I_D}{K} = \begin{cases} 0, & V_{GS} < V_T \\ (V_{GS} - V_T)^2 - (V_{GD} - V_T)^2, & V_{GS} > V_T, V_{GD} > V_T \\ (V_{GS} - V_T)^2, & V_{GS} > V_T, V_{GD} < V_T \end{cases}$$

The model is illustrated in Figure 1. The two discontinuities are readily apparent:  $\partial^2 I_D / \partial V_{GS}^2$  is discontinuous at  $V_{GS} = V_T$ , and  $\partial^2 I_D / \partial V_{DS}^2$  is discontinuous at  $V_{GD} = V_T$ . The inverter devices will pass through both these discontinuities during a full-scale transition of the input and output signals; an example trajectory is marked in Figure 1. As a result, the time derivatives of the drain current will exhibit associated discontinuities. Therefore, the asymptotic rolloff rate of an inverter current spectrum based on this model *cannot* be steeper than 60 dB/decade<sup>1</sup>. The load voltage waveform is essentially the integral of the supply current waveform, and so its spectrum

rolls off by an additional 20 dB/decade, yielding 80 dB/decade for the S-H model. A representative collection of output voltage spectra generated with the S-H model is shown in Figure 2.

The spectral drawbacks of the S-H model are accompanied by other shortcomings. The most obvious one is the dependence on the square of the gate-source voltage. This dependence represents an idealized long-channel behavior which is never approached by minimum-length devices in submicron processes [9]. A model suitable for our purposes should reproduce the short-channel characteristics of modern processes and also be continuous throughout its regions of operation, yet be simple enough to allow well-controlled experiments. The latter condition ruled out the models of the popular BSIM family as well as several others. An extensive search ended at the Maher-Mead model [6][8]. This physically-based model is not well known outside the transistor-modelling community. It is an implicit model where the charge densities at the drain and source ends of the channel are iterated for. The same set of equations are used from subthreshold to

1. The general rule is well stated by Lee [4]: “the spectrum of a signal will decay as  $1/f^n$ , where  $n$  is the number of derivatives of the signal required to yield an impulse.”

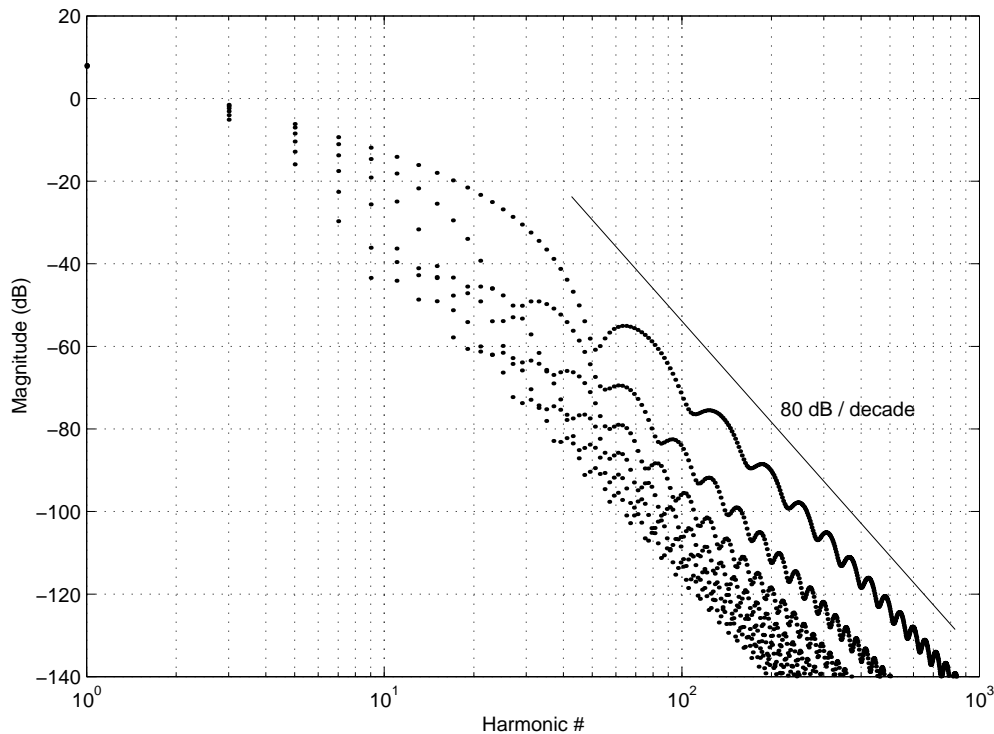


Figure 2. Spectra of output voltage waveforms of a capacitively loaded inverter, where the inverter devices have been modelled with the Shichman-Hodges model. The spectra differ only in the capacitive load driven. The output voltage waveforms were computed according to explicit formulae [3].

strong inversion and throughout the triode and pentode regions, with no splicing, smoothing, or fitting functions.

We implemented the DC behavior of the model<sup>2</sup> as far as described by Mead [8], and then used the Matlab ODE solvers to simulate one switching cycle of a symmetric inverter driving a linear capacitive load. Some spectra (obtained with FFTs, as before) of output voltage waveforms are shown in Figure 3. Clearly, the Maher-Mead model has allowed us to transcend the problems associated with non-physical discontinuities. Certain parameter combinations (of which more later) yield an asymptotic spectrum rolloff of up to 160 dB/decade.

### III. HARMONIC GENERATION IN INVERTERS

When device model discontinuities have been eliminated, the generation of high harmonics in actual circuits may be re-examined with a higher degree of confidence. Even in the absence of actual device model discontinuities, the

high-frequency content of the drain current waveforms will be generated by the strongest nonlinearities of the device. At and below the device threshold, the drain current depends exponentially on the gate voltage, providing large magnitudes of high-order time derivatives even for smooth gate-voltage waveforms.

The input voltage waveform in the vicinity of the device threshold voltage may be approximated with a straight line; then, the drain current will approximate an exponential function of time, with a time constant inversely proportional to the edge rate of the input waveform at the threshold voltage. The magnitudes of the derivatives of an exponential function grow when the time constant shrinks. A faster input edge rate should therefore result in an increased amount of high-order harmonics. Simulations with the same setup as before confirm this qualitative argument. Figure 4 shows the results of a set of simulations where only the time constant of the input signal has been varied.

We have not been able to derive exact expressions for the spectra of Figure 4 (the Maher-Mead model is implicit, and closed expressions for the output waveforms cannot be found). Even when the output waveform is known exactly, such as for a Shichman-Hodges device with a lin-

2. The voltage-dependent intrinsic capacitances of the device were not implemented. The AC behavior was assumed to be dominated by the linear load capacitance on the output side; the input capacitance would not influence the waveform, as the input signal was given by an independent voltage source.

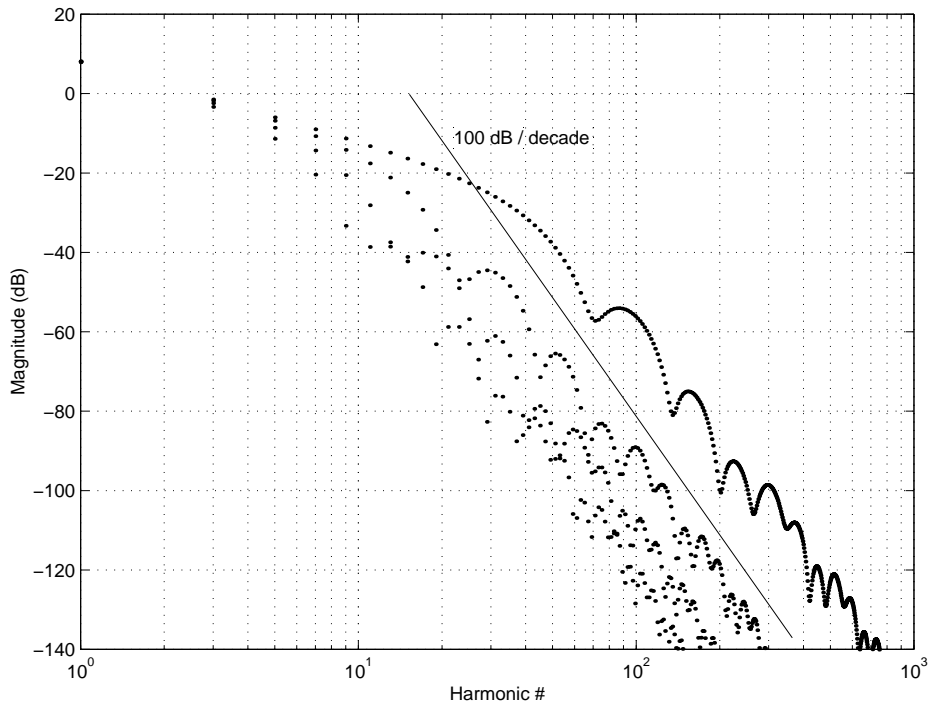


Figure 3. Example spectra of output voltage waveforms of a capacitively loaded inverter, where the inverter devices have been modelled with the Maher-Mead model. The spectra differ only in the capacitive load driven.

ear capacitive load driven by an exponential input waveform [3], closed-form expressions for the output spectrum are complex enough to bring little additional insight. Because of this, we have so far used simulation results such as those shown in Figure 4 to judge the influence of the input edge rate on the harmonic content of the output signal.

Any approximate expressions for the spectrum magnitudes would have to take several device parameters into account. The most important one seems to be the threshold voltage of the devices. A device with a low threshold voltage has a large subthreshold current and therefore turns on softly, yielding a steep spectrum rolloff (up to 160 dB per decade in our experiments).

It would appear that low threshold voltages would be beneficial for highly-integrated wireless communication devices, since the magnitudes of high-order harmonics are small. Very low threshold voltages, however, cause leakage currents and thereby idle power dissipation. Possibly, alternative logic styles could be found, where the dissipation cost for limiting high-frequency switching noise would be less pronounced than for static CMOS; however, we consider this possibility to be remote.

#### IV. TAPERED BUFFER DESIGN

The Matlab results described in the previous section immediately suggest a way to reduce the harmonic content of the output signal of a tapered buffer chain. Slower transitions of the input signal of the last stage in the chain will reduce the high-order harmonics in the last stage.

Output transition time is a common design constraint in design procedures for tapered buffer chains. Conventional design procedures for tapered buffer chains [1] assume the same ratio of load capacitance and input capacitance for all buffer stages. To first order, this assumption results in equal transition times for all stages. A requirement for a certain transition time of the last stage fixes the width of the devices of the last buffer and thereby the capacitive load for the next-to-last stage. The buffer chain excluding the last stage can then be sized using the unconstrained version of the design procedure. This idea may be trivially extended to allow control of the transition time for the next-to-last stage as well, such that all but the last *two* buffers are sized with the unconstrained procedure.

Each additional constraint may force deviations from the buffer dimensions which the unconstrained design procedure would find; changes in delay, power, or other cost functions may be expected. It is however important to realize that the cost function minima are rather shallow,

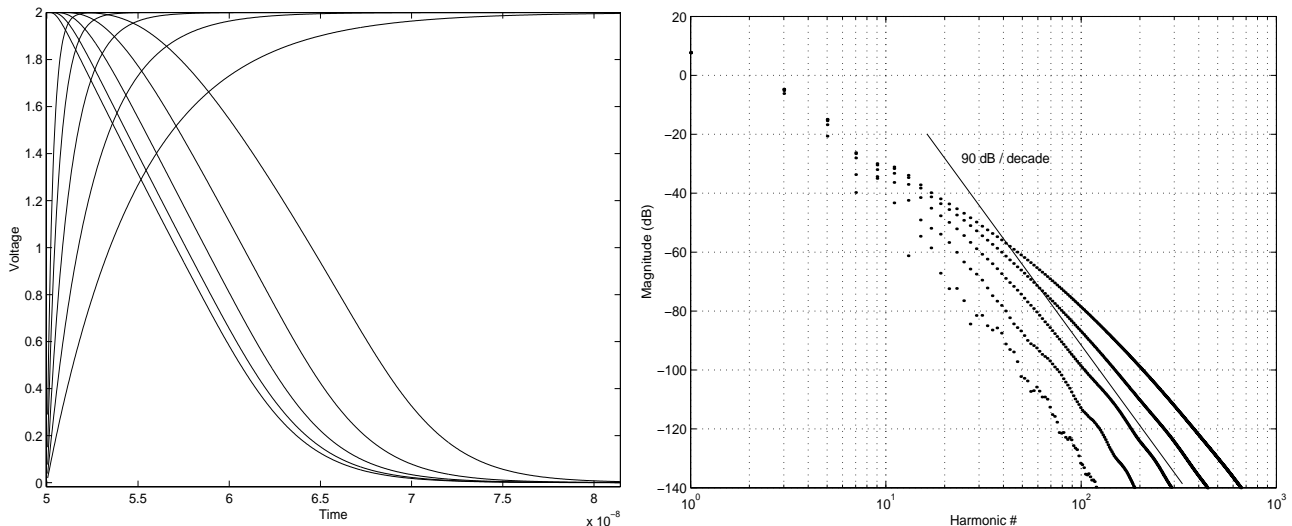


Figure 4. Input and output waveforms and spectra of a capacitively loaded inverter (Maher-Mead models) for varying input edge rates. Slower input edges mean a softer turn-on of the devices and thus lower levels of high-frequency harmonics.

so a significant improvement in the harmonic content might be reached with a small increase in stage delay (cf. Figure 4).

The target transition time for the two last stages should be selected based on the acceptable level of harmonics in some band of interest. The relation between transition times and harmonic content must presently be investigated by simulation. Matlab is not the best possible tool for this task. Special-purpose circuit simulation programs, such as the Cadence program Spectre [4], are much more numerically efficient at solving the stiff systems of non-linear differential equations common in circuit simulation. Additionally, performance data on the devices available in industrial semiconductor processes are most often provided as parameter sets for a device model provided with a certain simulator. For these reasons, we have used Spectre in an attempt to quantify the harmonic content of the output voltage waveform of a tapered buffer. We have used the BSIM3v3.1 model with a parameter set for a 0.25- $\mu$ m process from one of our ASIC suppliers. We used the ratiometric Fourier analyzer rather than FFT post-processing. Some results are shown in Figure 5.

The Spectre simulations are in qualitative agreement with the Matlab results: decreasing the edge rate at the input of the last stage in a buffer chain reduces the harmonic content of the output waveform. Quantitatively, however, we see significant discrepancies between the spectrum rolloff rates in the two cases. The Spectre-produced spectra roll off with at most 75 dB per decade, and the rolloff does not improve with lower edge rates. The discrepancies are

large enough to produce very different results when optimizing a buffer chain for low levels of high harmonics.

## V. CONCLUSION

Accurate estimates of the harmonic content of the switching waveforms of common digital circuits would allow designers and CAD tools to minimize the amount of switching noise produced, and possibly to distribute a given “switching noise budget” across several blocks. Such design procedures would help designers produce highly integrated systems with a minimum of switching-noise interference. Based on the findings described in this paper, we believe that transistor model quality is critically important for the accuracy of switching noise estimates.

Our Spectre simulations do not correlate well with the Matlab findings. The spectrum rolloff rates displayed by the Spectre simulations suggest problems with the model or, at least, with the parameter set. The BSIM3v3.1 model is complex: the model card lists approximately 100 parameters for each process corner. It is not inconceivable that a small discontinuity could be hiding inside the model, ruining the accuracy of the spectrum calculations.

We tend to have more faith in the qualitative aspects of our Matlab results than in those of the Spectre results<sup>3</sup>. This is since the parameters of the Maher-Mead model

3. There is one caveat: the non-linear device capacitances were not included in the Matlab runs. We believe their influence on the spectrum should be similar to that of the device threshold.

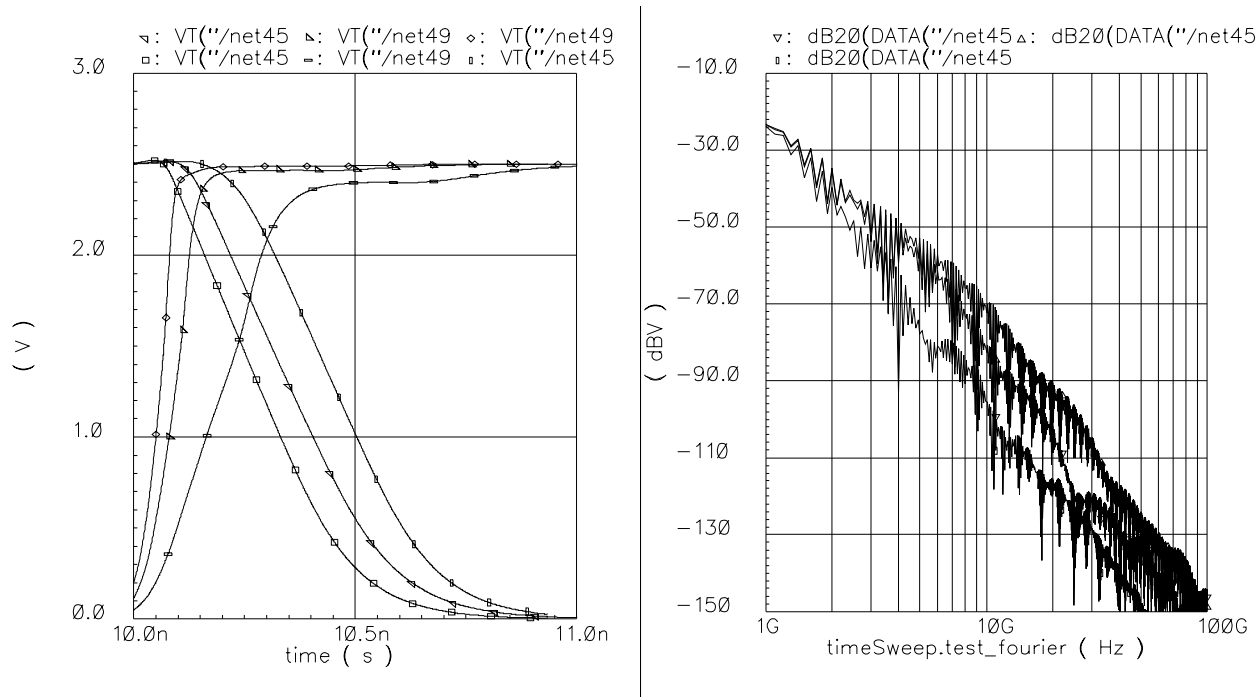


Figure 5. The figure shows input and output waveforms of the last buffer stage of a tapered buffer, and spectra of output voltage waveforms, for several values of the input edge rate. Simulations have been done in Cadence Spectre, using the BSIM3v3.1 device model with a parameter set for a 0.25- $\mu\text{m}$  process.

are few and mostly independent of each other. Furthermore, the parameters are grounded in device physics, and the model behaves according to expectation when a parameter value is changed. In contrast, it is hard even to understand what to expect when a single parameter is changed in the BSIM3v3.1 model.

Laboratory measurements will be necessary to determine which model represents the high-frequency switching harmonics more faithfully. We suggest that the correlation of simulated and measured spectra of a switching inverter would be a suitable design kit test for a process intended for mixed-signal use. Until such data are available, the prudent designer will be pessimistic and use the BSIM3v3.1 results. A buffer chain designed according to such guidelines may exhibit more delay than would be optimal, but the high harmonics are likely to be sufficiently suppressed.

## VI. References

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