

Harmonic Content of Digital CMOS Switching Waveforms

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Background

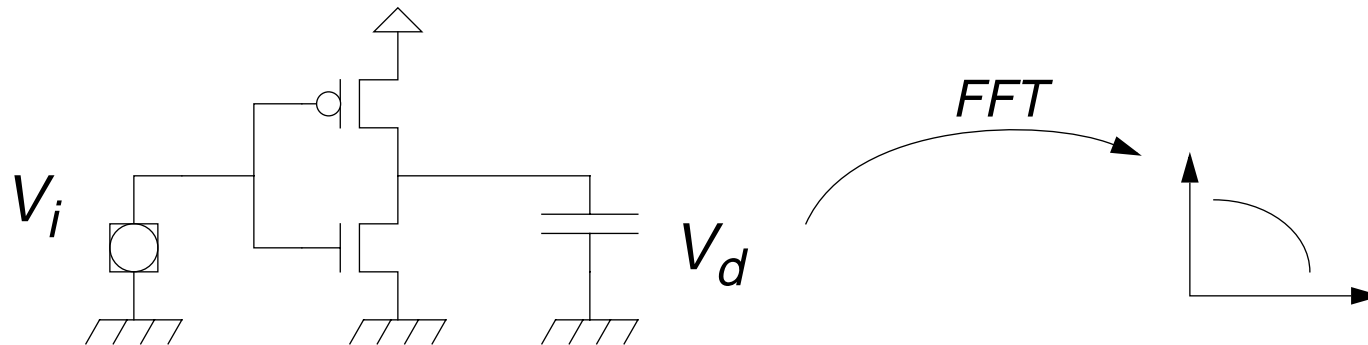
- ◆ *Near-future wireless digital communication devices will be highly integrated*
 - ◆ *Single-chip solutions possible soon*
- ◆ *Switching harmonics from digital parts influence radio performance*
- ◆ *Important to predict levels of high-order harmonics*
 - ◆ *Example: $f_{clock} \sim 10$ MHz, $f_{RF} \sim 1$ GHz; $n_{harm} \sim 100$*
- ◆ *Problem may be split in three parts: generation, coupling, pickup*
 - ◆ *Focus here is on noise generation*
 - ◆ *Q: What circuit parameters influence waveform spectra?*

Talk overview

- ◆ *Approach*
- ◆ *Influence of device model quality*
 - ◆ *Shichman-Hodges*
 - ◆ *Maher-Mead*
- ◆ *Harmonic generation in switching inverters*
- ◆ *Tapered-buffer design for low levels of high harmonics*
- ◆ *Experiences with vendor design kit*

Approach

- ◆ *Compute spectrum of output of switching inverter*



- ◆ *Simplest possible interesting circuit :-)*
- ◆ *Solve DE for some input signal, then do FFT*
 - $C (dV_d / dt) = I_d = f(V_i (t), V_d (t))$

- ◆ *Do experiments in Matlab*
 - ◆ *Canned routines for many tasks*
 - ◆ *Flexible*

Device model influence

- ◆ *Solution to*

$$-C (dV_d(t)/dt) = I_d = f(V_i(t), V_d(t))$$

is determined by $f(\bullet, \bullet)$

- ◆ *Simple example of $f(\bullet, \bullet)$: Shichman-Hodges*

- ◆ $I_d = 0, V_{GS} < V_T$

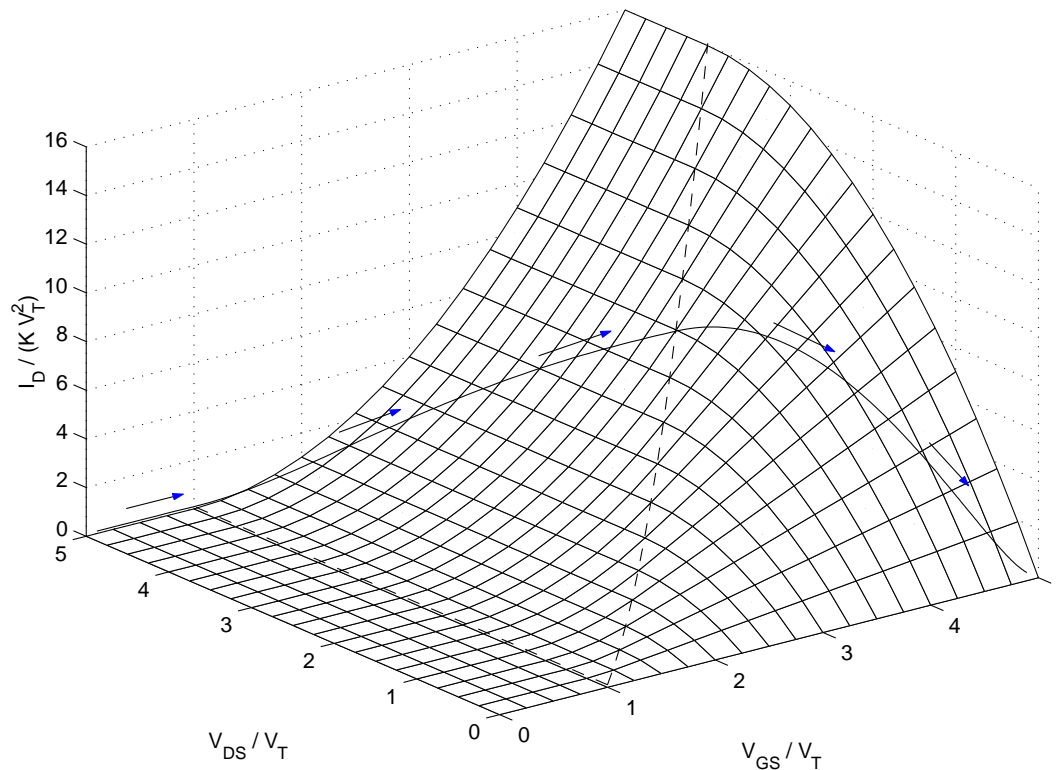
- ◆ $I_d = (V_{GS} - V_T)^2 - (V_{GD} - V_T)^2, V_{GS} > V_T, V_{GD} > V_T$

- ◆ $I_d = (V_{GS} - V_T)^2, V_{GS} > V_T, V_{GD} < V_T$

- ◆ *I_d and its first derivatives are continuous at “seams”, but second derivatives are not!*

Device model influence, cont.

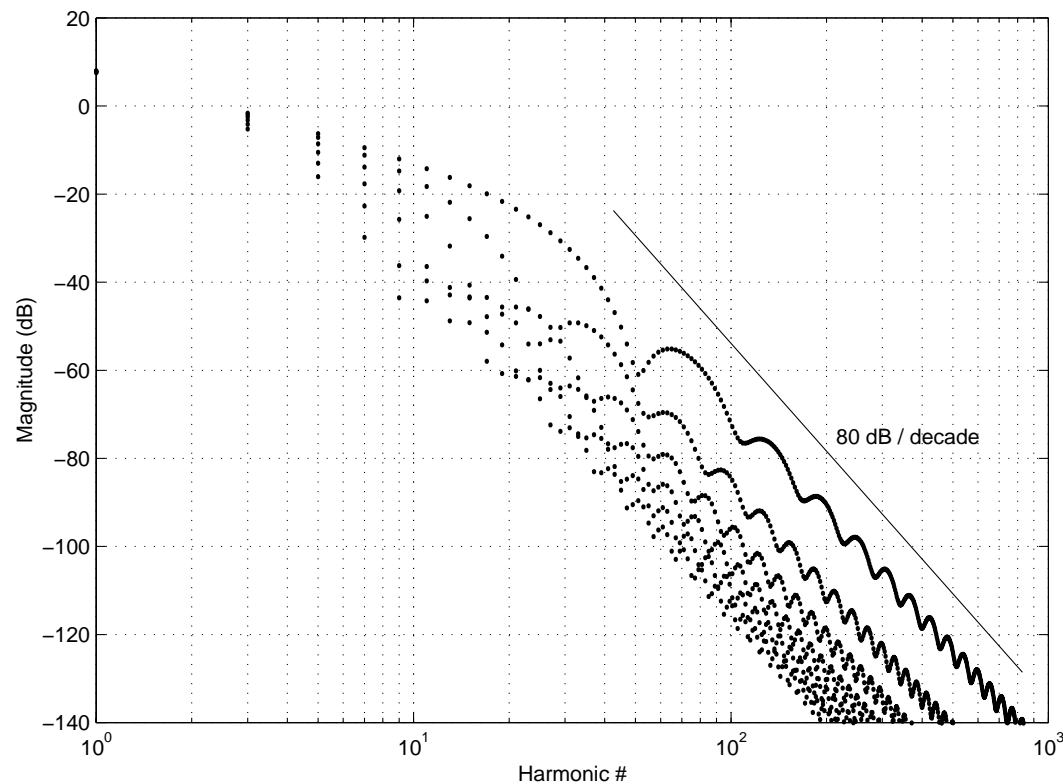
- ◆ *Devices cross both discontinuities during inverter transition*



- ◆ *Exact path depends on circuit and signal parameters*
- ◆ *Both discontinuities encountered in any transition*

Device model influence, cont.

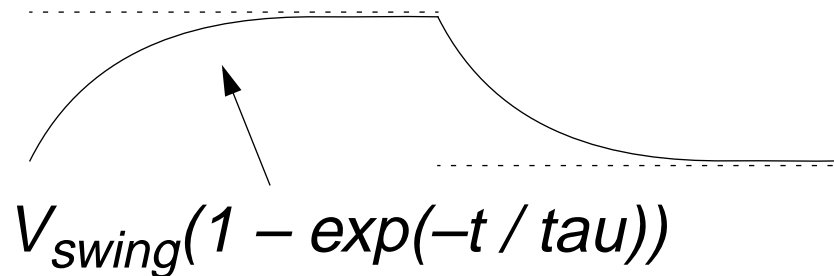
◆ Output voltage waveform spectra for S+H model



- ◆ *Asymptotic rolloff is 80 dB/decade, for all sets of parameter values*
- ◆ *Accuracy at high harmonics limited by model!*

Spectrum estimation prerequisites

- ◆ *Smooth input signals*
 - ◆ *We use exponential input signals*



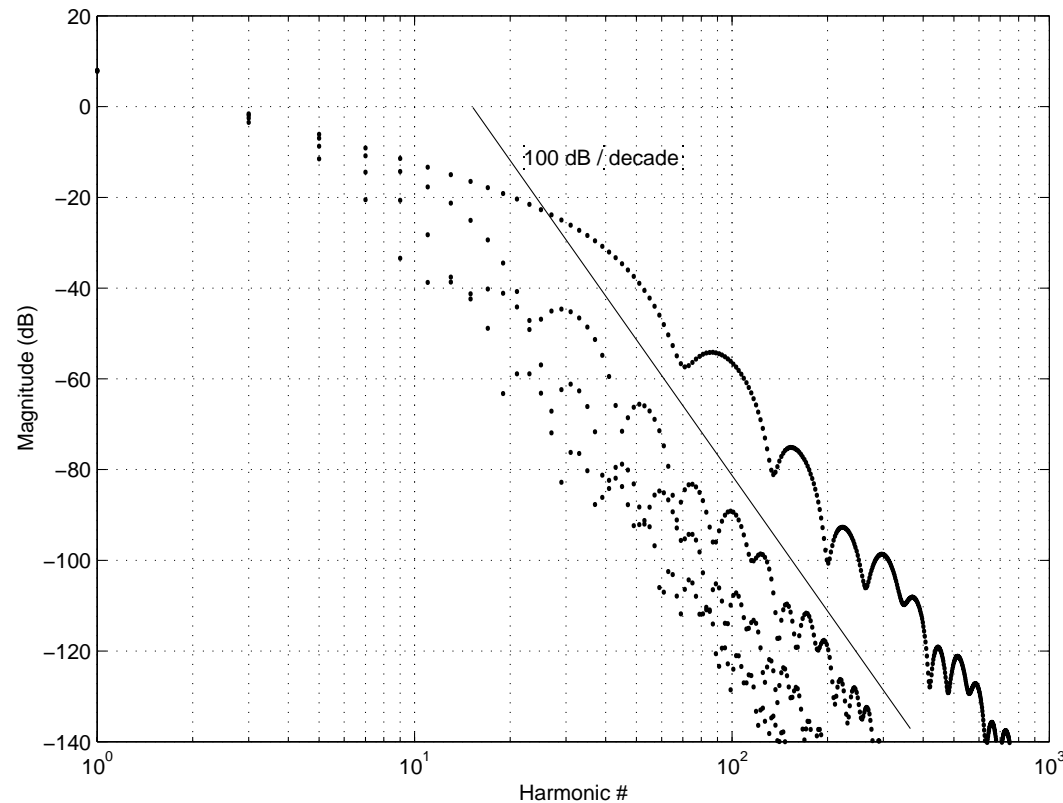
- ◆ *Many continuous derivatives*
 - ◆ *Mathematically simple, few parameters*
 - ◆ *Similar to actual digital circuit waveforms*
 - ◆ *Splice together to form pulse trains*
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- ◆ *Smooth device models*
 - ◆ *We use the Maher-Mead model*

Maher-Mead device model

- + *Continuous everywhere*
- + *Based on physical description*
- + *Few parameters, physical interpretations*
- *Implicit expressions (iterate for drain current)*
- *Not widely known outside device-modeling community*
- *Not widely supported in commercial tools*

◆ *Possible alternatives exist*

Maher-Mead spectra



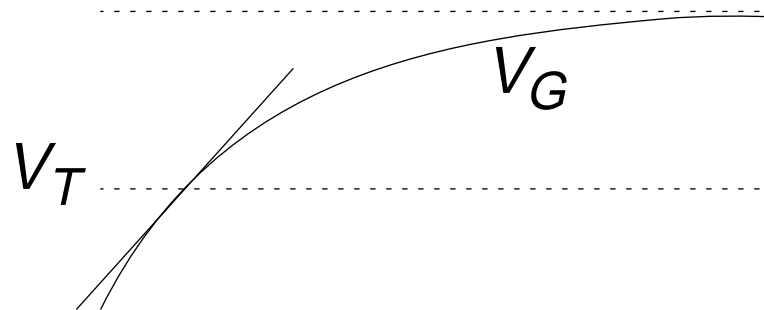
- ◆ *Results different from S-H spectra*
 - ◆ *Steeper asymptotic rolloff*
 - ◆ *Much steeper for some parameter combinations*

Harmonic generation

- ◆ Asymptotic rolloff rate with no discontinuities in models?
 - ◆ Set by “strongest” nonlinearity in $f(\bullet, \bullet)$
 - ◆ Just below device threshold:

$$f(V_G, V_D) \sim \exp(V_G), \quad V_G \approx V_T$$

- ◆ Gate voltage waveform is smooth around threshold



- ◆ In this neighborhood, approximate with straight line:

$$V_G \approx K \cdot t$$

Harmonic generation, cont.

- ◆ *Then, close to threshold, drain current is essentially exponential with time*

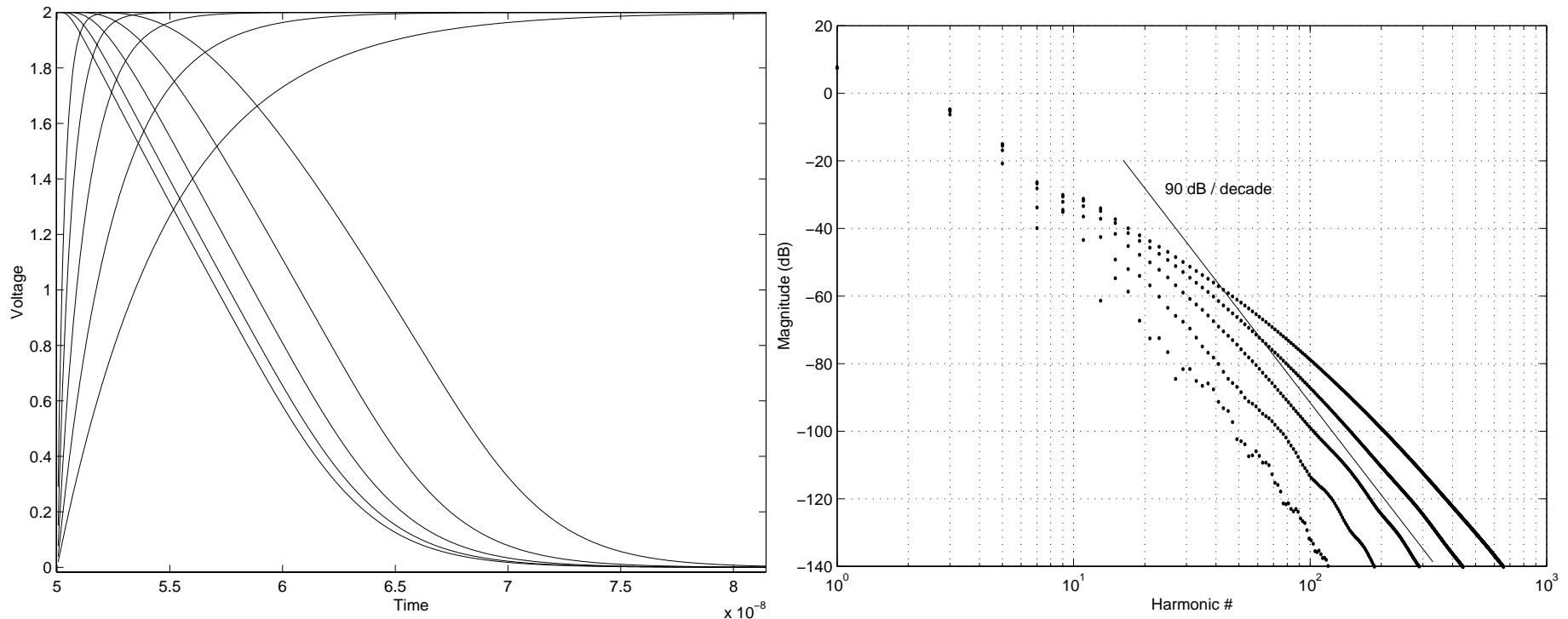
$$I_d(t) \sim \exp(K \cdot t), \quad V_G \sim V_T$$

- ◆ *High-order derivatives grow with K*

$$D^n [\exp(K \cdot t)] \sim K^n \exp(K \cdot t)$$

- ◆ *Steeper input edges (larger K) should produce more high harmonics!*

Influence of input edge rate

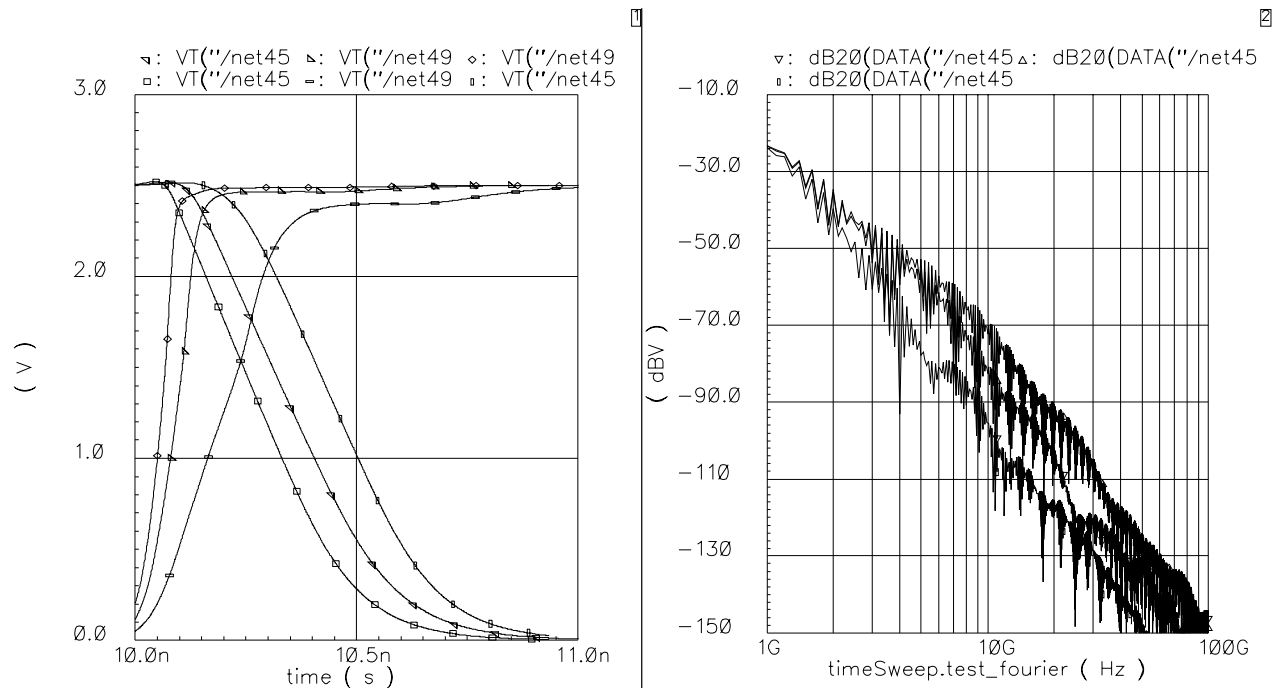


- ◆ *Input edge rate has strong influence on high harmonics*
 - ◆ *In this simulation, ~10 dB at 200th harmonic*
 - ◆ *Input edge rate affects delay too*
- ◆ *Caveat: noise improvement is circuit and device dependent*

How to size tapered buffers?

- ◆ *“Classic” method says to use constant scaling factor F*
 - ◆ *$F \approx e$ for lowest overall delay*
 - ◆ *F higher when power, area etc. significant*
- ◆ *Common extension to method is to fix output edge rate*
 - ◆ *Fixes width of last buffer stage, thus its input capacitance*
 - ◆ *$N - 1$ preceding stages now sized as usual*
- ◆ *Noise-aware method fixes edge rate on input of last stage*
 - ◆ *$N - 2$ stages sized as usual*
 - ◆ *Improves output voltage and supply current spectra*
- ◆ *Select edge rate to trade off delay vs. high harmonics*
 - ◆ *Look to silicon vendor’s Design Kit for process info*

Vendor design kit test



- ◆ *Example: BSIM3v3.1, 0.25u, Cadence Spectre*
- ◆ *Significantly different from Maher-Mead results*
 - ◆ *Slower rolloff*
 - ◆ *Input edge rates have less influence at high harmonics*

Conclusions

- ◆ *Device-model quality critical for switching noise estimates*
 - ◆ *Cruder models (PWL &c. used with faster simulators) would be even worse*
- ◆ *Vendor design kit indicates worse switching noise than Maher-Mead does*
 - ◆ *Who is more accurate?*
 - ◆ *Measurements needed*
- ◆ *Spectrum from inverter would make good design-kit test*
- ◆ *For low levels of high harmonics, size inverter chains such that transitions are no faster than necessary*
 - ◆ *Especially later stages (larger current)*