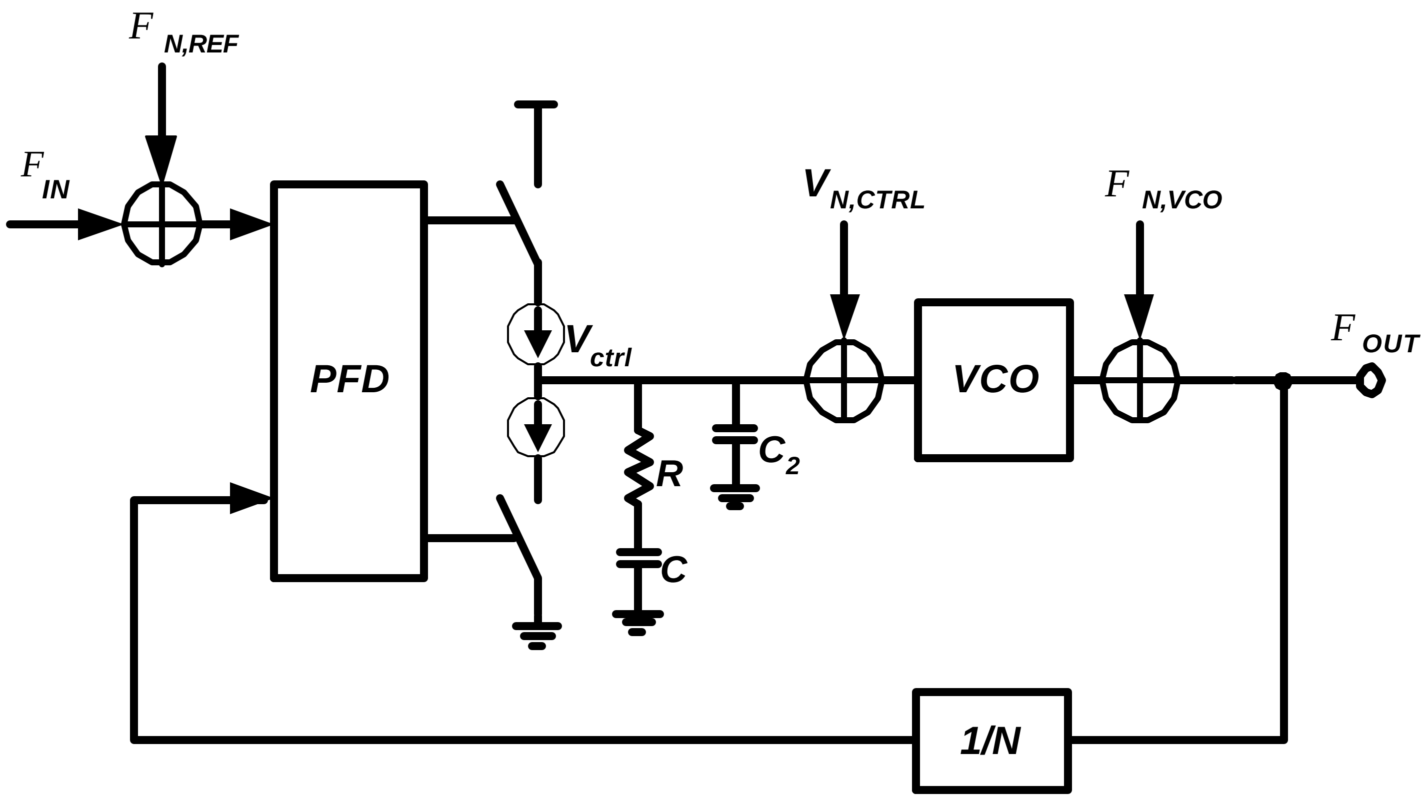
EE290C High-Speed Electrical Interfaces **Spring 2004.**

HOMEWORK 2. **Due: Thursday, March 11, 2004 at 5pm in 558 Cory**

This is an individual assignment!

Problem 1:



A third-order charge-pump PLL is shown in the above figure along with noise sources corresponding to the input reference clock, control node and VCO.
The VCO gain is K_{VCO} (Hz/V) and the charge-pump current is I_{CH} (A).

a) Find the noise transfer function from the various noise sources to the output of the PLL.

Solution:

For $F_{N,REF}$:

$$\Phi_{OUT} = \left(\Phi_{N,REF} - \frac{1}{N}\Phi_{OUT}\right) \times I_{CH} \times Z_{LF}(s) \times \frac{K_{VCO}}{s} \Rightarrow \frac{\Phi_{OUT}}{\Phi_{N,REF}} = \frac{I_{CH} \cdot Z_{LF}(s) \cdot K_{VCO}}{s + \frac{1}{N} \cdot I_{CH} \cdot Z_{LF}(s) \cdot K_{VCO}}$$

where $Z_{LF}(s) = \frac{sRC + 1}{s^2 RCC_2 + s(C + C_2)}$.

Letting $z = \frac{1}{2}\sqrt{\frac{1}{N} \cdot I_{CH} \cdot K_{VCO} \cdot R^2 \cdot \frac{C^2}{C+C_2}}$ and $w_N = \frac{2z}{RC} = \sqrt{\frac{I_{CH} \cdot K_{VCO}}{N \cdot (C+C_2)}}$ we can

write: $\frac{\Phi_{OUT}}{\Phi_{N,REF}} = N \cdot \frac{1 + s \cdot \frac{2z}{w_N}}{1 + s \cdot \frac{2z}{w_N} + s^2 \cdot \frac{1}{w_N^2} \cdot \left(1 + s\frac{RCC_2}{C+C_2}\right)}$. This is the same low-pass transfer function as in the case of the second-order PLL, except for the correcting factor in the denominator due to the third-order pole.

For $V_{N,CTRL}$:

$$\Phi_{OUT} = \left(V_{N,CTRL} - \Phi_{OUT} \times \frac{1}{N} \times I_{CH} \times Z_{LF}(s)\right) \times \frac{K_{VCO}}{s} \Rightarrow \frac{\Phi_{OUT}}{V_{N,CTRL}} = \frac{K_{VCO}}{s + \frac{1}{N} \cdot I_{CH} \cdot Z_{LF}(s) \cdot K_{VCO}}$$

This can be written: $\frac{\Phi_{OUT}}{V_{N,CTRL}} = \frac{K_{VCO} \cdot s \cdot \frac{1}{w_N^2}\left[1 + s\frac{RCC_2}{C+C_2}\right]}{1 + s \cdot \frac{2z}{w_N} + s^2 \cdot \frac{1}{w_N^2} \cdot \left[1 + s\frac{RCC_2}{C+C_2}\right]}$ which is a band-pass transfer function.

For the equivalent output noise of the VCO $F_{N,VCO}$:

$$\Phi_{OUT} = \Phi_{N,VCO} - \Phi_{OUT} \times \frac{1}{N} \times I_{CH} \times Z_{LF}(s) \times \frac{K_{VCO}}{s} \Rightarrow \frac{\Phi_{OUT}}{\Phi_{N,VCO}} = \frac{s}{s + \frac{1}{N} \cdot I_{CH} \cdot Z_{LF}(s) \cdot K_{VCO}}$$

This can be written: $\frac{\Phi_{OUT}}{\Phi_{N,VCO}} = \frac{s^2 \cdot \frac{1}{w_N^2} \cdot \left[1 + s\frac{RCC_2}{C+C_2}\right]}{1 + s \cdot \frac{2z}{w_N} + s^2 \cdot \frac{1}{w_N^2} \cdot \left[1 + s\frac{RCC_2}{C+C_2}\right]}$ which is high-pass.

b) Find the maximum achievable phase margin for this PLL and the unity-gain frequency for which it is achieved, assuming that the loop filter parameters R, C, C_2 are set.

Solution:

The loop transfer function of the PLL is:

$$T(s)=\frac{1+s\cdot\frac{2z}{w_N^2}}{s^2\cdot\frac{1}{w_N^2}\cdot\left[1+s\frac{RCC_2}{C+C_2}\right]}=(-1)\frac{\left(1+jw\cdot\frac{2z}{w_N^2}\right)\left(1-jw\frac{RCC_2}{C+C_2}\right)}{w^2\cdot\frac{1}{w_N^2}\cdot\left[1+w^2\cdot\left(\frac{RCC_2}{C+C_2}\right)^2\right]}.$$

The numerator can be written:

$$Num(w)=\left[1+w^2\frac{R^2C^2C_2}{C+C_2}\right]+j\cdot\left[wRC-\frac{wRCC_2}{C+C_2}\right].$$

The phase of the loop transfer function is:

$$\angle T(w)=-180^o+\arctan\left[\frac{wRC-\frac{wRCC_2}{C+C_2}}{1+w^2\frac{R^2C^2C_2}{C+C_2}}\right]=-180^o+\arctan\left[\frac{wRC^2}{C+C_2+w^2R^2C^2C_2}\right]\ (1).$$

Taking the derivative:

$$\frac{\partial\angle T(w)}{\partial w}=\frac{RC^2\left[C+C_2+w^2R^2C^2C_2\right]-wRC^2\cdot 2wR^2C^2C_2}{[\cdots]^2}=0$$

$$\Rightarrow RC^2(C+C_2)+w^2R^3C^4C_2=0$$

$$\Rightarrow w_0=\sqrt{1+\frac{C}{C_2}}\times\frac{1}{RC}$$

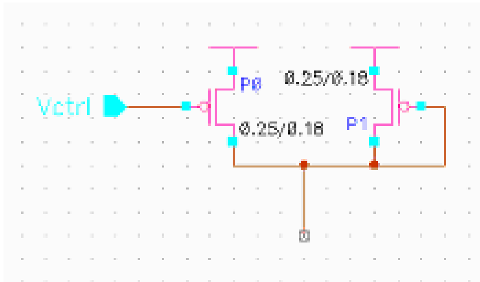
This is the frequency for which the phase is maximized, and therefore if we change the loop gain (determined by I_{CH} and K_{VCO}) to have ω_0 as the unity-gain frequency, then we obtain the maximum phase margin.
Substituting ω_0 in (1) we get the maximum phase margin:

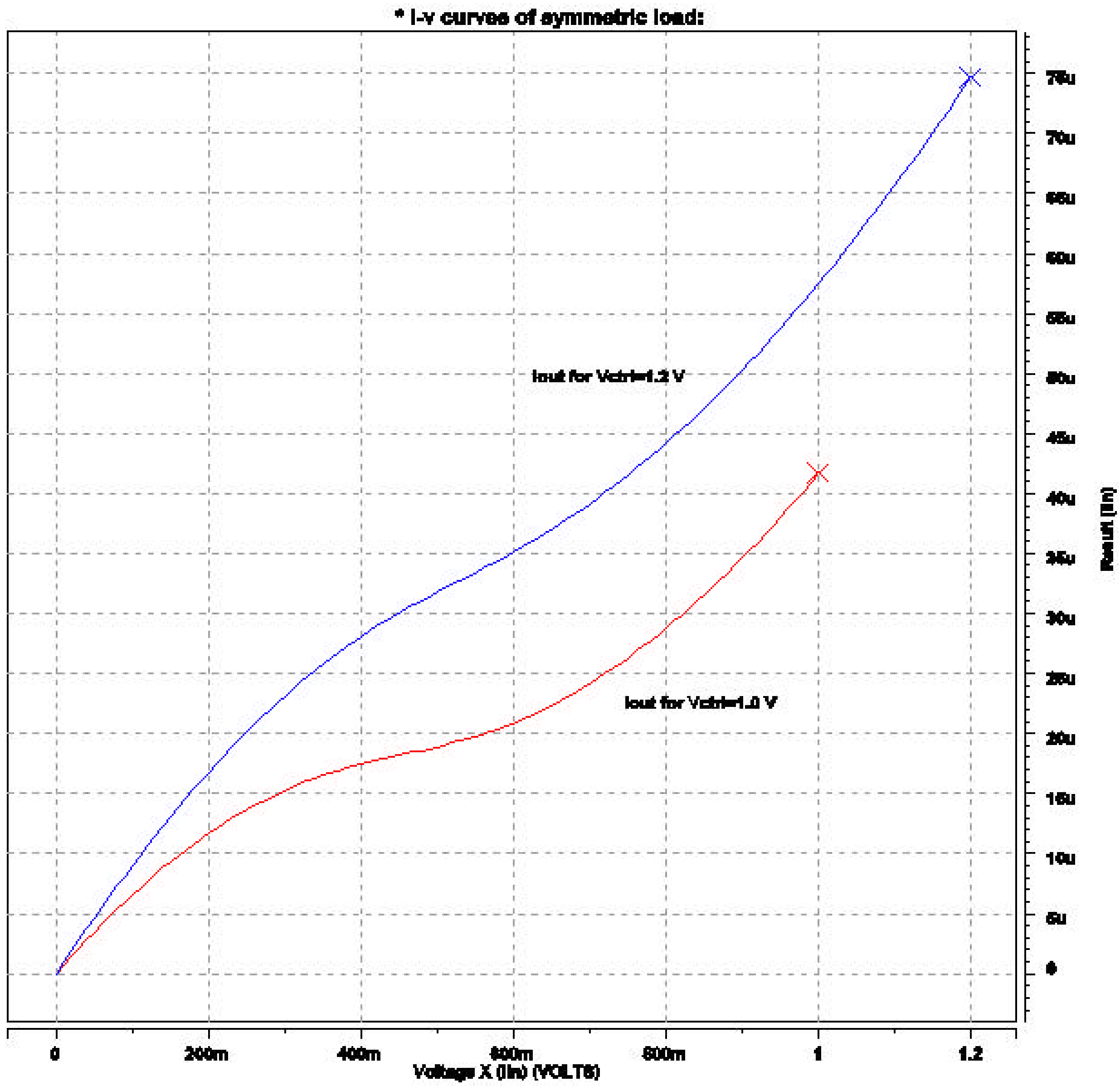
$$PM_{\max}=\arctan\left[\frac{w_0RC^2}{C+C_2+w_0^2R^2C^2C_2}\right].$$

Problem 2:
Read the paper:
J. Maneatis, "Low-Jitter Process-Independent DLL and PLL Based on Self-Biased Techniques", *IEEE J. Solid-State Circuits*, vol. 31, no. 11, pp. 1723-32, Nov. 1996.

a) Plot the I-V characteristics for V_{CTRL} values of 1V and 1.2V of the symmetric load in Fig. 5, using HSPICE. The definition of V_{CTRL} is as in Fig. 5. Let the PMOS devices be (0.25/0.18) μm. Use the 1.8V, 0.18 μm class technology.

Solution:
The curves are shown below:

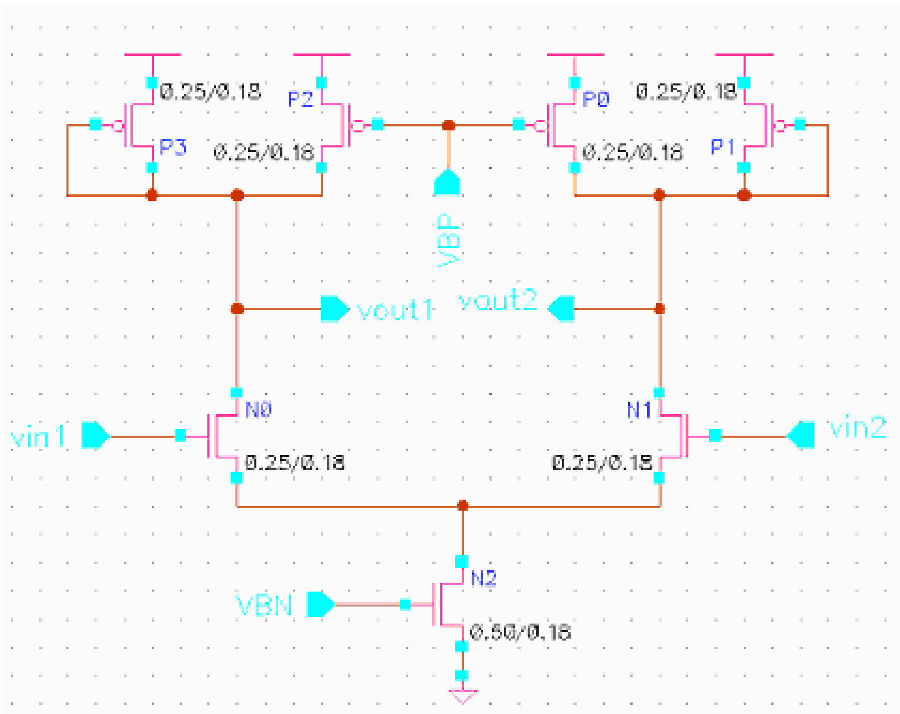




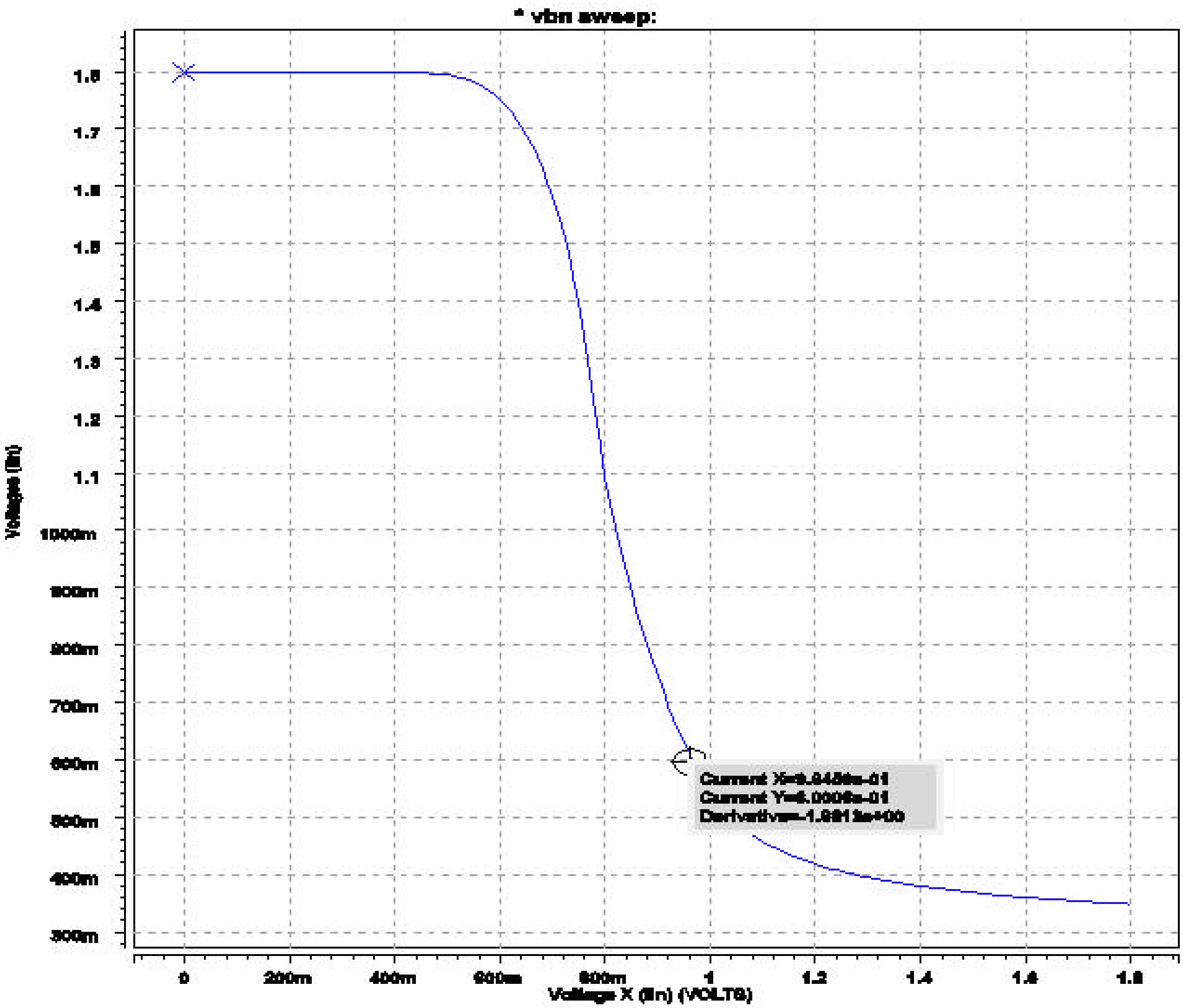
b) In the 1.8V, 0.18μm class technology, design a 9-stage ring oscillator at 1 GHz with voltage swing of 1.2V using the differential buffer delay stage of Fig. 1. Adjust the V_{BP}, V_{BN} bias voltages accordingly (do not design a bias circuit). Use minimum length transistors. You may add additional capacitance at the nodes of the ring oscillator to achieve the specified frequency.

Solution:

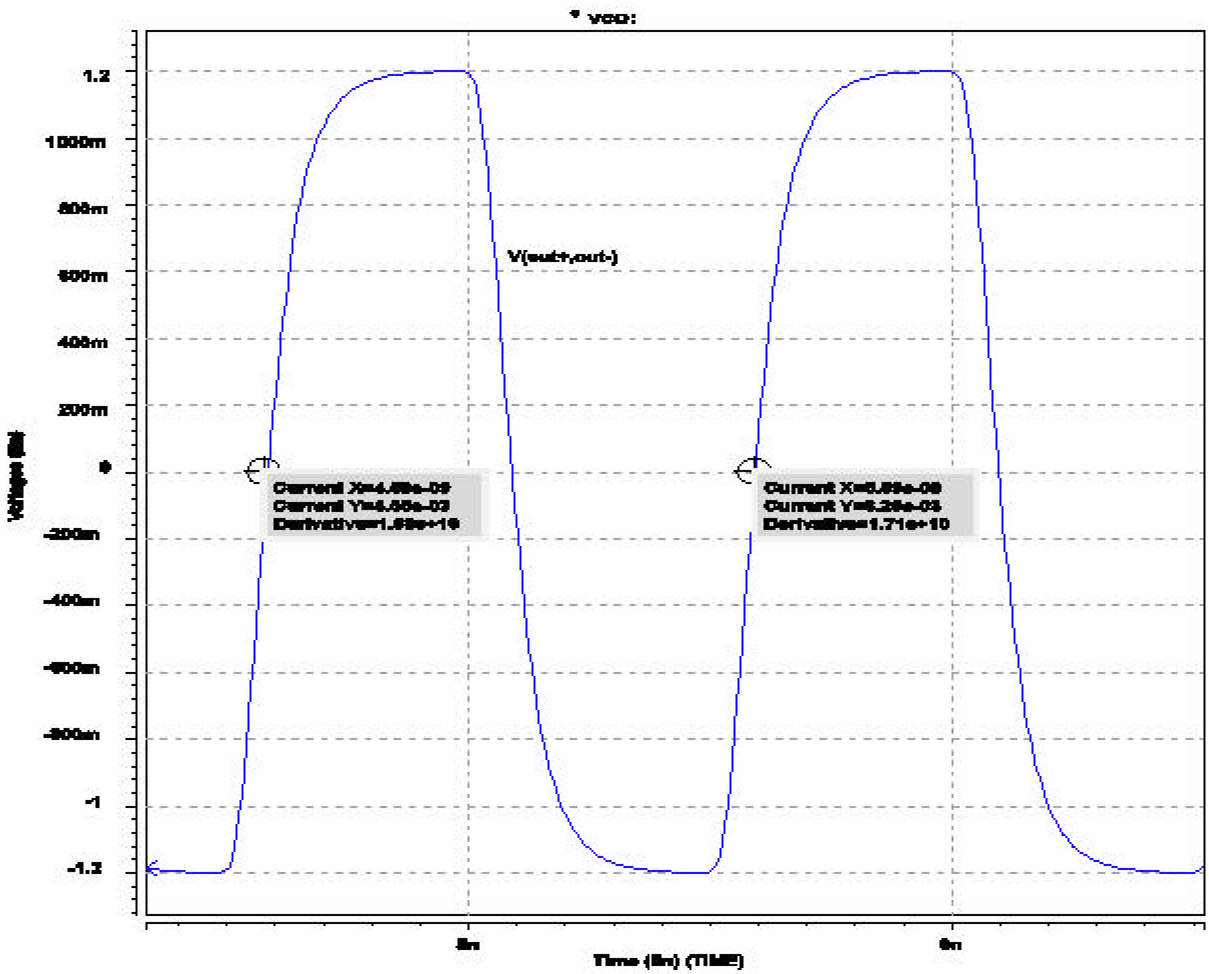
Since the voltage swing is 1.2V (we assume this means single-ended), the value of V_{BP} to V_{DD} should be 1.2V. Assuming a drive ratio between NMOS and PMOS of 2:1 we use the following VCO stage:



We sweep V_{BN} with V(vdd,vin1)=0 and V(vdd,vin2)=1.2V, in order to find the value that gives V(vout1)=0.6V. This way we essentially emulate the replica-bias circuit in Figure 2. The result is shown in the Figure and we get V_{BN}=964 mV.



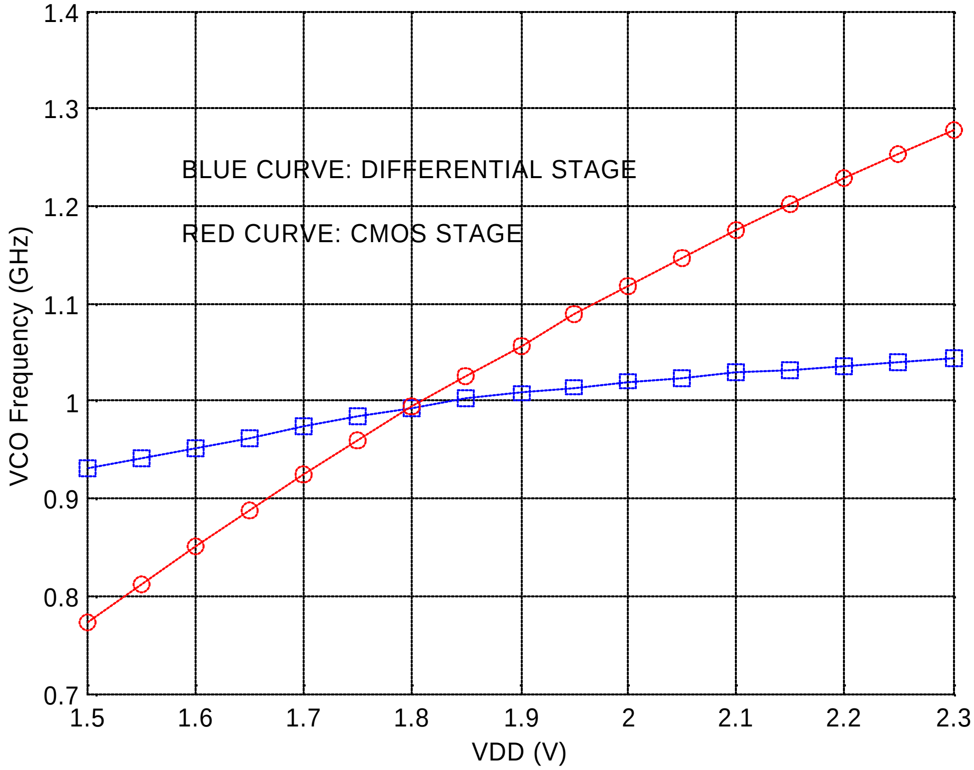
Using these bias voltages, we design a 9-stage oscillator and add caps to get f= 1 GHz. The differential waveform is shown below and is obtained when we add 1.98 fF of capacitance to the output nodes. The voltage swing and frequency are the correct ones.



c) What is the sensitivity of the delay to changes in the supply voltage for this element? Compare it to a symmetrically sized CMOS inverter with same delay. Use HSPICE.

Solution:

We build a 9-stage 1GHz oscillator out of CMOS stages. We use approximately the same sizes as in the differrential stage oscillator (WP=0.5u, WN=0.25u) and add 2.9fF capacitances at the outputs to achieve 1 GHz oscillation frequency.The following figure shows the oscillation frequency in the two cases as a function of the supply voltage.



From this figure we can determine the average sensitivity of the two VCOs.
Sensitivity for differential stage VCO: 143.4 MHz/V
Sensitivity for CMOS stage VCO: 632.5 MHz/V

d) Describe the operation of the replica-feedback bias circuit of Fig. 2.

Solution:
In order to obtain the correct levels for the differential VCO stage, we take the output of the half-buffer replica when its input is equal to VDD and VBP=Vctrl, and we compare that output to Vctrl using the Diff. Amplifier. Using negative feedback, we adjust VBN, so that the output voltage is equal to Vctrl.