

UNIVERSITY OF CALIFORNIA AT BERKELEY
College of Engineering
Department of Electrical Engineering and Computer Science

R. W. Brodersen
David Sobel
Sohrab Emami

Design Problem 1
(Due 10/06/04)

EECS 140
Fall 2004

This project must be performed individually. Each person should turn in a project report. Information on what to include in the report and how to submit your circuit will be available later.

Design Objective

The objective of this project is to design an operational amplifier with a differential input and a single-ended output. It must meet the following specifications:

Specification	Condition	Notes
L _{min}	0.13μm	L must be integer multiple of 0.01μm
W _{min}	0.15μm	W must be integer multiple of 0.01μm
V _{DD}	1.2V	
V _{SS}	0V	
R _L	1kΩ	Don't include this device in your schematic. It is automatically included in the testbenches
A _{DM} (=V _{out} /V _{id})	≥1000	Small-signal differential-mode voltage gain
A _{CM} (=V _{out} /V _{ic})	≤0.1	Small-signal common-mode voltage gain
V _{ICM,max} - V _{ICM,min}	≥0.5V	A _{DM} and A _{CM} specs must be met over this common-mode swing
V _{out,pp}	≥0.6V	A _{DM} spec must be met over this output swing. V _{OUT} must swing from V _{DD} /2+300mV to V _{DD} /2-300mV while maintaining A _{DM}
Area	Minimize	
Power	Minimize	

The available circuit components are NMOS transistors, PMOS transistors or resistors. Ideal sources can only be used to generate the supply voltages, not to generate bias currents or voltages. The design specifications are as following,

The design goal is to minimize the following figure of merit ($Watts \cdot \mu m^2$),

$$FOM = Power \cdot Area$$

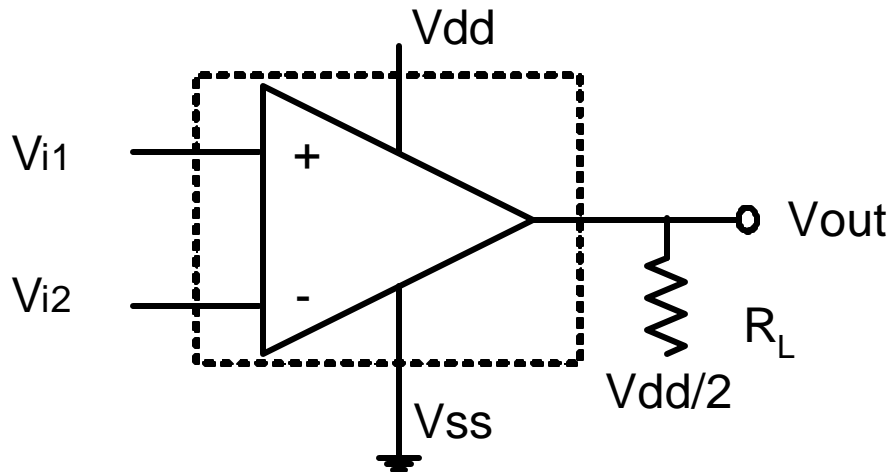


Figure 1

Area Calculation

Calculate the area by adding up the gate area ($W \cdot L$) of all the transistors and the area of the resistors. For the transistors, the minimum L is $0.13 \mu\text{m}$ and the minimum W is $0.15 \mu\text{m}$. For the resistors, the minimum W and L are $0.5 \mu\text{m}$; the sheet resistance is 250ohm/square . You are allowed to tie the bulk of any transistor to the source instead of to the positive or negative supply, but at the cost of an area penalty. If you choose to tie the bulk to the source, the area of the transistor should be doubled.

Device Models

http://bwrc.eecs.berkeley.edu/classes/ee140/dp/model_ee140.sp

The device models are encapsulated in a sub-circuit; use:

```
x1 d g s b nmos w=10u l=0.13u
```

```
x2 d g s b pmos w=10u l=0.13u
```

to instantiate an NMOS and a PMOS transistor respectively (you have to use the prefix 'x' instead of 'm'). The reason for using a subcircuit is to allow λ to decrease with increasing transistor length. The output resistance parameter λ will stay the same as before for minimum length transistors ($L_{\text{min}}=0.13\mu\text{m}$), but will decrease with increasing L (drawn L , not effective L). Since the output resistance is proportional to $1/\lambda$, the output resistance increases with increasing L . Since we are using level-2 device model, it is worthwhile to calculate level-1 parameters of the device model for your hand calculations.

Spice testbenches

Test benches will be provided for you to run a set of simulation tests on your circuit. Ultimately, your final circuit performance will be evaluated by these testbenches, so be sure to familiarize yourself with them. (The TA's will be going over them in section.) More information on the testbenches (and the testbenches themselves) will be released in another document on the website.

Please note that the testbench files will include all your input sources (power, signal) as well as your output load. Therefore, you do NOT need to include these devices in your own netlist. See other handout for more information.

What to include in your report

See handout on webpage

Grading

100 points total:

25 points for conciseness and clearness of the report

25 points for meeting the specifications for everything but A_{DM}

20 points for meeting the A_{DM} specification

20 points for how well FOM is minimized

10 points for originality and robustness of design