UNIVERSITY OF CALIFORNIA AT BERKELEY
College of Engineering
Department of Electrical Engineering and Computer Science

R. W. Brodersen
Sohrab Emami
David Sobel

Design Problem 2
(Due 11/10/04)

EECS 140
Fall 2004

You can work in groups of two, or alone. If you work in groups of two, submit only one project report per group. There will be no extra credit for working alone.
Information on what to include in the report and how to submit your circuit will be available later.

Design Objective

The objective of this project is to design an operational amplifier (Figure 1) with a differential input and a single-ended output. It must meet the following specifications:

Specification	**Condition**	**Notes**
L_{min}	0.13um	L must be integer multiple of 0.01um
W_{min}	0.15um	W must be integer multiple of 0.01um
$V_{DD\text{-}min}$	1.2V	Supply voltage, V_{DD}, varies from $V_{DD\text{-}min}$ to $V_{DD\text{-}max}$.
$V_{DD\text{-}max}$	1.4V	
V_{SS}	0V	
R_L	1kΩ	Don't include the load in your schematic. It is automatically included in the testbenches
R_S	500Ω	Don't include the source resistance in your schematic. It is included in the testbenches
A_{DM0} (= v_{out}/v_{id})	≥1000	Low frequency small-signal differential-mode voltage gain
A_{CM0} (= v_{out}/v_{ic})	≤0.1	Low frequency small-signal common-mode voltage gain
$V_{ICM,max}$ - $V_{ICM,min}$	≥0.3V	A_{DM0} and A_{CM0} specs must be met over this common-mode swing for both $V_{DD\text{-}min}$ and $V_{DD\text{-}max}$ @ V_{OUT}=0.6V
$V_{out,pp}$	≥0.6V	A_{DM0} spec must be met over this output swing for both $V_{DD\text{-}min}$ and $V_{DD\text{-}max}$ @ $V_{ICM,Q}$. (i.e. V_{OUT} must swing from 300mV to 900mv while maintaining A_{DM0} spec.)
Maximum supply current	1mA	Maximum supply current over the entire range of V_{out} and V_{DD}.
3dB-bandwidth of $A_{DM}(f)$ (= $v_{out}(f)/v_{id}(f)$)	**Maximize**	At V_{out}=0.6V, V_{DD}=1.2V, and V_{ICM}=$V_{ICM,Q}$. Also $\lvert A_{CM}(f)\rvert$ must remain less than 0.1 over this bandwidth.

And the design goal is to **maximize the 3dB-bandwidth** of the differential to single-ended voltage gain of the amplifier.

The available circuit components are NMOS transistors, PMOS transistors, and resistors. (Ideal internal sources can not be used to generate bias currents or voltages.)

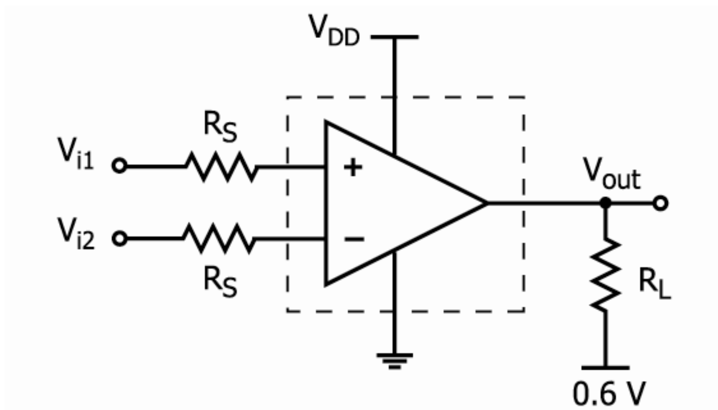

Figure 1

Device Models

http://bwrc.eecs.berkeley.edu/classes/ee140/dp/model_ee140.sp

The device models are encapsulated in a sub-circuit; use:

```
x1 d g s b nmos w=10u l=0.13u
x2 d g s b pmos w=10u l=0.13u
```

to instantiate an NMOS and a PMOS transistor respectively (you have to use the prefix ‘x’ instead of ‘m’). The reason for using a subcircuit is to allow λ to decrease with increasing transistor length. The output resistance parameter λ will stay the same as before for minimum length transistors (L_{min}=0.13μm), but will decrease with increasing L (drawn L, not effective L). Since the output resistance is proportional to 1/ λ, the output resistance increases with increasing L.

Spice testbenches

Test benches will be provided for you to run a set of simulation tests on your circuit. Ultimately, your final circuit performance will be evaluated by these testbenches. More information on the testbenches (and the testbenches themselves) will be released in another document on the website.

Please note that the testbench files will include all your input sources (power, signal) as well as your source and output resistances. Therefore, you do NOT need to include these devices in your own netlist.

What to include in your report

See handout on webpage

Grading

100 points total:
25 points for conciseness and clearness of the report
40 points for meeting the specifications
25 points for how well the 3-dB bandwidth is maximized.
10 points for originality of the design.