

**UNIVERSITY OF CALIFORNIA AT BERKELEY**  
**College of Engineering**  
**Department of Electrical Engineering and Computer Science**

R. W. Brodersen  
S. Emami  
D. Sobel

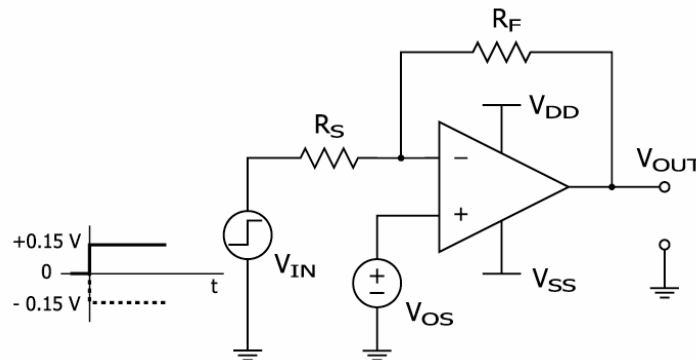
Design Problem 3  
(Due 12/13/04)

EECS 140  
Fall 2004

You can work in groups of two, or alone. If you work in groups of two, submit only one project report per group. There will be no extra credit for working alone. Information on what to include in the report and how to submit your circuit will be available later.

### Design Objective

The goal of this project is to design an operational amplifier with a differential input and a single ended output. Figure 1 shows the feedback configuration for which the operational amplifier has to be designed.



**Figure 1** Feedback configuration

The amplifier specifications are listed in Table 1 and your design must meet the specs over the process corners. (slow, typical, and fast)

The closed loop gain of the circuit is (very close to)  $R_F/R_S = 2$ . Thus, for a 0.3 V peak-to-peak input voltage range, the peak-to-peak output voltage range should be 0.6 V.

**The figure of merit of the amplifier is the settling time.** (worst case over the process corners) The settling is measured for a step at the input going from 0 to  $\pm V_{in,pp}/2$ . The settling accuracy of  $\pm 0.02\%$  relates to both the dynamic settling error, and the settling error due to a finite amplifier gain (static settling error).

The  $A_{cm}$  specification applies to the open loop amplifier (without feedback). You are free to use a small input offset voltage source ( $< 1$  mV) to bias the output voltage at 0 V.

The available circuit components are NMOS transistors, PMOS transistors, and capacitors. You are allowed to use only one resistor. Ideal sources can only be used to generate the supply voltages, not to generate bias currents or voltages.

Specification	Condition	Notes
$L_{\min}$	0.13 $\mu\text{m}$	L must be integer multiple of 0.01 $\mu\text{m}$
$W_{\min}$	0.15 $\mu\text{m}$	W must be integer multiple of 0.01 $\mu\text{m}$
$V_{\text{DD}}$	+0.6V	Positive supply voltage
$V_{\text{SS}}$	- 0.6V	Negative supply voltage
$R_{\text{F}}$	1k $\Omega$	Don't include this resistor in your schematic. It is automatically included in the testbenches.
$R_{\text{S}}$	500 $\Omega$	Don't include this resistor in your schematic. It is automatically included in the testbenches.
$A_{\text{CM0}}$	$\leq 0.1$	Low frequency, open-loop small-signal common-mode voltage gain.
Maximum supply current	1mA	Maximum supply current over the entire range of operation.
Settling accuracy	0.02%	Due to both the dynamic settling error and the settling error due to a finite amplifier gain (static settling error).
$t_{\text{settle}}$	Minimize	Worst case settling time. (over the process variation)

**Table 1**

## Device models and process variation

[http://bwrc.eecs.berkeley.edu/classes/ee140/dp/model\\_ee140.lib](http://bwrc.eecs.berkeley.edu/classes/ee140/dp/model_ee140.lib)

The device models are encapsulated in a sub-circuit; use:

```
x1 d g s b nmos w=10u l=0.13u
x2 d g s b pmos w=10u l=0.13u
```

to instantiate an NMOS and a PMOS transistor respectively (you have to use the prefix 'x' instead of 'm'). The reason for using a subcircuit is to allow  $\lambda$  to decrease with increasing transistor length. The output resistance parameter  $\lambda$  will stay the same as before for minimum length transistors ( $L_{\min}=0.13\mu\text{m}$ ), but will decrease with increasing L (drawn L, not effective L). Since the output resistance is proportional to  $1/\lambda$ , the output resistance increases with increasing L.

Your design will be evaluated over the process corners. (typical (TT), fast (FF), and slow (SS) transistor models) This can be done by using the following HSPICE statements:

```
.include circuit.sp
.LIB 'modle_ee140.lib' TT
.
.
.ALTER
.DEL LIB 'model_ee140.lib' TT $removes LIB from memory
.PROT $protect statements below .PROT
.LIB 'model_ee140.lib' FF $get fast model library
.UNPROT
```

## **Spice testbenches**

Test benches will be provided for you to run a set of simulation tests on your circuit. Ultimately, your final circuit performance will be evaluated by these testbenches. More information on the testbenches (and the testbenches themselves) will be released in another document on the website.

Please note that the testbench files will include all your input sources (power, signal) as well as feedback network resistances. Therefore, you do NOT need to include these devices in your own netlist.

## **What to include in your report**

See handout on webpage.