University of California
Berkeley

College of Engineering
Department of Electrical Engineering
and Computer Science

Robert W. Brodersen
EECS140

Analog Circuit Design

I-1

EECS 140
ANALOG INTEGRATED CIRCUITS

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This course will focus on the design of MOS analog integrated circuits with extensive use of Spice for the simulations. In addition, some applications of analog integrated circuits will be covered which will include RF amplification and discrete and continuous time filtering. Though the focus will be on MOS implementations, comparison with bipolar circuits will be given.

Required Text

Analysis and Design of Analog Integrated Circuits, 4th Edition, P.R. Gray, P. Hurst, S. Lewis and R.G. Meyer, John Wiley and Sons, 2001

Supplemental Texts

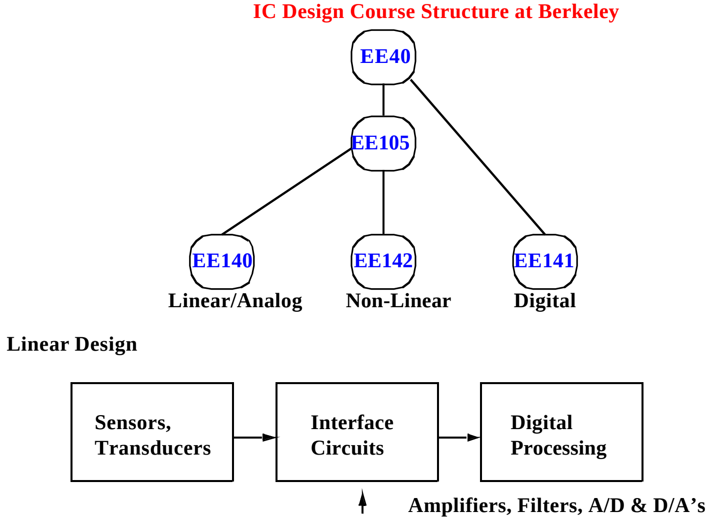
B. Razavi, Design of Analog CMOS Integrated Circuits, McGraw-Hill, 2001.
Thomas Lee, The Design of CMOS Radio Frequency Integrated Circuits, Cambridge University Press, 1998
The SPICE Book, Andre Vladimirescu, John Wiley and Sons, 1994

Prerequisites

EECS 105: Microelectronic Devices and Circuits

I-2

IC Design Course Structure at Berkeley



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Analog Circuit Design

Lectures
on
MOS DEVICE MODELS

M-1

Assumed Knowledge

a) KCL, KVL - Kirchoff Laws

b) Voltage, Current Dividers

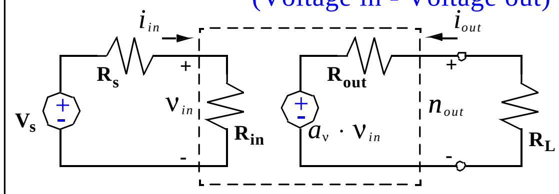
c) Thevenin, Norton Equivalents

d) 2-Port Equivalents

e) Phasors, Frequency Response

M-2

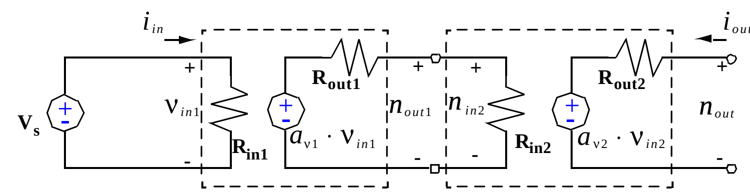
2-Port Equivalent Circuit (Voltage in - Voltage out)



$$R_{in} = \left.\frac{v_{in}}{i_{in}}\right|_{R_L \to \infty}^{i_{out} \to 0}$$

$$R_{out} = \left.\frac{v_{out}}{i_{out}}\right|_{R_S = v_{in} = 0}$$

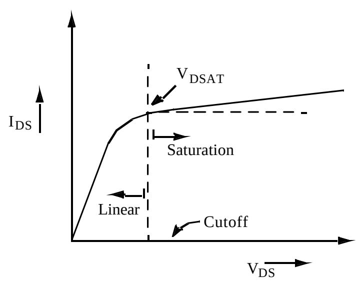
$$A_v = \left.\frac{v_{out}}{v_{in}}\right|_{R_L \to \infty}$$

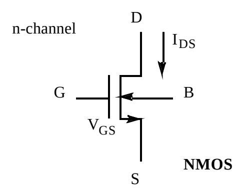


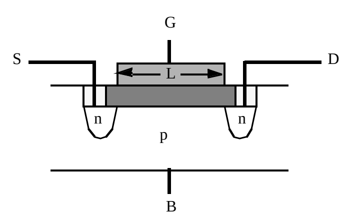
$$n_{out} = a_{v2} \cdot v_{in2} = a_{v2} \cdot v_{out1} = a_{v2} \cdot \left(a_{v1} \cdot v_{in1} \cdot \left(\frac{R_{in2}}{R_{out1} + R_{in2}}\right)\right)$$

M-3

MOS Large Signal Equations







M-4

MOS Large Signal Equations (Cont.)

Cutoff :

$V_{GS} < V_T$

Linear :

$V_{GS} > V_T$

$V_{DS} < V_{DSAT} = V_{GS} - V_T$

$$I_{DS} = k' \cdot \frac{W}{L} \cdot \left(V_{GS} - V_T - \frac{V_{DS}}{2}\right) \cdot V_{DS}$$

Saturated :

$V_{GS} > V_T$

$V_{DS} > V_{DSAT} = V_{GS} - V_T$

$$I_{DS} = \frac{k'}{2} \cdot \frac{W}{L} \cdot (V_{GS} - V_T)^2 (1 + \lambda \cdot V_{DS})$$

MOS Large Signal Equations (Cont.)

M-5

$$V_T = V_{To} + \gamma \cdot [(2 \cdot \phi_f + V_{SB})^{\frac{1}{2}} - (2 \cdot \phi_f)^{\frac{1}{2}}]$$

$$(V_{SB} > 0)$$

$V_{To} \equiv$ Threshold Voltage @ $V_{SB} = 0$

$\phi_f \equiv$ Fermi Potential ≈ 0.3

$\gamma \equiv$ Body Effect Factor

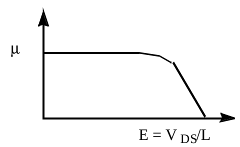
$\lambda \equiv$ Short Channel Effect

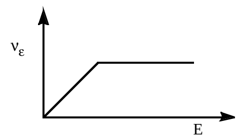
$W \equiv$ Width of Device

$L \equiv$ Length

$k' = \mu \cdot C_{ox}$

mobility — Oxide Capacitance

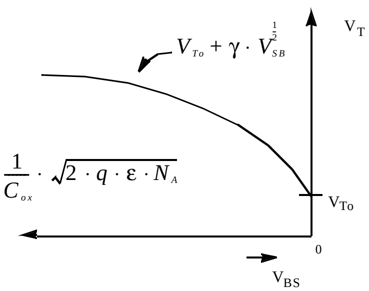




MOS Large Signal Equations (Cont.)

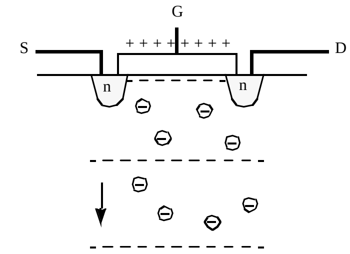
M-6

Body Effect :



$V_{To} + \gamma \cdot V_{SB}^{\frac{1}{2}}$

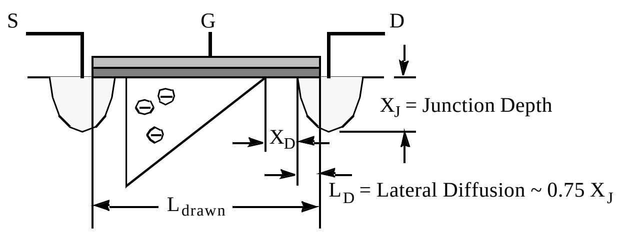
$$\gamma = \frac{1}{C_{ox}} \cdot \sqrt{2 \cdot q \cdot \varepsilon \cdot N_A}$$



MOS Large Signal Equations (Cont.)

M-7

Short Channel Effect (λ):



$$L = L_{drawn} - 2 \cdot L_D$$

$$L_{EFF} = L - X_D$$

$$X_D = f(V_{DS})$$

MOS Large Signal Equations (Cont.)

M-8

$$I_D^{(A)} = \frac{k'}{2} \cdot \frac{W}{L_{EFF}} \cdot (V_{GS} - V_T)^2$$

Modeled as

$$I_D^{(B)} = \frac{k'}{2} \cdot \frac{W}{L} \cdot (V_{GS} - V_T)^2 \cdot (1 + \lambda \cdot V_{DS})$$

$$\frac{\partial I_D^{(B)}}{\partial V_{DS}} = \lambda \cdot I_{DS}$$

$$\frac{\partial I_D^{(A)}}{\partial V_{DS}} = -\frac{k'}{2} \cdot \frac{W}{L_{EFF}^2} \cdot (V_{GS} - V_T)^2 \cdot \frac{dL_{EFF}}{dV_{DS}}$$

$$\frac{\partial I_D^{(A)}}{\partial V_{DS}} = \frac{I_D}{L_{EFF}} \cdot \frac{dX_D}{dV_{DS}} = \lambda \cdot I_D$$

MOS Large Signal Equations (Cont.)

$$\lambda = \frac{1}{L_{EFF}} \cdot \left(\frac{dX_D}{dV_{DS}}\right) \approx \frac{1}{L} \cdot \left(\frac{dX_D}{dV_{DS}}\right)$$

↑ Weak function of V_{DS}

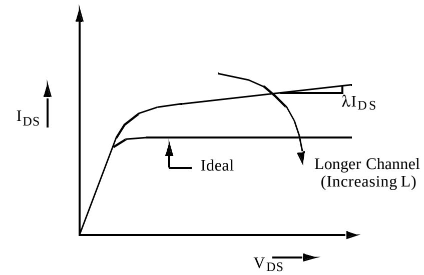
$$X_D \approx \left[\frac{2 \cdot \varepsilon \cdot (V_{DS} - V_{DSAT})}{q \cdot N_A}\right]^{\frac{1}{2}}$$

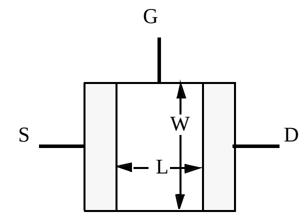
Fixed → ε = Dielectric constant of silicon

N_A = Substrate doping

$$\frac{dX_D}{dV_{DS}} = \frac{1}{2} \cdot \left(\frac{2 \cdot \varepsilon}{q \cdot N_A}\right)^{\frac{1}{2}} \cdot \left(\frac{1}{V_{DS} - V_{DSAT}}\right)^{\frac{1}{2}}$$

MOS Large Signal Equations (Cont.)

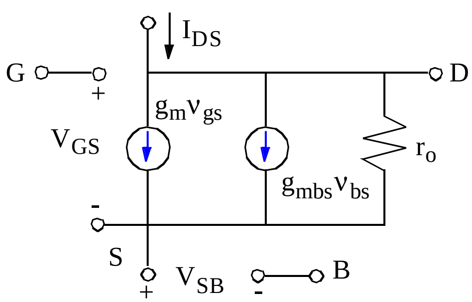




W/L is the parameter of interest

$$C_G \propto W \cdot L \cdot C_{ox}$$

MOS Small Signal Model (Low Frequency)



$$I_{DS} = \underbrace{\frac{dI_{DS}}{dV_{GS}}}_{g_m} \cdot v_{gs} + \underbrace{\frac{dI_{DS}}{dV_{BS}}}_{g_{mbs}} \cdot v_{bs} + \underbrace{\frac{dI_{DS}}{dV_{DS}}}_{1/r_o} \cdot v_{ds}$$

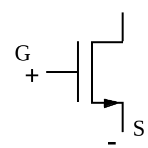
MOS Small Signal Model (Cont.)

<u>In Saturation :</u>

$$g_m = \frac{dI_{DS}}{dV_{GS}} = k' \cdot \frac{W}{L} \cdot (V_{GS} - V_T) \cdot (1 + \lambda \cdot V_{DS})$$

$$g_m \approx k' \cdot \frac{W}{L} \cdot (V_{GS} - V_T) = k' \cdot \frac{W}{L} \cdot V_{DSAT} = \left(2 \cdot k' \cdot \frac{W}{L} \cdot I_{DS}\right)^{\frac{1}{2}}$$

What is V_{DSAT} ?



$$I_{DS} = \frac{k'}{2} \cdot \frac{W}{L} \cdot (V_{GS} - V_T)^2 = \frac{k'}{2} \cdot \frac{W}{L} \cdot V_{DSAT}^2$$ and from above,

$$g_m = k' \cdot \frac{W}{L} \cdot V_{DSAT}$$ so,

$$V_{GS} = V_T + V_{DSAT}$$

$$V_{DSAT} = \left(\frac{2 \cdot I_{DS}}{k' \cdot W/L}\right)^{\frac{1}{2}}$$

MOS Small Signal Model (Cont.)

M-13

g_{mbs} calculation :

$$g_{mbs} = g_{mb} = \frac{dI_{DS}}{dV_{BS}} = -k' \cdot \frac{W}{L} \cdot (V_{GS} - V_T) \cdot (1 + \lambda \cdot V_{DS}) \cdot \frac{dV_T}{dV_{BS}}$$

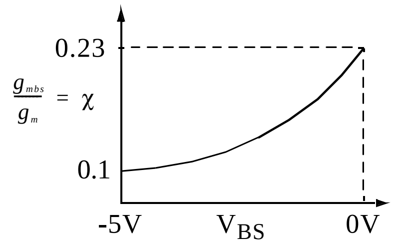
$$\frac{dV_T}{dV_{BS}} = -\frac{\gamma}{2 \cdot (2 \cdot \phi_f + V_{SB})^{0.5}} \equiv -\chi$$

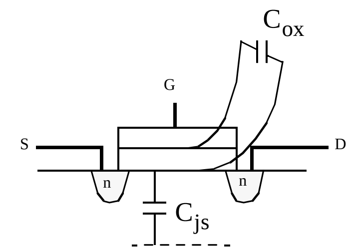
$$g_{mbs} = \underbrace{k' \cdot \frac{W}{L} \cdot (V_{GS} - V_T) \cdot (1 + \lambda \cdot V_{DS})}_{g_m} \cdot \chi$$

$$\boxed{\frac{g_{mbs}}{g_m} = \chi} \qquad \boxed{\chi = \frac{\gamma}{2 \cdot (2 \cdot \phi_f + V_{SB})^{0.5}}}$$

MOS Small Signal Model (Cont.)

M-14





$\gamma = 0.5$
$\phi_f = 0.3$
$k' = 90e\text{-}6$
$\lambda = 0.01$
$V_{To} = 0.7$

$$Qchannel_{duetovgs} \approx C_{ox} \cdot v_{gs}$$

$$Qchannel_{duetovbs} \approx C_{js} \cdot v_{bs}$$

$$\chi = \frac{C_{js}}{C_{ox}}$$

MOS Small Signal Model (Cont.)

M-15

r_o calculation :

$$\frac{1}{r_o} = \left(g_{mds} = \frac{dI_{DS}}{dV_{DS}} = \frac{d}{dV_{DS}} \left(\frac{k'}{2} \cdot \frac{W}{L} \cdot (V_{GS} - V_T)^2 \cdot (1 + \lambda \cdot V_{DS}) \right) \right)$$

$$\frac{1}{r_o} = \frac{k'}{2} \cdot \frac{W}{L} \cdot (V_{GS} - V_T)^2 \cdot \lambda$$

$$\frac{1}{r_o} = \lambda \cdot I_{DS}$$

$$r_0 = \frac{1}{\lambda \cdot I_{DS}}$$

MOS Small Signal Model (Cont.)

M-16

<u>Comparison with Spice Level 1</u>:

$$VTO = V_{To} \sim 0.5 \rightarrow 1.0V$$

$$PHI = 2 \cdot \phi_f \sim 0.6$$

$$GAMMA = \gamma \sim 0.05 \rightarrow 0.5$$

$$LAMBDA = \lambda \sim 0.01 \rightarrow 0.1$$

$$KP = k' = \mu \cdot C_{ox} \sim nmos \rightarrow 50 - 100\mu\frac{A}{V^2}$$

$$pmos \approx \frac{1}{3} nmos$$

MOS Small Signal Model (Cont.)

Summary:

$$g_m \approx \left(2 \cdot k' \cdot \frac{W}{L} \cdot I_{DS}\right)^{\frac{1}{2}} = k' \cdot \frac{W}{L} \cdot V_{DSAT} = \frac{2 \cdot I_{DS}}{V_{DSAT}}$$

$$g_{mbs} = \chi \cdot g_m$$

$$\chi = \frac{\gamma}{2 \cdot (2 \cdot \phi_f + V_{SB})^{0.5}}$$

$$r_0 = \frac{1}{\lambda \cdot I_{DS}}$$

$$\frac{I_{DS}}{g_m} = \frac{V_{GS} - V_T}{2} = \frac{V_{DSAT}}{2}$$

$$V_{DSAT} = \left(\frac{2 \cdot I_{DS}}{k' \cdot W / L}\right)^{\frac{1}{2}}$$

$$V_{DSAT} = V_{GS} - V_T$$

$$V_{GS} = V_T + \left(\frac{2 \cdot I_{DS}}{k' \cdot W / L}\right)^{\frac{1}{2}}$$

$$I_{DS} = \frac{k'}{2} \cdot \frac{W}{L} \cdot (V_{GS} - V_T)^2$$

$$V_T = V_{To} + \gamma \cdot [(2 \cdot \phi_f + V_{SB})^{\frac{1}{2}} - (2 \cdot \phi_f)^{\frac{1}{2}}]$$

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Analog Circuit Design

Lectures on SPICE

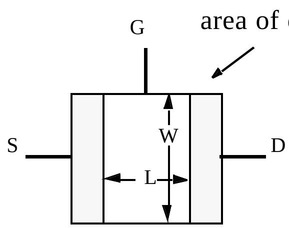
Spice Transistor Model :

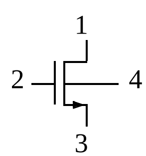
M1 1 2 3 4 nch L=1µ W=10µ

AD=( ) AS=( ) PD=( ) PS=( ) NRD=( )

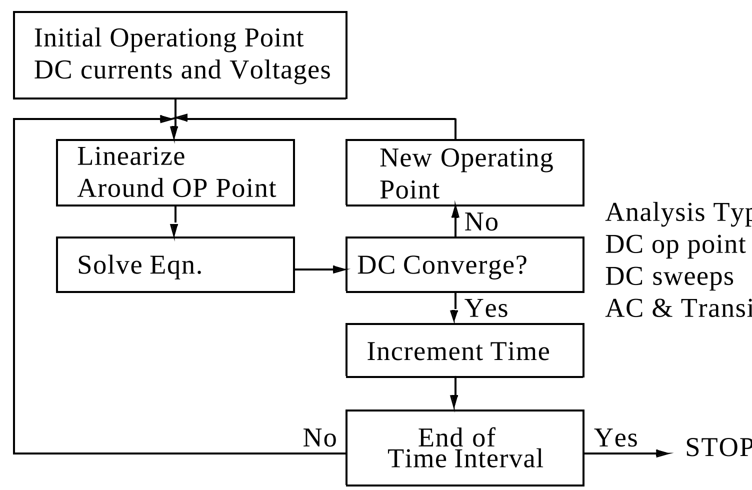
parasitic resistors

area of drain



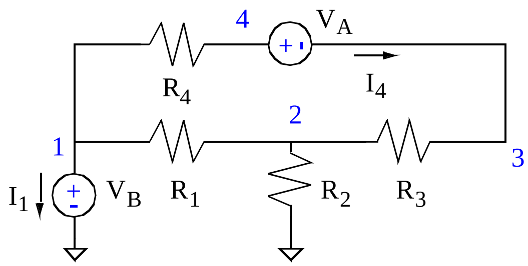


SPICE



Analysis Types :
DC op point .op
DC sweeps
AC & Transient

SP-3



$G_i = 1/R_i$

$$\begin{aligned}
\text{Node 1}: &\quad (G_1 + G_4)\cdot V_1 - G_1\cdot V_2 - G_4\cdot V_4 + I_1 = 0\\
\text{Node 2}: &\quad -G_1\cdot V_1 + (G_1+G_2+G_3)\cdot V_2 - G_3\cdot V_3 = 0\\
\text{Node 3}: &\quad -G_3\cdot V_2 + G_3\cdot V_3 - I_4 = 0\\
\text{Node 4}: &\quad -G_4\cdot V_1 + G_4\cdot V_4 + I_4 = 0\\
&\quad V_1 = V_B\\
&\quad -V_3 + V_4 = V_A
\end{aligned}$$

SP-4

$$\begin{bmatrix} G_1+G_4 & -G_1 & 0 & -G_4 & 1 & 0\\ -G_1 & G_1+G_2+G_3 & -G_3 & 0 & 0 & 0\\ 0 & -G_3 & -G_3 & 0 & 0 & -1\\ -G_4 & 0 & 0 & -G_4 & 0 & 1\\ 1 & 0 & 0 & 0 & 0 & 0\\ 0 & 0 & -1 & 1 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_1\\ V_2\\ V_3\\ V_4\\ I_1\\ I_4 \end{bmatrix} = \begin{bmatrix} 0\\ 0\\ 0\\ 0\\ V_B\\ V_A \end{bmatrix}$$

Current src

$$\begin{bmatrix} G & F\\ B & R \end{bmatrix} \begin{bmatrix} V\\ I \end{bmatrix} = \begin{bmatrix} C\\ E \end{bmatrix}$$

Votlage src

Total # of EQNS $N = n + n_v + n_l$

n = # of circuit nodes

n_v = # of independent voltage srcs

n_l = # of inductors

SP-5

Matrix Solution

$$[A][x] = [b]$$

x — we need

Solve by Gaussian Elimination

(0) denotes iteration step

$$\begin{matrix} e_1^{(0)}\\ e_2^{(0)}\\ e_3^{(0)} \end{matrix} \begin{bmatrix} a_{11}^{(0)} & a_{12}^{(0)} & a_{13}^{(0)}\\ a_{21}^{(0)} & a_{22}^{(0)} & a_{23}^{(0)}\\ a_{31}^{(0)} & a_{32}^{(0)} & a_{33}^{(0)} \end{bmatrix} \begin{bmatrix} x_1\\ x_2\\ x_3 \end{bmatrix} = \begin{bmatrix} b_1^{(0)}\\ b_2^{(0)}\\ b_3^{(0)} \end{bmatrix}$$

Eliminate a_{21}, a_{31}

$$e_1^{(1)} = e_1^{(0)} \qquad e_2^{(1)} = e_2^{(0)} - \frac{a_{21}^{(0)}}{a_{11}^{(0)}}\cdot e_1^{(0)} \qquad e_3^{(1)} = e_3^{(0)} - \frac{a_{31}^{(0)}}{a_{11}^{(0)}}\cdot e_1^{(0)} \qquad \begin{bmatrix} x & x & x\\ 0 & x & x\\ 0 & x & x \end{bmatrix}$$

SP-6

Then eliminate $a_{32}^{(1)}$

$$\begin{aligned} e_1^{(2)} &= e_1^{(1)}\\ e_2^{(2)} &= e_2^{(1)}\\ e_3^{(2)} &= e_3^{(1)} - \frac{a_{32}^{(1)}}{a_{22}^{(1)}}\cdot e_2^{(1)} \end{aligned} \qquad \begin{bmatrix} x & x & x\\ 0 & x & x\\ 0 & 0 & x \end{bmatrix}$$

Upper triangular matrix can be solved

$$\begin{bmatrix} a_{11}^{(2)} & a_{12}^{(2)} & a_{13}^{(2)}\\ 0 & a_{22}^{(2)} & a_{23}^{(2)}\\ 0 & 0 & a_{33}^{(2)} \end{bmatrix} \begin{bmatrix} x_1\\ x_2\\ x_3 \end{bmatrix} = \begin{bmatrix} b_1^{(0)}\\ b_2^{(1)}\\ b_3^{(2)} \end{bmatrix}$$

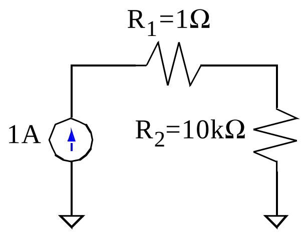
$$\begin{aligned} x_3 &= \frac{b_3^{(2)}}{a_{33}^{(2)}}\\ x_2 &= \frac{(b_2^{(1)} - a_{23}^{(1)}\cdot x_3)}{a_{22}^{(1)}}\\ x_1 &= \frac{(b_1^{(0)} - a_{13}^{(0)}\cdot x_3 - a_{12}^{(0)}\cdot x_2)}{a_{11}^{(0)}} \end{aligned}$$

Solution

SP-7

Accuracy

Can’t divide by 0 or small numbers, so pivoting is used to reorder eqn’s (Basically renumbering nodes). Puts maximum values on diagonal.



$$\begin{bmatrix} 1 & -1 \\ -1 & 1.0001 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} 1 \\ 0 \end{bmatrix}$$

$$\frac{1}{1} - \frac{1}{10k} = G_1 + G_2$$

If the computer only has 4 digits of precision then we get,

$$\begin{bmatrix} 1 & -1 \\ -1 & 1 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} 1 \\ 0 \end{bmatrix}$$

$$V_1 - V_2 = 1$$
$$-V_1 + V_2 = 0$$
$$V_1, V_2 = \infty$$

Actually,

$$V_1 = 10,001V$$
$$V_2 = 10,000V$$

SP-8

To control accuracy

.options PIVTOL = <values> (10^{18})

This sets the allowable range of conductance values.

ERROR : Maximum entry ......at STEP .... is less than PIVTOL

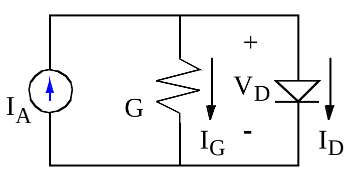
-Probably means you have an incorrect element or floating node

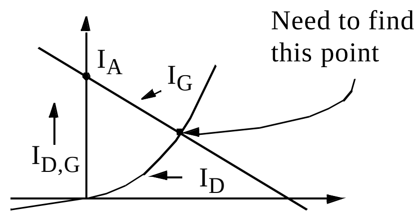
SP-9

Solution of the DC equations with non-linear models

$$I_D = I_s \cdot \left(e^{\frac{V_D}{V_{TH}}} - 1\right)$$

$$I_G = G \cdot V$$



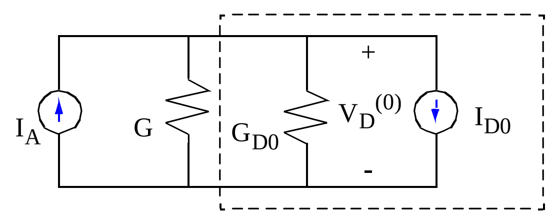


SP-10

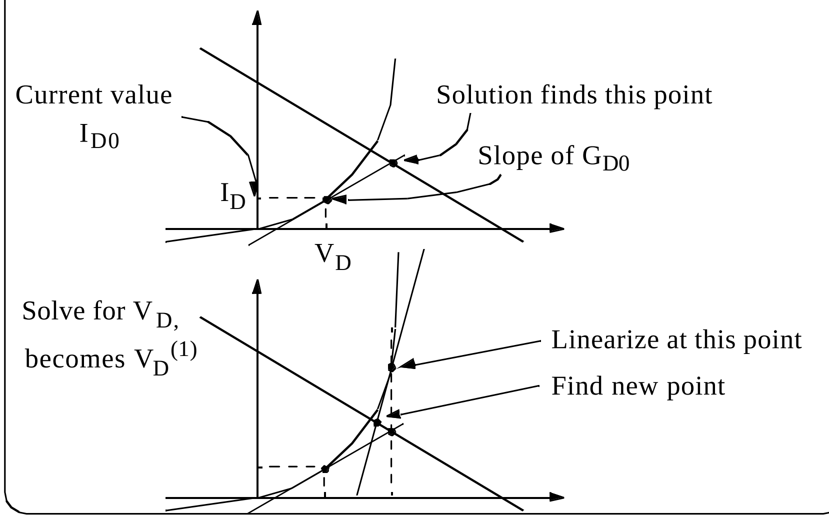
Newton-Raphson Iteration :

- Make guess of next operation point in iteration

Start at initial guess and linearize diode eqn.



SP-11



SP-12

Convergence

Keep iterating until all voltages and currents are within a a tolerance value.

$V_n^{(i)}$ = node voltage n at iteration i

$$\varepsilon_{Vn} = REL(V) \cdot max(|V_n^{(i+1)}|, V_n^{(i)}) + ABS(V)$$

The convergence check is :

$$|V_n^{(i+1)} - V_n^{(i)}| \le \varepsilon_{Vn}$$

$REL(V) \sim 10^{-4}$ (Default 10^{-3})

$ABS(V) \sim 10^{-6}$ (Default $50\mu V$)

ABS(V) should be at least two orders of magnitude below required accuracy.
These values would give 1 part in 10^4 accuracy down to $100\mu V$ resolution

SP-13

Current convergence is broken into two types; MOS and NOT MOS

$$MOS\begin{cases} ABSMOS \sim ABSOLUTE(10^{-6}) \\ RELMOS \sim RELATIVE(0.5) \end{cases}$$

$$NOTMOS\begin{cases} ABSI \sim ABSOLUTE(10^{-9}) \\ RELI \sim RELATIVE(0.01) \end{cases}$$

ITL = # of steps in iteration (200)

When you get

ERROR no convergence in DC analysis and the last node voltages

Then it hasn't converged in 200 times - something is probably wrong with your netlist