



```
xcs2 xcs2d xcs1d vss vss nmos w=0.15u l=0.20985u
xsrc3 xcs2d xg3 vdd vdd pmos w=0.15u l=0.13u
```

```
xcd vdd xcs2d vout vss nmos w=0.48u l=0.13u
rb vdd vout 66
```

```
.ends
```

```
.param vdd = 1.2
```

```
.param victest = 'vic'
```

```
* amplifier
```

```
xa in out vddp vddn amplifier
```

```
* input circuit
```

```
vic com gnd dc 'victest'
```

```
vid in com dc 0 ac 1
```

```
* supply and load
```

```
vddp vddp gnd dc 'vdd'
```

```
vddn gnd vddn dc 0
```

```
rl out gnd 50
```

```
* analysis statements
```

```
.op
```

```
.tf v(out) vid
```

```
.end
```