

GOOD WRITE UP

$A = 18 \mu^2$   
 $P = 13 \mu W$   
 $FOM = 1.57$

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Spring 2004 EE 140 - Design Problem 1 Report

Topology and FOM Minimization strategy

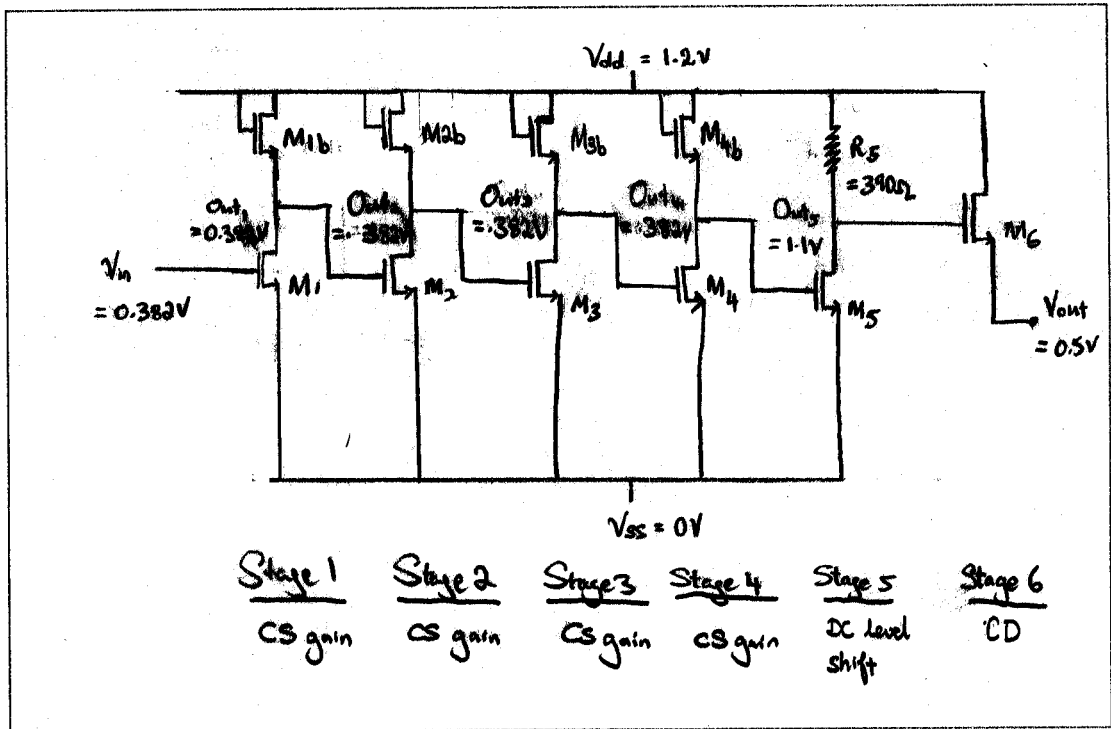


Figure 1: Circuit schematic

In order to minimize the FOM, I need to reduce the current and device areas in the gain stages. This desire is counter balanced by the need to meet the gain specifications. Another consideration is whether I should operate at moderate or strong inversion. While working in moderate inversion would give rise to high gain and small currents, it comes at the price of slower circuits (which is not a factor in this assignment) and greater complexity.

My initial design worked at near sub-threshold regions but after looking at the output stage, I realized that the complexity was not justified since the FOM is dominated by the output stage. Given the 50 ohms load and an output DC level of at least .5V and using a common drain output stage as in figure 2, I would need to run a current of 10mA since  $\frac{.5V}{50\Omega} = 10mA$ .

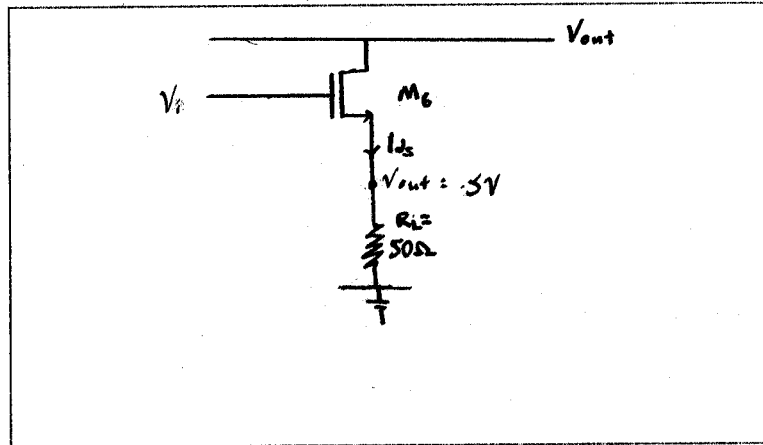


Figure 2: output stage

$$I_d = (W/2L)K(V_i - V_{out} - V_t)^2$$

$$10mA = (W/L)(310\mu A/V^2)(1.1 - .5 - .3)^2$$

This corresponds to a  $(W/L) = 46.5$  even if I have bias the DC input level of this stage at 1.1V. Since I would be working with currents *in the order of* microamps *elsewhere*, the Power consumption contributions from the other stages would be at least an order of magnitude of 3 less. Hence, I decided to work instead at  $V_{gs} > V_t + 3V_{th} = 0.378V$  so that the level 1 models would be valid.

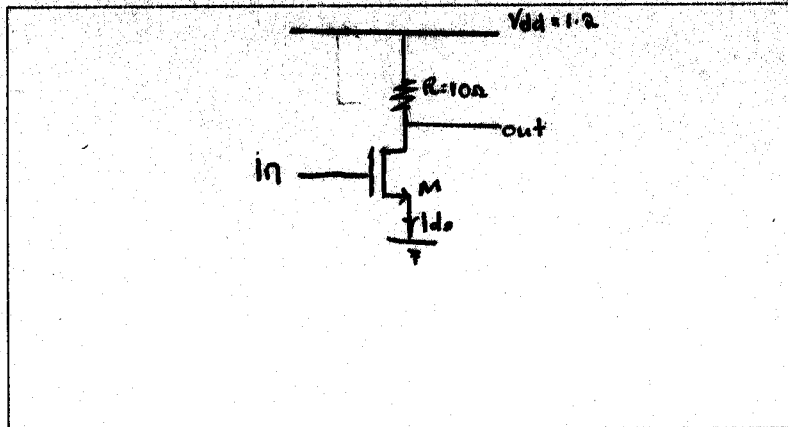


Figure 3: Common Source amp to calculate K

Using a simple common source circuit as in figure 3, I ran a SPICE simulation which generated values for  $G_m$  and  $I_d$  for  $(W/L) = 6\mu/.13\mu$ ,  $.15\mu/.13\mu$ ,  $50\mu/.13\mu$  for  $V_{gs}=.4V$  and  $(W/L) = 6\mu/.13\mu$  for  $V_{gs}=1V$  in the output file. This is summarized in Table 1 below.  $K$  is obtained from back-calculation using  $K = I_d / ((W/L) (V_{gs} - V_t)^2)$

	Simulated Measure Values		Calculated K	$C_m$
	$I_{ds}$	$G_m$		
$(W/L) = 6\mu / .13\mu$ , $V_{gs}=.4V$	143 $\mu A$	2.86mS	619 $\mu A/V^2$	2.86mS
$(W/L) = 50\mu / .13\mu$ , $V_{gs}=.4V$	1.19mA	23.8mS	620 $\mu A/V^2$	23.8mS
$(W/L) = .15\mu / .13\mu$ , $V_{gs}=.4V$	71.6 $\mu A$	71.6 $\mu S$	619 $\mu A/V^2$	71.6 $\mu S$
$(W/L) = 6\mu / .13\mu$ , $V_{gs}=1V$	7mA	20.1mS	620 $\mu A/V^2$	20.1mS

Table 1: Calculating K

I did not calculate  $\lambda$  because its effect on the circuit is  $\ll 10\%$ . From the table, I assumed that the value of  $K$  is constant in the range of values, I would be using at  $K = 620\mu A/V^2$ .

To further reduce area, I used diode-connected transistors with the common source stages, as in figure 4, in place of resistors. This also simplifies the calculation for stage voltage gains since:

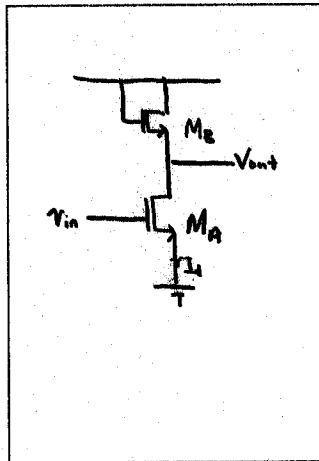


Figure 4 Gain Stage

$$R_{mB} = \frac{1}{g_{mB}} = \frac{1}{\sqrt{\frac{2I_d}{(W/L)_B K}}} = \sqrt{\frac{(L/D)_B K}{2I_d}}$$

$$A_v = g_{m_A} (R_{mB} \parallel r_{o_A})$$

( $r_{o_A}$ ) is assumed large since  $\lambda < .1$ ,  $I_{ds} = 90\mu A \Rightarrow r_o > 10^5 \text{ ohms}$

$$A_v = \frac{g_{m_A}}{g_{m_B}}$$

$$A_v = \sqrt{\frac{(W/L)_A}{(W/L)_B}}$$

to reduce area

Thus, minimizing L to be  $.13\mu m$ , I need only to consider the ratios of the Ws. Choosing the diode connected transistor to be of minimum dimensions  $W = .15\mu m$ ,  $L = .13\mu m$ . I am expecting a  $G_m$  in the order of  $<= 1\text{mS}$  which gives a diode-connected transistor resistance in the order of  $1k$  and a maximum current in the order of  $100\mu A$  for the transistors to be in saturation since:

$$\begin{aligned} \text{For diode connected resistor, } g_{m_B} &= \frac{W}{L} K (V_{dd} - V_{out} - V_t) \\ &= \frac{.15}{.13} \mu (620\mu) (1.2 - 0.382 - 0.3) \\ &= 0.37 \text{ mS} < 1 \text{ mS} \\ \therefore r_{mB} &\geq 1k \end{aligned}$$

$$V_{dd} - I_d (r_{mB}) = V_{out}$$

$$I_d = \frac{V_{dd} - V_{out}}{r_{mB}}$$

$$\approx 300\mu A$$

$$\frac{1}{2} \left(\frac{W}{L}\right) K (V_{in} - V_t)^2 \leq 300\mu A$$

$$\left(\frac{W}{L}\right) \leq 143$$

Setting L to be the minimum  $0.13\mu m$ , I choose  $W = 6\mu$ , for the common source transistor, giving a stage gain of about  $\sqrt{40}$ . This means I need about 4 gain stages to achieve a gain of 1600, with the expectation that roughly half the gain has to be traded off in later stages to support the load of  $50\text{ohms}$ .

$$\frac{W_A}{W_B} = \sqrt{\frac{6\mu}{.15\mu}} = \sqrt{40}$$

$$A = (\sqrt{40})^4 = 1600$$

In addition, I set  $V_{out} = V_{in}$  for each stage so that I need not worry about the biasing points for transistors in the cascade. I calculated the  $V_{in}$  required to be:

$$\begin{aligned}
 I_{ds} &= \frac{1}{2} \left( \frac{W}{L} \right)_1 (V_{in} - V_t)^2 = \frac{1}{2} \left( \frac{W}{L} \right)_2 (V_{dd} - V_{out} - V_t)^2 \\
 &= \frac{1}{15} (V_{in} - 0.3)^2 = \frac{15}{18} (0.9 - V_{in})^2 \\
 \sqrt{40} (V_{in} - 0.3) &= 1.07 (0.9 - V_{in}) \\
 V_{in} &= \underline{0.382V}
 \end{aligned}$$

From previous calculations, I need the DC input level for the final CD stage to be about 1.1V, hence I would need to step up the output level <sup>of the previous stage</sup> achieved this using a CS stage with a resistor. Choosing the same dimensions as my other common source transistors out of convenience, the current is about 96uA from:

$$(W/2L)K(V_{gs} - V_t)^2 = (6u/26u) (620u) (0.082)^2 = 96uA$$

With this current, I need a resistor with about  $.1V / 96uA \approx 1000k\Omega$  to shift the DC level to 1.1V. All transistors except for that in the common drain stage (stage 6) have their bulk tied to the source to eliminate body effects since they contribute very little to the FOM and the complexity of having to deal with the body effect is unjustified.

Stage 5 is used primarily to shift the DC output level of stage 4 to match the input DC level of stage 6 using a small resistor at the expense of some gain. I could have used a PMOS stage instead but since the addition of more CS stages is relatively cheap, I avoided the unnecessary trouble of having to calculate the PMOS parameters.

## Device Vdsat and Ids calculations

**Table 2: Parameters for transistors**

	W	L	Vdsat		Ids	
			Measured	Calculated	Measured	Calculated
M1	6u	.13u	85.7mV	82mV	88uA	96uA
M2	6u	.13u	85.75mV	82mV	88uA	96uA
M3	6u	.13u	85.46mV	82mV	87.5uA	96uA
M4	6u	.13u	87mV	82mV	90.6uA	96uA
M1b	.15u	.13u	514mV	518mV	88uA	96uA
M2b	.15u	.13u	514mV	518mV	88uA	96uA
M3b	.15u	.13u	517mV	518mV	87.5uA	96uA
M4b	.15u	.13u	579mV	518mV	90.6uA	96uA
M5	6u	.13u	78mV	82mV	87.7uA	96uA
M6	46.8u	.13u	365mV	300mV	10mA	10mA

For M1, M2, M3, M4, M5,

$$\begin{aligned} V_{dsat} &= V_{gs} - V_t \\ &= .382V - .3V \\ &= \underline{82mV} \end{aligned}$$

For M1b, M2b, M3b, M4b,

$$\begin{aligned} V_{dsat} &= V_{dd} - out - .3V \\ &= 1.2V - .382V - .3V \\ &= \underline{518mV} \end{aligned}$$

For M6,

$$\begin{aligned} V_{dsat} &= out5 - V_{out} - V_t \\ &= 1.1V - .5V - .3V \\ &= \underline{.3V} \end{aligned}$$

The results for the later stages do not match up with the calculations as well because I realized, after running through Spice, that the gain was about 800, so I reduced W/L for stage 6 and the resistance for stage 5, pushing the DC bias level for the last stage to 1.165V rather than 1.1V in my calculations.

**Table 3: Parameters for Resistors**

	W	L	R
R5	.78u	.5u	390 $\Omega$

**Simulation Results**

	Specifications	Simulated	Calculated
Vin	.35 - .85V	.3857V	.382V
Vout	.5 - .7V	.5V	.5V
Av	>500	502	<u>562</u>

$$A_v = (1 + \beta) \cdot (g_{m_s} R_{out_s}) \left( \frac{g_{m_s} R_s}{(1 + \beta) g_{m_s} R_s + 1} \right)$$

$$f_{os} = 1600 \left( 2.35 \text{ms} \left( \frac{390}{1000} \right) \right) \left( \frac{81.5 \text{m} \times 50}{(1 + 0.095) 81.5 \text{m} \times 50 + 1} \right)$$

$$= \underline{562}$$

$\therefore$  The calculations using  $\mu$  level 1 equations matches the simulation very well.

$$f = \frac{\tau}{2(2\beta_e + V_{be})^{1/2}}$$

$$= \frac{0.2}{2(2(0.3) + .5)^{1/2}}$$

$$= \underline{0.095}$$

$$g_{m_s} = \left( \frac{W}{L} \right)_s K (0.382 - 0.3)$$

$$= \underline{2.35 \text{mS}}$$

$$g_{m_s} = \left( \frac{W}{L} \right)_s K (V_d - V_{out} - V_t)$$

$$= \frac{46.8 \mu}{13 \mu} (620 \mu) (1.165 - 0.5 - 0.3)$$

$$= \underline{81.5 \text{mS}}$$

$$\text{Total Area} = 2[(6\mu \cdot 13\mu) \cdot 5 + (.15\mu \cdot 13\mu) \cdot 4] + 46.8\mu \cdot 13\mu + .78\mu \cdot .5\mu$$

$$= \underline{6.92 \times 10^{-11} \text{m}^2} \quad 14.43 (\mu\text{m})^2$$

$$\text{Total Power Consumption} = \underline{7.5 \text{mW}} [1.4 \times 8\mu + 87.5\mu \times 2 + 89.7\mu + 90.6\mu \times 2] \times 1.2\text{V} = 10.95 \text{mW}$$

$$\text{FOM} = \frac{2[(6\mu \cdot 13\mu \cdot 5 \cdot 85 \text{mV} \cdot 88\mu\text{A}) + (.15\mu \cdot 13\mu \cdot 4 \cdot 514 \text{mV} \cdot 88\mu\text{A}) + 46.8\mu \cdot 13\mu \cdot 365 \text{mV} \cdot 10 \text{mA}]}{2.2 \times 10^{-14} \text{Wm}^2}$$

$$= \frac{14.43 \times 10.95 \text{m}}{2.2 \times 10^{-14}} = \boxed{0.187}$$

Conclusion

In the design of this amplifier, the challenge was to support the  $50\Omega$  load at an output dc level of  $0.5\text{V}$ . The dominance of the FOM associated with this stage was critical in many of the design choices. For example, operating at strong inversion allowed the level 1 equations to model the amplifier more accurately. After meeting the specifications, I iteratively fine tuned some parameters associated with the dominant stage to reduce the overall FOM.

Comment

I noticed that if the specifications allowed for  $V_{\text{dd}} = 0.6\text{V}$  and  $V_{\text{ss}} = -0.6\text{V}$ , the biasing of the out at DC level could be zero (ground) allowing for a much smaller transistor for the common drain output stage, with an expected reduction in the FOM by at least 2 orders of magnitude since the current could be much smaller and  $\frac{W}{L}$  could correspondingly be reduced.