

EE140 Design problem 1 guidelines

1 Report guidelines

Your project report should include the following sections:

- Discussion of your topology choice: explain why you chose a certain topology and compare your topology with possible alternatives.
- Discussion of your FOM minimization strategy: explain how you chose all the W 's, L 's, V_{dsat} 's and currents; show your calculations.
- A schematic (drawn by hand) of your circuit, annotated with all the node voltages.
- Provide a table with W , L , V_{dsat} and I_{ds} for every transistor. For V_{dsat} and I_{ds} , include both the calculated and the simulated values.
- Provide a table with W , L and R for every resistor.
- Make a table with the simulation results from test benches and compare it with design specifications. Explain differences with your hand calculations.
- List FOM and the total area, the power consumption of your design.
- Comments and conclusion.

DO NOT INCLUDE SPICE NETLIST IN THE PROJECT REPORT.

2 Circuit submission guidelines

Send an email to ee140@cory.eecs.berkeley.edu with your name in the subject and your circuit in the body of the email. Make sure to send the email in plain text, not in html.

The body of the email should be the same as the file used to run the test bench:

```
.param VIC = < your midpoint of the common mode input range >  
.subckt amplifier in out vdd vss  
< your circuit >  
.ends
```

The subcircuit should be named 'amplifier' and the order of the input nodes should be: positive input node, output node, positive supply, negative supply. You can change the names of the nodes.