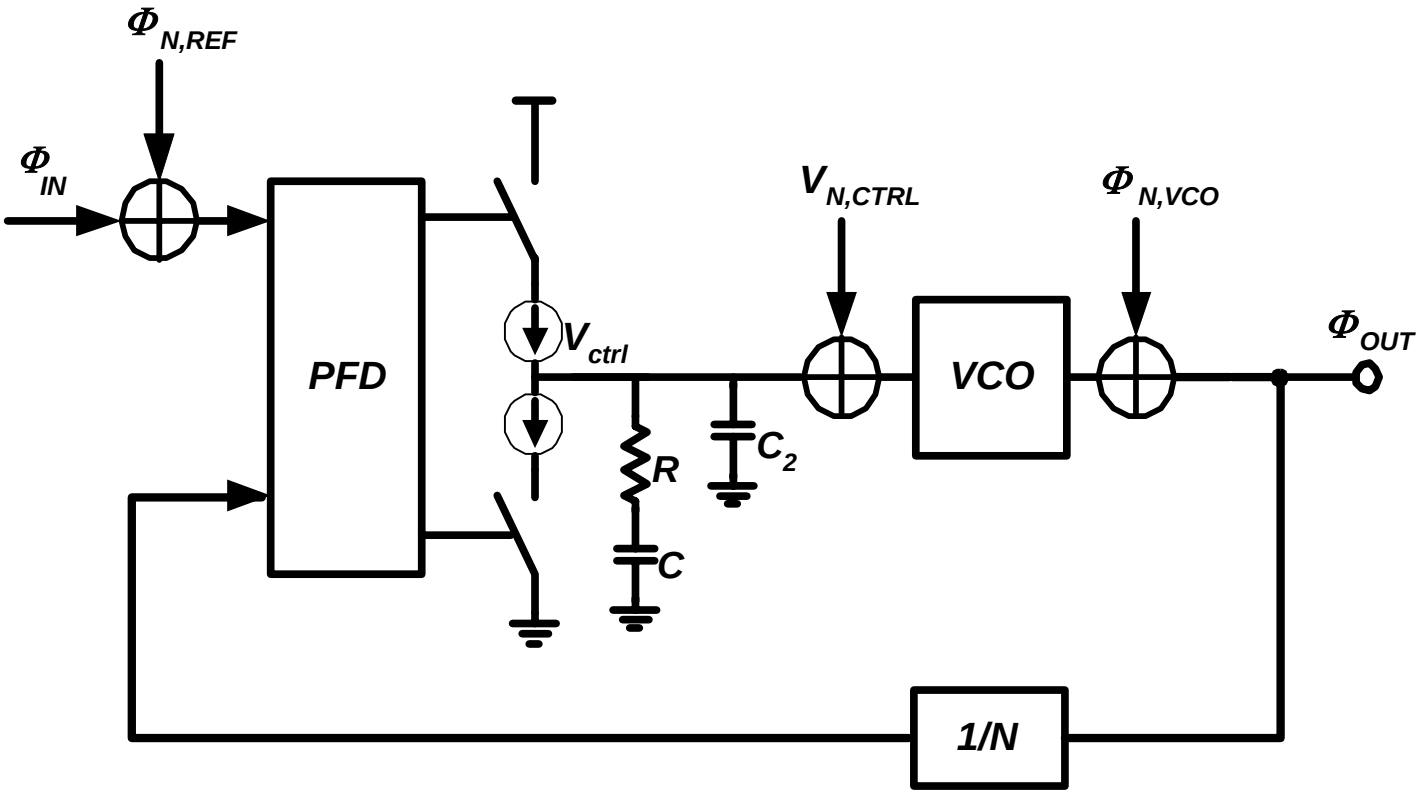
EE290C High-Speed Electrical Interfaces **Spring 2004.**

HOMEWORK 2. **Due: Thursday, March 11, 2004 at 5pm in 558 Cory**

This is an individual assignment!

Problem 1:



A third-order charge-pump PLL is shown in the above figure along with noise sources corresponding to the input reference clock, control node and VCO.
The VCO gain is K_{VCO} (Hz/V) and the charge-pump current is I_{CH} (A).

a) Find the noise transfer function from the various noise sources to the output of the PLL.
b) Find the maximum achievable gain margin for this PLL and the unity-gain frequency for which it is achieved, assuming that the loop filter parameters R, C, C_2 are set.

Problem 2:

Read the paper:
J. Maneatis, "Low-Jitter Process-Independent DLL and PLL Based on Self-Biased Techniques", *IEEE J. Solid-State Circuits*, vol. 31, no. 11, pp. 1723-32, Nov. 1996.

a) Plot the I-V characteristics for V_{CTRL} values of 1V and 1.2V of the symmetric load in Fig. 5, using HSPICE. The definition of V_{CTRL} is as in Fig. 5. Let the PMOS devices be (0.25/0.18) μm. Use the 1.8V, 0.18 μm class technology.
b) In the 1.8V, 0.18μm class technology, design a 9-stage ring oscillator at 1 GHz with voltage swing of 1.2V using the differential buffer delay stage of Fig. 1. Adjust the V_{BP}, V_{BN} bias voltages accordingly (do not design a bias circuit). Use minimum length transistors. You may add additional capacitance at the nodes of the ring oscillator to achieve the specified frequency.
c) What is the sensitivity of the delay to changes in the supply voltage for this element? Compare it to a symmetrically sized CMOS inverter with same delay. Use HSPICE.
d) Describe the operation of the replica-feedback bias circuit of Fig. 2.