

## CLASS PROJECT.

Assigned: March 15, 2004

**Overview**

Your task is to design a serial high-speed electrical link backplane system. The target data rate is 6.25Gb/s over a 20-inch FR4 backplane and two 3-inch daughter cards. The system is plesiochronous, with a separate clock crystal source on each card.

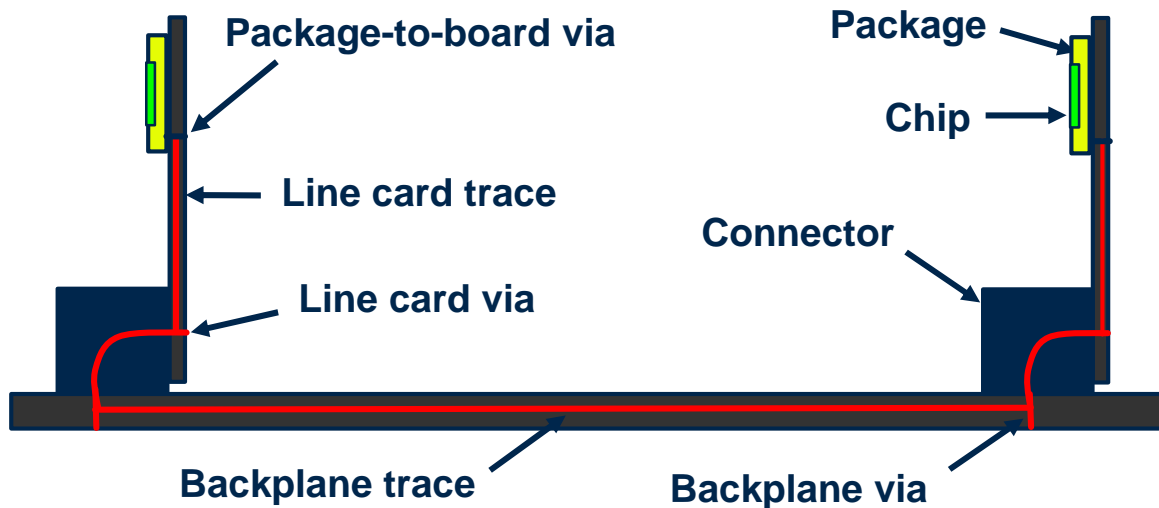


Figure 1: Sketch of a link.

The task of your group is, in the first phase, to develop the concept of a system that will achieve this data rate, and, in the second phase, to implement it as multiple blocks in Spice.

At a minimum you must get the basic through channel to operate reliably at 6.25Gb/s. Extra credit will be given if you can achieve reliable operation at an even higher rate. A SPICE model of the worst trace of this backplane is available on the course web page. It consists of a set of files that describe a baseline channel.

M20.spi is the top-level file and has a simple current mode piece-wise linear source which will generate a step response that is then propagated through the signal path. The signal path is made up of W-element models for the different components as shown in Figure 1 above. The output is the measured parameter vq1. The models include the chip pin parasitics, the models of the vias, connectors, package, etc... Right now the pin parasitics are only approximate; in your final report you will have a circuit design for the transmitter and receiver and use the parasitics from these to regenerate your system margins.

The baseline m20.spi channel consists of a 20" FR4 backplane trace, middle layer of a 300mil thick backplane, and two 3" FR4 cards with 2 high-speed connectors. In addition to designing for operation in this case you need to modify the deck to simulate also:

- Top and bottom layers at 20" (longest backplane trace)
- Top and bottom layers at 1.5" (shortest backplane trace)

Your design needs to be able to operate in all conditions. Extra credit will be given for operation in systems where boards are manufactured with +/- 10% impedance variations.

## Task

Your task is to perform the system-level electrical design for the link that is to operate over the existing backplane. The project is done in groups of 4-5 students. Specifically, you should address:

1. **Signaling convention:** How symbols are encoded into voltage or current, how the line is driven, terminated, and received.
2. **Timing convention:** How events are discriminated in your system, how clocks are distributed, recovered, and/or generated.
3. **Specification of Driver, Receiver, and Timing Circuits:** As part of your signaling and timing conventions describe at a high level how these circuits operate. You will also need to develop a high level model of the driver circuits to complete your Matlab simulation. (No transistor level design is required in the first phase).

To validate and evaluate your design you must perform the following analyses on it:

1. **Noise Budget:** Calculate all contributions to noise and interference, compute the net voltage noise margin. (Assume there is a 5mV Gaussian noise source on each backplane signal). In the second phase you will estimate the BER.
2. **Timing Budget:** Calculate all contributions to timing uncertainty and compute the net timing margin.
3. **SPICE Simulation of Channel:** Build an accurate SPICE model of your channel including the driver, thru channel (provided), and receiver. Characterize this line with a simulated TDR and TDT response. Simulate your timing and signaling conventions on this channel using a short pseudo-random sequence and an isolated "1" and "0" to generate an eye diagram. Compare the simulated eye opening with your computed voltage and timing margins. Simulate the frequency response of your lines giving S11 and S12 parameter.

### Building Blocks:

In your system level simulation, you are supposed to specify the characteristics of your basic building blocks. Please keep in mind that in the second phase, you will be supposed to design these blocks, so the more relaxed the specifications are, you will have an easier job in the second phase. We are specifying some hard constraints on these parameters.

1. Crystal oscillators – you can choose any frequency between 1MHz and 300MHz, with 20ppm accuracy.

2. Current-mode drivers with drive of up to 20mA and rise/fall time as low as 50ps. Drive current will be within 5% of the specified value.
3. Voltage-mode drivers with an output impedance as low as 10-Ohms and the swing between two power rails. Voltage accuracy is set by noise on the power supplies. Rise/fall times may be as low as 50ps. Actual output impedance is within +/-20% of the specified value.
4. Controlled-output-impedance driver: This cell is a voltage driver cell with paralleled output driver transistor pairs. By setting an associated control register you can turn off one or more of the pairs to adjust the output resistance of the driver in 5% increments. Swing and supply tolerances are as in the voltage-mode driver. If you use this type of driver you must include a method for determining the actual output impedance presented by the drivers on each chip and setting it to match your system requirements. Process variations are assumed to give you a +/- 50% chip to chip variation in resistance from nominal for a given register setting in production parts. Within a single chip variation in resistance for a given register setting is less than 2%.
5. On-chip termination resistors matched to within 20% of a value you specify.
6. Programmable termination resistor: Like the controlled-output-impedance driver this is a programmable resistor constructed from a parallel combination of transistors. Setting a control register allows you to control the impedance of the resistor in 5% increments. If you use this resistor, you must include a method for setting it. As with the drivers, process variations will give a +/- 50% chip to chip variation in resistance from nominal for a given register setting in production parts. Within a single chip variation in resistance for a given register setting is less than 2%.
7. Clocked receivers (differential) with a sensitivity of 10mV, a maximum offset of +/-40mV, and an aperture time of 20ps. You can reduce the offset using an offset calibration method if you describe in your report how this is accomplished. Input capacitance is 100fF per receiver.
8. Unlocked receivers (differential) with a gain-bandwidth product of 30GHz (you decide how to trade between gain and bandwidth) and a maximum offset of +/-40mV. As with the clocked receivers you may use offset calibration to reduce this offset if you describe how to accomplish it. Input capacitance is 100fF per receiver.
9. Delay lines with arbitrary programmable delay and jitter equal to 5% of the overall delay. The delay of the line may be controlled either digitally or via a control voltage.
10. On-chip VCOs with center frequency between 100MHz and 5GHz, a tuning range of up to 5:1, and jitter of 10% of the cycle time.
11. Phase comparators with +/-10ps phase offset.

12. Charge pumps and loop filters as described in the class. Assume they are ideal, with 1% matching between the UP and DOWN currents.

13. Flip-flops with a regeneration time constant of 100ps and a delay of 500ps.

14. Arbitrary combinational and sequential logic modules. Assume a fan-out of 4 inverter delay is 50ps.

If you need a module that is not on this list, or if you would like to change the specification of a module, please discuss it with the instructors.

**Grading:**

Your project (phase 1) will be graded according to the following criteria:

1. Completeness of the design (30%)
2. Robustness of design (20%)
3. Creativity and elegance of design (10%)
4. Completeness of analysis (20%)
5. Clarity of the report (20%)