

D. Markovic

TuTh 11-12:30

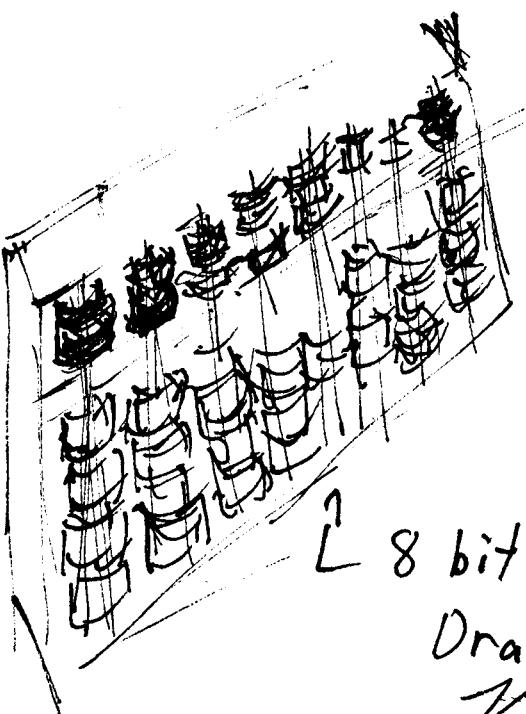
Thursday, November 10, 6:30-8:00pm

EECS 141: FALL 2005—MIDTERM 2

Midterm Solutions

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| NAME | Last | First |
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| SID | |
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8 bit adder

Drawn by
Ke. Zi

- Problem 1 (8):
- Problem 2 (16):
- Problem 3 (11):
- Problem 4 (5):

| | |
|-------------------|--|
| Total (40) | |
|-------------------|--|

PROBLEM 1: Wires (8pts)

Consider RC network shown in Fig. 1. Assume the transmission gate can be modeled as a resistance R_3 . Capacitance of this gate is included in C_3 .

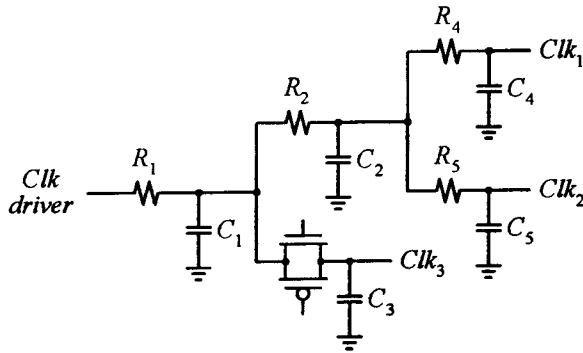


Fig. 1: RC network.

- a. Write expressions for the time constants associated with Clk_1 , Clk_2 , and Clk_3 . (6 pts)

+ 2

$$\tau_1 = R_1 C_1 + (R_1 + R_2) C_2 + R_1 C_3 + (R_1 + R_2 + R_4) C_4 + (R_1 + R_2) C_5$$

+ 2

$$\tau_2 = R_1 C_1 + (R_1 + R_2) C_2 + R_1 C_4 + (R_1 + R_2) C_5$$

+ 2

$$\tau_3 = R_1 C_1 + (R_1 + R_2) C_3 + R_1 C_2 + R_1 C_4 + R_1 C_5$$

- b. If $R_1 = R_2 = R_4 = R_5 = R$, $C_1 = C_2 = C_3 = C_4 = C_5 = C$, what value of R_3 (in terms of R) is required to balance the delays to Clk_1 , Clk_2 , and Clk_3 ? (2 pts)

$$+1 \quad \tau_2 = \tau_1 = 9RC$$

$$+1 \quad 9RC = \tau_3 = 5RC + R_3 C$$

$$R_3 = 4R$$

$$R_3 = 4R$$

PROBLEM 2: Logic Gates (16 pts)

Consider dynamic gate shown in Fig. 2. Assume $C_{gs} = C_{gd} = C_{db} = C_{sb} = S * 1\text{fF}$, where S is the size of the transistor as indicated in the schematic. The input capacitance of the inverter is 20 fF.

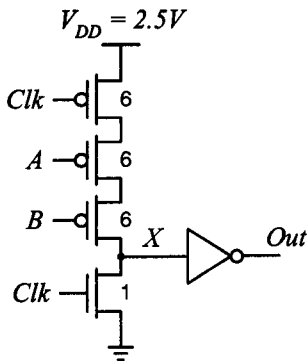


Fig. 2: Dynamic gate.

- a. Is it the best to make V_M of the inverter equal to $V_{DD}/2$, greater than $V_{DD}/2$, or less than $V_{DD}/2$? (3 pts)

Circle one answer:

$V_M = V_{DD}/2$

$V_M > V_{DD}/2$

$V_M < V_{DD}/2$ (2) pt.

Briefly explain your answer below:

faster pull-down at the output of inverter (1) pt.

- b. What are the logic levels of inputs A and B that create worst-case charge sharing scenario during evaluation phase? Circle one answer: (1 pt)

$A = B = 0$

$A = 0, B = 1$

$A = 1, B = 0$

$A = B = 1$ (1) pt.

What is the worst voltage level at node X resulting from charge sharing effects? (4 pts)

$V_{out} (V) = 1.034$

$C_x = 6(C_{gd} + C_{dB}) + (C_{gd} + C_{dB}) + 20 = 34\text{f}$ (2) pt.

$C_y = 6(C_{gs} + C_{sB}) + 6(C_{gd} + C_{dB}) = 24\text{f}$ (1) pt.

$V_x = V_{dd} \cdot \frac{C_y}{C_x + C_y} = 2.5 \times \frac{24}{58} = 1.034$ (1) pt.

- c. In addition to charge sharing, assume each transistor connected contributes $S \cdot 1nA$ of reverse biased diode current. Assume V_M of the inverter is $V_{DD}/2$. For how long will the output be valid in the evaluation phase? (4 pts)

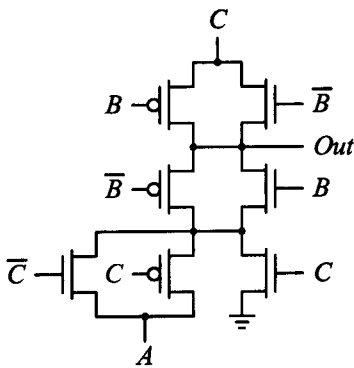
+ 2 pts - 0.5 for each diode (x3)
0.5 for signs

$$T_{valid} = 1.14 \mu S$$

+ 1 pt - $|\Delta V| = \frac{V_{dd}}{2} - 1.034 = 0.216$

+ 1 pt - $Q = (C_x + C_y)\Delta V = I_r \cdot t$

- d. Write Boolean expression that describes logic function of the gate below. (2 pts)

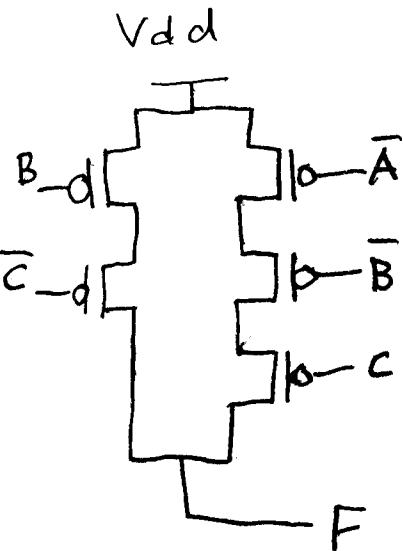


$$Out = \bar{B} \cdot C + A \bar{B} \bar{C}$$

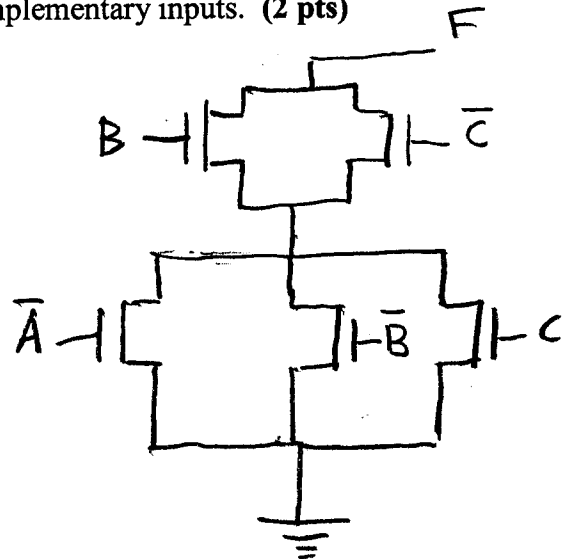
1 pt for each term.

Fig. 2d: Logic gate.

- e. Implement gate from part (d) in static complementary CMOS using **minimum number of transistors**. You may assume both true and complementary inputs. (2 pts)



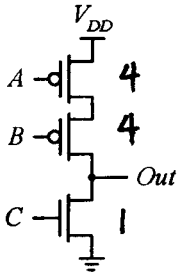
+ 1 PUN
+ 1 PDN



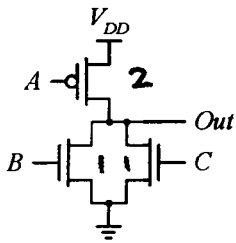
PROBLEM 3: Logical Effort (11)

For logical effort calculation, assume that the PMOS/NMOS width ratio in the unit inverter is 2/1.

- a. Determine the logical effort of inputs A, B, and C for the gates shown below. Also, determine the parasitic delay of each gate. (5 pts)



| | |
|--------------|-----------|
| $LE_A = 4/3$ | (0.5 pts) |
| $LE_B = 4/3$ | (0.5 pts) |
| $LE_C = 1/3$ | (0.5 pts) |
| $P = 5/3$ | (1 pt.) |



| | |
|--------------|-----------|
| $LE_A = 2/3$ | (0.5 pts) |
| $LE_B = 1/3$ | (0.5 pts) |
| $LE_C = 1/3$ | (0.5 pts) |
| $P = 4/3$ | (1 pt.) |

- b. Sizes the transistors in Fig. 3b so that the circuit provides the same pull-up and pull-down current at the output *Out* as a unit inverter. The input capacitance of all inputs (*A*, *B*, and *C*) should be equal. (6 pts)

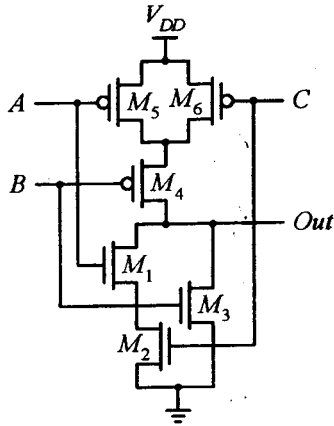


Fig. 3b: Complex logic gate.

| | |
|-----------------|--------------------|
| Pull-up: | $M_4 = 4.5$ (1pt.) |
| | $M_5 = 3.5$ (1pt.) |
| | $M_6 = 3.5$ (1pt.) |

| | |
|-------------------|------------------|
| Pull-down: | $M_1 = 2$ (1pt.) |
| | $M_2 = 2$ (1pt.) |
| | $M_3 = 1$ (1pt.) |

For the pull-down network:

$$M_3 = 1$$

$$\frac{1}{M_1} + \frac{1}{M_2} = 1 \quad (1)$$

note that inputs *A* and *C* are identical

$$\therefore M_1 = M_2 \text{ and } M_5 = M_6 \quad (2)$$

combining (1) and (2):

$$M_1 = M_2 = 2$$

For the pull-up network:

$$\frac{1}{M_4} + \frac{1}{M_5} = \frac{1}{2} \quad (3) \quad \leftarrow \text{same PD as inverter}$$

$$M_4 + M_3 = M_5 + M_1 \quad (4) \quad \leftarrow \text{same input caps}$$

$$M_4 + 1 = M_5 + 2 \quad (5)$$

$$M_4 - 1 = M_5$$

Solving (3) and (5) for M_4 and M_5 :

$$M_4 = \frac{5 + \sqrt{17}}{2} \approx 4.5$$

$$M_5 = M_4 - 1$$

$$M_5 \approx 3.5 = M_6$$

PROBLEM 4: Arithmetic Blocks (5 pts)

16-bit ($N = 16$) Carry Skip Adder is shown in Fig. 4. It is organized in blocks of $B = 4$ bits. For simplicity, assume $t_{carry} = t_{sum} = t_{skip}$. You may ignore t_{setup} .

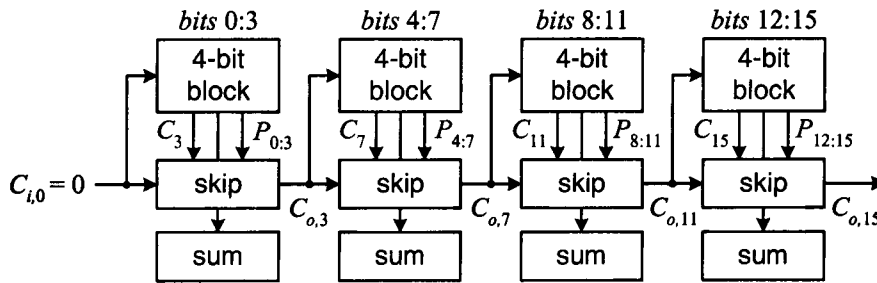
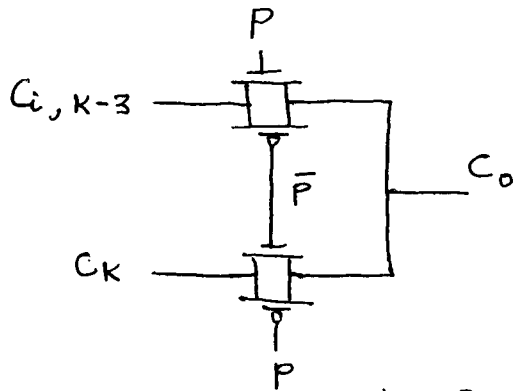
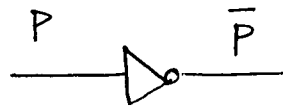


Fig. 4: Adder.

a. Implement the skip function using transmission gates and inverters. (2 pts)



$k = 3, 7, 11, 15$



inverter (0.5) pt
inputs (0.5) pt
gate (1) pt

b. What is the optimal block size B that minimizes the delay of the adder? B does not have to be an integer. (3 pts)

$$B = 2\sqrt{2}$$

$$t_d = B t_{carry} + \left(\frac{N}{B} - 1\right) t_{skip} + (B - 1) t_{carry} + t_{sum} \quad (2) \text{ pt.}$$

Set the derivative to 0.

$$0 = t \left(2 - \frac{N}{B^2} \right)$$

$$0 = 2 - \frac{N}{B^2}$$

$$B = \sqrt{\frac{N}{2}} = 2\sqrt{2} \quad (1) \text{ pt.}$$

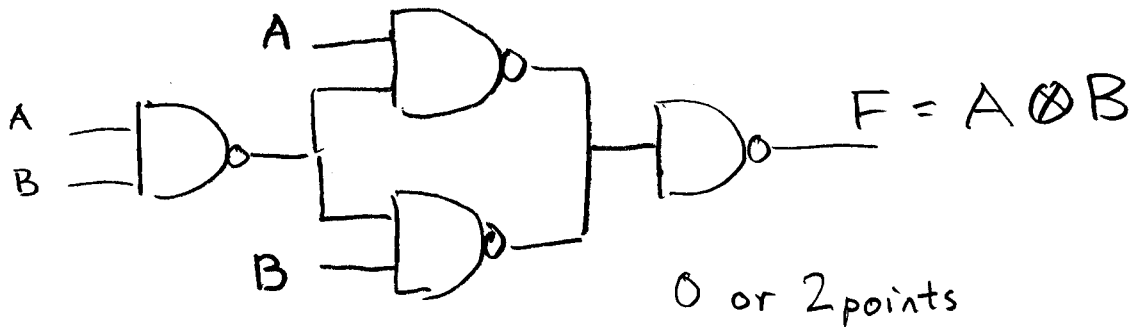
Bonus - no partial credit

PROBLEM 5: Extra Credit (5 pts)

Being expert digital IC designers, we know the fact that any logical function can be implemented using 2-input NAND gates only or 2-input NOR gates only.

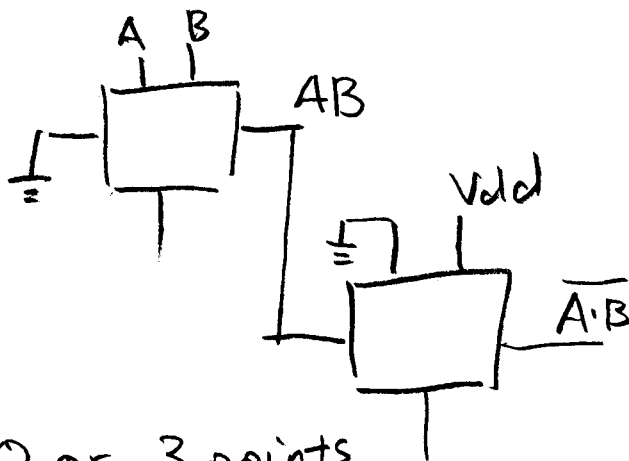
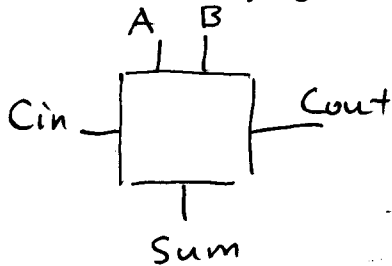
- a. Design a 2-input XOR gate using only 2-input NAND gates. Use the fewest number of gates possible. (2 pts)

4 gates



- b. (standard interview question):

Prove any logic function can be implemented using full adder cells. (3 pts)



| A | B | Cin | Cout | Sum |
|---|---|-----|------|-----|
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 |
| 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 0 | 0 |

Cout
AB
if
Cin =

if $A=0, B=1$
Sum = \overline{Cin}

0 or 3 points