

UNIVERSITY OF CALIFORNIA
College of Engineering
Department of Electrical Engineering and Computer Sciences
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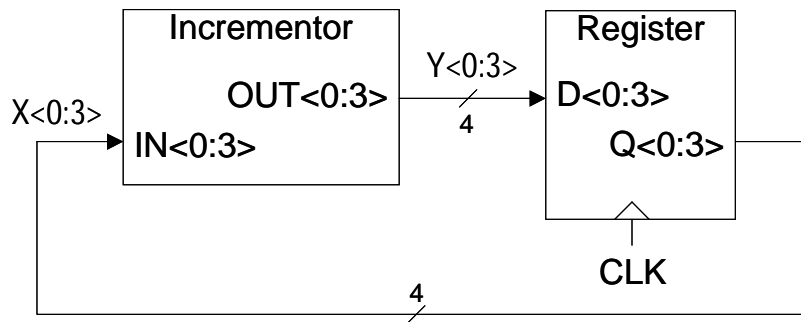
Dejan Markovic

Homework #8
 Due Friday, November 18, 5pm

EECS141

Problem 1 – Activity Factor

Consider the decimal counter shown below. The static logic block is a 4-bit binary incrementor. Its input is a 4-bit binary number $IN\langle 3:0 \rangle$, where $IN\langle 3 \rangle$ represents the most significant bit of the input number. Its output is a 4-bit binary number $OUT\langle 3:0 \rangle$ that has a numeric value 1 greater than, unless the input is 9, in which case the output is 0. I.e., if the input is 5 (0101), the output will be 6 (0110). If the input is 9 (1001), the output is (0000).



a) What are p_0 and p_1 , the probabilities of a 0 and of a 1, for each of the four bits $X\langle 0 \rangle$ through $X\langle 3 \rangle$?

Soln:

$X\langle 0 \rangle$: $p_1 = \text{Prob}(X = 1, 3, 5, 7, \text{ or } 9) = 0.5$ (5 out of 10 cases), $p_0 = 0.5$

$X\langle 1 \rangle$: $p_1 = \text{Prob}(X = 2, 3, 6, \text{ or } 7) = 0.4$, $p_0 = 0.6$

$X\langle 2 \rangle$: $p_1 = \text{Prob}(X = 4, 5, 6, \text{ or } 7) = 0.4$, $p_0 = 0.6$

$X\langle 3 \rangle$: $p_1 = \text{Prob}(X = 8 \text{ or } 9) = 0.2$, $p_0 = 0.8$

b) What are the activity factors α_0 through α_3 for each of the four bits $X\langle 0 \rangle$ through $X\langle 3 \rangle$?

Soln: Cannot use $p_0 \cdot p_1$ here because successive logic values are correlated with each other. Note that X follows the repeating pattern 0, 1, 2, ..., 9, 0, 1, ... and look at the soln's to the previous part to count how many transistions there are for each bit in one cycle.

$X\langle 0 \rangle$: $0 \rightarrow 1$ occurs every other cycle, $\alpha_0 = 0.5$

$X\langle 1 \rangle$: $0 \rightarrow 1$ occurs when X changes from 2-3, and from 5-6, or 2 times every 10 cycles, $\alpha_1 = 0.2$

$X\langle 2 \rangle$: $0 \rightarrow 1$ occurs when X changes from 3-4, or once every 10 cycles, $\alpha_2 = 0.1$

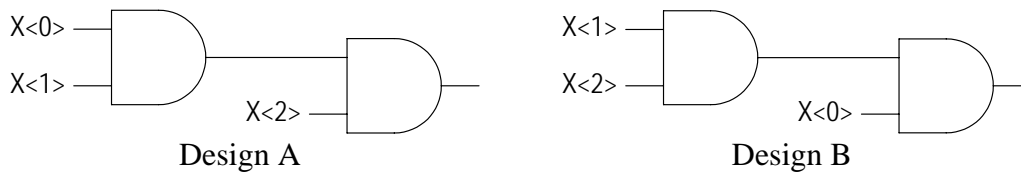
$X<3>: 0 \rightarrow 1$ occurs when X changes from 7-8, or once every 10 cycles, $\alpha_3 = 0.1$

c) If the capacitance at each node for X is 5 fF, the capacitance at each node for Y is 4 fF, and the circuit is clocked at 250 MHz, what is the dynamic power consumption of this circuit? Ignore all other capacitances, assume there is no glitching, and $V_{DD} = 2.5$ V.

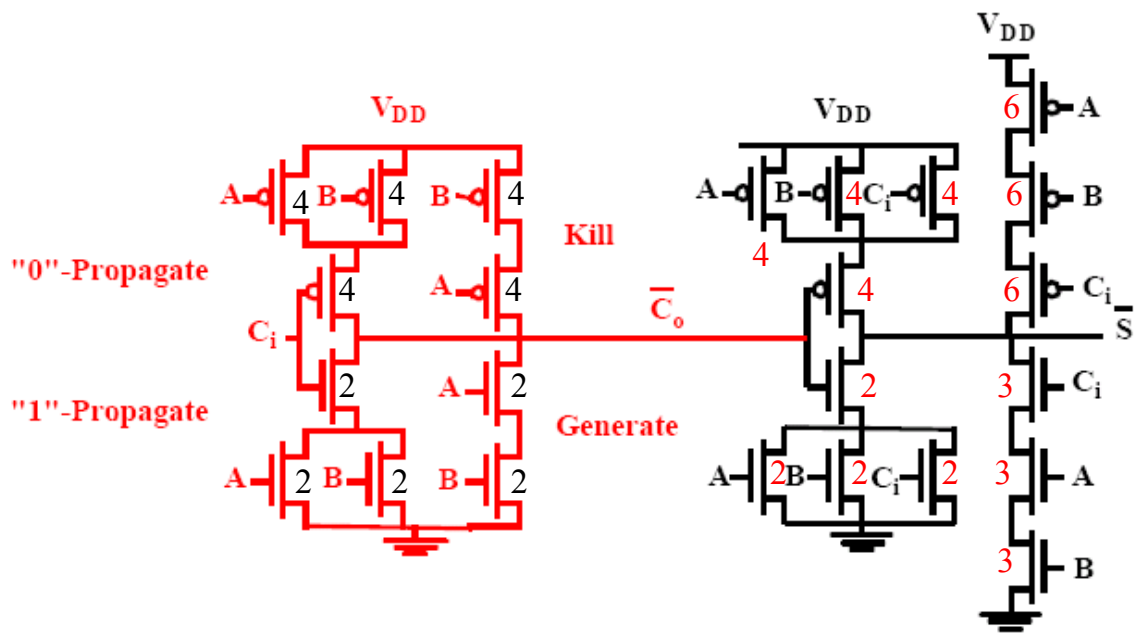
Soln: Note that X and Y nodes go through all of the same transitions, so just count their capacitances together.

$$P = f \cdot \sum C V_{DD}^2 \alpha_i = 250 \text{ MHz} \cdot 9 \text{ fF} \cdot 6.25 \text{ V}^2 \cdot (0.5 + 0.2 + 0.1 + 0.1) = 12.7 \text{ } \mu\text{W}$$

d) In addition to the incrementor logic, you wish to add logic that detects when $X<3:0>$ has a value 7. Recognizing that $X<3:0>$ is never 15, this can be accomplished with a 3-input AND of bits $<0>$ through $<2>$. If this is to be accomplished with only 2-input AND gates, which of the two choices below is preferable? Why?



Soln: Design B is better because it consumes less dynamic power. Note that the intermediate node in A is 1 when $X = 3$ or 7, and thus has an activity factor of 0.2 (2 $0 \rightarrow 1$ transitions every 10 cycles). The intermediate node in B is 1 when $X = 6$ or 7, thus only has an activity factor of 0.1, leading to less dynamic power consumption. All other nodes have the same activity factors in both designs (assuming no glitching).



Logical effort:

	Carry		Sum
A	12/3	A	15/3
B	12/3	B	15/3
C_i	6/3	C_i	15/3

We can see that the mirror adder has lower logical effort for all inputs except C_i . However we should not forget the extra loading and delay of the additional inverters in the complementary architecture. When those are included the mirror adder wins overall.