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Homework 10

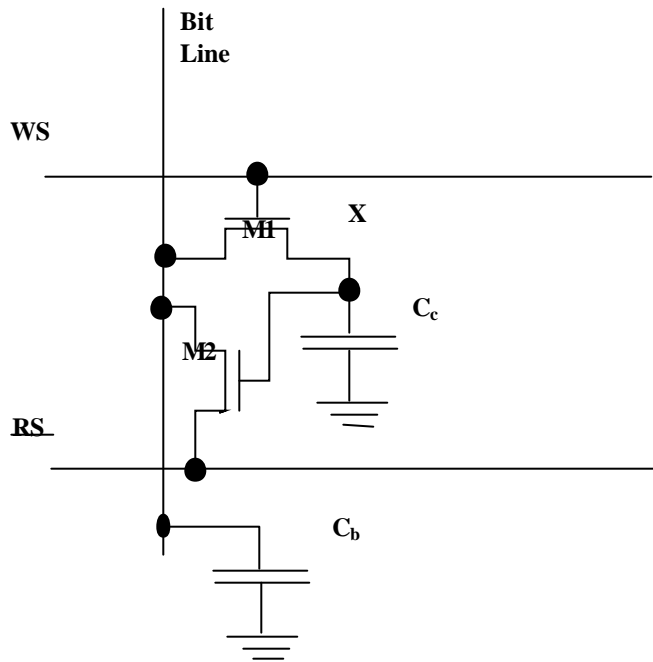
EECS 141

*Never Ever Never Due - for your own practice*

**Problem 1 – 2-T Memory Cell**

The 2-T memory cell shown below uses 2 identical transistors with  $W/L = 0.4/0.25$ . Separate lines are provided for the read select (**RS**) and write select (**WS**) signals, which both switch between 0 and 2.5V. The Bit Line is precharged to  $V_{dd}/2$  prior to a read. A write is done by pulling the bit line either to  $V_{dd}$  or to GND. Ignore the body effect and channel-length modulation. ( $\gamma=0$ ;  $\lambda=0$ ). You may assume that  $k_n' = 115 \mu A/V^2$ ,  $V_{dd}=2.5$ ,  $V_t = 0.4$ .

- Explain the operation of the memory. Draw waveforms for BL, WS, and RS and  $V_x$  for reads and writes of both '1's and '0's.
- Determine maximum current through M2 during a read operation.
- The bit line is connected to a single-ended sense-amp, which switches when the voltage reaches  $V_{dd}/2 \pm 200mV$ . Compute the time required to read a data bit. Assume that  $C_c=10fF$  and  $C_b=2pF$ .



## Problem 2 – DRAM Memory Cell

A 1-T DRAM cell as following consists of a single transistor connected in series with a capacitor. For a read, the bit line is precharged to  $V_{DD}/2$  by a clocked precharge circuit. Then, the access transistor is turned on by applying  $V_{DD}$  to the word line. A write is performed by applying  $V_{DD}$  or GND to the bit line and  $V_{DD}$  to the word line. Assume that  $V_{T0} = 0.4 \text{ V}$ ,  $\gamma = 0.3 \text{ V}^{1/2}$ ,  $|2\phi_F| = 0.6 \text{ V}$

- Find the maximum voltage across the storage capacitor  $C_S$  after writing a 1 into the memory cell (i.e., bit line is driven to  $V_{DD} = 2.5 \text{ V}$ ).
- Ignoring leakage currents, find the voltage on the bit line when this “1” is read from the memory cell.

