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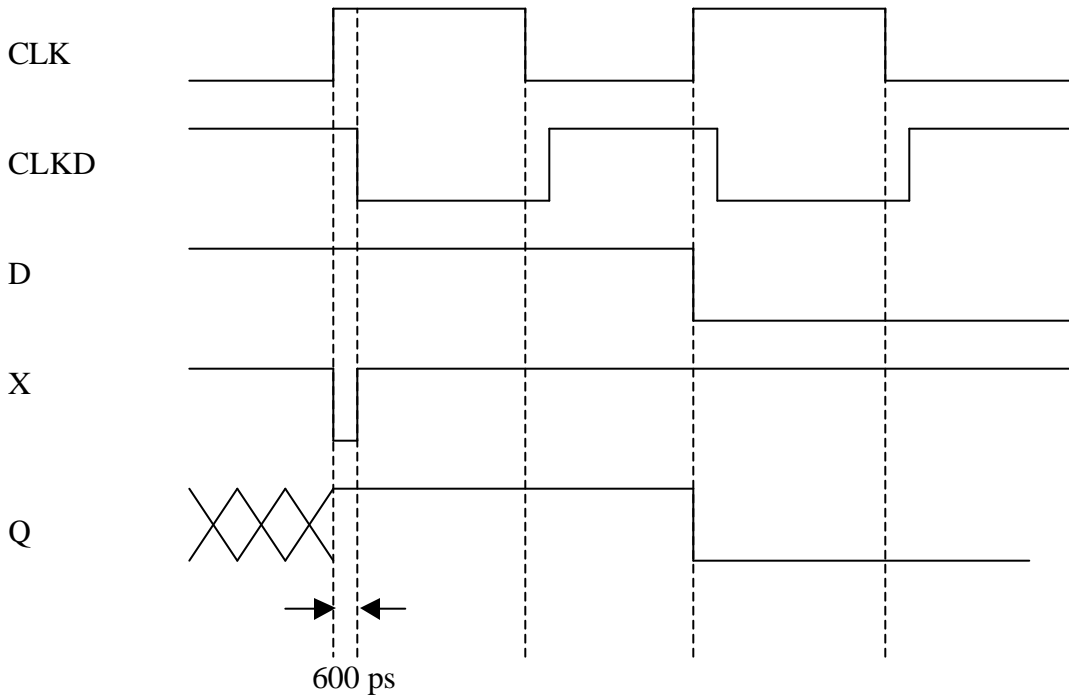
Dejan Markovic

Homework #9 Solutions

EECS 141

Problem 1 – Pulse-triggered latch

a)



b) With respect to clock rising edge,

$$t_{\text{setup}} = 0$$

$$t_{\text{hold}} = 3 t_{p,\text{inv}} = 600\text{ps}$$

c) There is only dynamic power consumption in this circuit.

$$P = CV_{dd}^2 f_{0 \rightarrow 1} = (C_X + C_Q + C_{\bar{Q}})V_{dd}^2 f_{CLK} 0.5a + C_{CLKD} V_{dd}^2 f_{CLK}$$

$$= (10f + 20f + 20f)(2.5)^2(100M) \times 0.5 \times 0.3 + 10f \times (2.5)^2(100M) = 10.9 \text{ mW}$$

$$P = 10.9 \mu\text{W}$$

d) The SPICE input deck and the simulation results are as following:

```
.model pmos pmos LEVEL=1 TOX=25 VTO=-0.7 KP=8e-6 LAMBDA=0.19 PHI=0.6  
.model nmos nmos LEVEL=1 TOX=25 VTO=0.7 KP=20e-6 LAMBDA=0.06 PHI=0.6  
.param wex=0.3
```

```
M1 a in vdd vdd PMOS l=0.25u w=2.5u  
M2 out in a vdd PMOS l=0.25u w=2.5u  
M3 out in b 0 NMOS l=0.25u w=1u  
M4 b in 0 0 NMOS l=0.25u w=1u  
M5 a out 0 vdd PMOS l=0.25u w=`2.5u*wex`  
M6 b out vdd 0 NMOS l=0.25u w=`1u*wex`
```

```
vdd vdd 0 2.5  
vin in 0 pulse 0 2.5 2ns 20ns 20ns 50ns 100ns
```

```
.OPTIONS post=2 nomod
```

```
.tran 1n 200ns  
.end
```

