UNIVERSITY OF CALIFORNIA AT BERKELEY
College of Engineering, Department of EECS

Dejan Markovic

EECS 141
Fall 2005

Project 1 Report for Groups A20 and B20 (max 4 pages)

Name (Last, First)	Student ID	Design Group
Good Report	EE141	A20
Project 1	Fall 2005	

Summary of results from Phase-1

Design	x_1	x_2	x_3	y_1	y_2	y_3
Baseline	1	2	3	2.82	2.82	2.82

D_{min} (t_{p0}) = 18.60	**E_{ref} = 277.39 $C_{gate}V_{dd}^2$**

Summary of results from Phase-2

Design	x_1	x_2	x_3	y_1	y_2	y_3
Optimized	1	1.26	1.51	1.53	1.45	1.27

Delay	D_{min}	$1.1D_{min}$	$1.2D_{min}$	Energy reduction (%)
Sub-design	18.60	20.46	22.32	14.99

Summary of results from Phase-3

D_{min} (ps)	E_{ref} (nJ)	D inc (%)	E red (%)
427.8	**$9.88 \cdot 10^{-3}$**	**9.43**	**19.2**

Scoreboard

Phase-1	
Phase-2	
Phase-3	
Total	

Phase 1: Baseline Design

Summary of results from Phase-1

Design	x_1	x_2	x_3	y_1	y_2	y_3
Baseline	1	2	3	2.82	2.82	2.82

$\mathbf{D_{min}}$ ($\boldsymbol{t_{p0}}$) = 18.60	$\mathbf{E_{ref}}$ = 277.39 $C_{gate}V_{dd}^2$

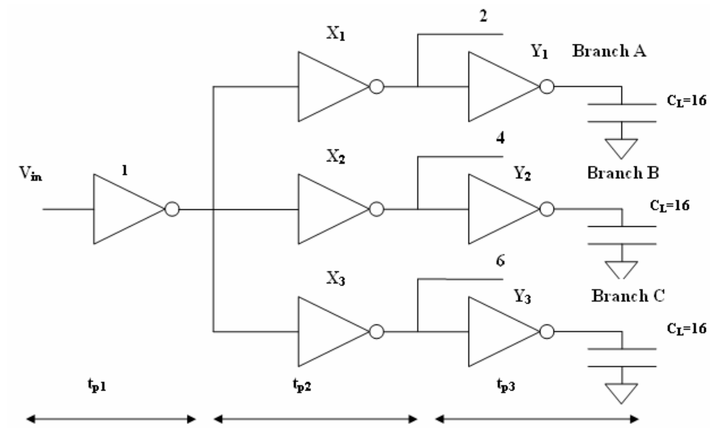
Phase I: Our goal is to minimize the maximum delay of the three branches from V_{in} to the load capacitor, C_L. As we learned from lecture, we want to make the delay through each period (t_{p1}, t_{p2}, and t_{p3}) the same through all three branches. The delay formulas of the three branches are listed as follows (*with the assumption that slope of the input signal is the same as slope of output signal*):

t_{p1} $\qquad$ t_{p2} $\qquad$ t_{p3}

$$D_A = t_{p0}\left[(1+\frac{x_1+x_2+x_3}{1.11}) + (1+\frac{2\cdot y_1}{1.11\cdot x_1}) + (1+\frac{16}{1.11\cdot y_1})\right]$$

$$D_B = t_{p0}\left[(1+\frac{x_1+x_2+x_3}{1.11}) + (1+\frac{4\cdot y_2}{1.11\cdot x_2}) + (1+\frac{16}{1.11\cdot y_2})\right]$$

$$D_C = t_{p0}\left[(1+\frac{x_1+x_2+x_3}{1.11}) + (1+\frac{6\cdot y_3}{1.11\cdot x_3}) + (1+\frac{16}{1.11\cdot y_3})\right]$$



Solving the optimal width:

1. $t_{p3a} = t_{p3b} = t_{p3c}$: $(1+\frac{16}{1.11\cdot y_1}) = (1+\frac{16}{1.11\cdot y_2}) = (1+\frac{16}{1.11\cdot y_3}) \Rightarrow y_1 = y_2 = y_3$

2. $(1+\frac{2\cdot y_1}{1.11\cdot x_1}) = (1+\frac{4\cdot y_2}{1.11\cdot x_2}) = (1+\frac{6\cdot y_3}{1.11\cdot x_3}) \Rightarrow x_1 : x_2 : x_3 = 1:2:3$

3. Since $D_A = D_B = D_C$, $\min(\max(D_A, D_B, D_C)) = \min(D_A)$, so we take the partial derivative of D_A respect to x_1 and y_1. $\frac{\partial D_A}{\partial x_1} = t_{p0}\left[\frac{6}{1.11} + \frac{2\cdot y_1}{1.11\cdot x_1^2}\right] = 0$, $\frac{\partial D_A}{\partial y_1} = t_{p0}\left[\frac{2}{1.11\cdot x_1} + \frac{16}{1.11\cdot y_1^2}\right] = 0$.

Solving the two equations above, we got $x_1 = 0.96um$ and $y_1 = 2.77um$, but we have the constraint that all the widths have to be greater or equal to 1um. We then switched to Microsoft Excel to solve for the optimal widths to minimize our delays (*by using the ratio of x and y we got from taking differentiation*). The table below shows the width values we got from using the solver. With all the width values, we can calculate E_{ref}, total Cap, and D_{min}, which is on the right side of the table.

Ind. Variables	**Optimal Width (um)**	**Dep. Variables**	**Dep. Values**
x1	1	*total Cap (C_{gate})*	277.39
x2	2	*Eref (C_{gate})*	277.39 V_{dd}^2
x3	3	*Energy Consumption (J)*	9.71E-12
y1	2.83		
y2	2.83	*Dmin/tp0*	18.60
y3	2.83	*Dmin (ps)*	468.11

Phase 2: Optimized Design

Summary of results from Phase-2

Design	x_1	x_2	x_3	y_1	y_2	y_3
Optimized	1	1.26	1.51	1.53	1.45	1.27

Delay	D_{min}	$1.1D_{min}$	$1.2D_{min}$	Energy reduction (%)
Sub-design	18.60	20.46	22.32	14.99

In phase II, our goal was to minimize energy while allowing for a mismatch in delays between the three branches. We began by writing the equation for energy in a cycle: $E = C_{cycle} \times V_{dd}^2$. We wanted energy in terms of C_{gate} and V_{dd} to compare it to E_{ref} of phase 1, where $\gamma = C_{intrinsic}/C_{gate} = 1.11$. We calculated C_{cycle} by calculating the intrinsic and gate capacitance seen at each node as shown below:

$$C_{cycle} = \gamma \cdot C_{gate} + (x_1 + x_2 + x_3) \cdot C_{gate} + C_A + C_B + C_C$$

Branch A: $C_A = \gamma \cdot x_1 \cdot C_{gate} + 2 \cdot y_1 \cdot C_{gate} + 2 \cdot (\gamma \cdot y_1 \cdot C_{gate} + C_L)$

Branch B: $C_B = \gamma \cdot x_2 \cdot C_{gate} + 4 \cdot y_2 \cdot C_{gate} + 4 \cdot (\gamma \cdot y_2 \cdot C_{gate} + C_L)$

Branch C: $C_C = \gamma \cdot x_3 \cdot C_{gate} + 6 \cdot y_3 \cdot C_{gate} + 6 \cdot (\gamma \cdot y_3 \cdot C_{gate} + C_L)$

After we had a formula for C_{cycle}, we saw that in order to decrease the overall energy, we wanted to assign the greatest amount of delay, $D_{min} \times 1.2$, to branch C. As shown by the equation for C_c, y_3 adds the *most capacitance* because it is involved in *six branches*, and is consequently multiplied by the greatest factor. Thus, we wanted to assign the largest delay to this branch:

$$D_C = t_{p0}\left[(1 + \frac{x_1 + x_2 + x_3}{1.11}) + (1 + \frac{6 \cdot y_3}{1.11 \cdot x_3}) + (1 + \frac{16}{1.11 \cdot y_3})\right]$$

By increasing D_C it will allow y_3 to become small since the last term has y_3 in the denominator. The y_3 in the second term is not as important because it is offset by x_3, which can be changed as D_C increases.

Once we had these constraints set, we inputted the equations into Excel and solved for the minimum C_{cycle} with the constraints of x_i and $y_i \geq 1$, $D_A \leq D_{min}$ of phase 1, $D_B \leq 1.1 \times D_{min}$, and $D_C \leq 1.2 \times D_{min}$. The table below summarizes our results from Excel:

Ind. Variables	Optimal Width (um)	Dep. Variables	Dep. Values
x1	1	*total Cap (C_{gate})*	235.81
x2	1.26	*E_{ref} (C_{gate})*	$235.81 \times Vdd^2$
x3	1.51	*Energy Consumption (J)*	8.25E-12
y1	1.53		
y2	1.45		
y3	1.27		

Delay	Delay/tp0	Delay	(ps)
D_A/tp0	18.60	*D_A*	468.11
D_B/tp0	20.46	*D_B*	514.92
D_C/tp0	22.32	*D_C*	561.73

We tested our assumption that branch C required the largest delay in Excel by setting the constraints as $D_A \leq 1.2 \times D_{min}$, $D_B \leq 1.1 \times D_{min}$, and $D_C \leq D_{min}$, and found the total capacitance to be greater; thus, our initial assumption was correct.

Phase 3: HSPICE Verification

Summary of results from Phase-3

D_{min} (ps)	E_{ref} (nJ)	D inc (%)	E red (%)
427.8	9.88×10^{-3}	9.43	19.2

<u>Considerations for SPICE Simulation</u>:

1. Add three *unit-size inverters* at the beginning to ensure realistic input signal slope.
2. Normalize all the inverters to *unit-size* by using the "m" tag. (eg. If width = 2.9um, then use width=0.97um and m=3 instead of width=2.9um and m=1), since that was our assumption when we did our hand calculations.
3. Add a *big inverter* after the 16x inverter to suppress *miller kick-back effect* (because the input won't track the output node very well with a big capacitor).
4. Use different voltage sources for those inverters where we don't want to measure energy.
5. Look at the current through each node of interest and compare it with the values we got directly from V_{dd}.
6. Look at the *delay* and *rise/fall time* of each inverter and see if it is bigger or smaller than what we expected.

<u>Phase I:</u>

Simulation Delay:	427.8ps	*Hand Calculation Delay:*	468.1ps
Difference:	40.3ps	*% Difference:*	8.6%

Why is there such big discrepancy? We went in and measured the rise/fall time of each node of interest and calculated their difference; then we calculated the delays through each node.

in* \ *node	***in***	***d0***	***d1***	***d2***
Low-High	Rise: 1.6×10^{-10} Slope: 3.24×10^{10}	Fall: 4.7×10^{-10} Slope: -1.27×10^{10}	Rise: 7×10^{-10} Slope: 7.63×10^{9}	Fall: 5×10^{-10} Slope: -1.02×10^{10}
High-Low	Fall: 1.39×10^{-10} Slope: -4.00×10^{10}	Rise: 5.86×10^{-10} Slope: 8.4×10^{9}	Fall: 6.51×10^{-10} Slope: -1.05×10^{10}	Rise: 4.57×10^{-10} Slope: 9.39×10^{9}

Difference **Difference** **Difference**

in \ ***Inverters***	X_{in1}	X_{A1}	X_{A2}
Difference of Rise and Fall (s)	4.47×10^{-10} 3.1×10^{-10}	6.5×10^{-11} 1.3×10^{-10}	-1.94×10^{-10} -2×10^{-10}
HSPICE DELAY (s)	1.225×10^{-10}	1.515×10^{-10}	1.56×10^{-10}
Hand Cal DELAY (s)	1.62×10^{-10}	1.53×10^{-10}	1.53×10^{-10}
Fan-in / Fan-out	1 / 6	6 / 5.64	5.64 / 2.84

As we can see from the table above, there is a large difference between the input and output signals' rise/fall time of X_{in1} (compared to the other two inverters) which results in a big discrepancy between the calculated delay and HPISCE delay. When we look back at the delay formula we used when we did our hand calculations: *delay = $t_{p0}\times(1+fanout/gamma)$*, t_{p0} and gamma are given and not likely to change, so the discrepancy must result from the non-ideal fan-out. We assumed that each inverter has the same fan-out, but this is clearly not the case. As a result, we got a smaller delay from the SPICE simulations than from our hand calculations. *If we wanted to make the circuit behave closer to our hand calculations, we would make a larger fan-in for X_{in1}.*

For the energy calculations, we tried to measure the currents going through V_{dd}; however, we thought the current we measured might not be very accurate since it could include *short-circuit current,* which we didn't try to minimize in phase II (because we cannot really calculate that current). In order to correct this, we measured the current at each node during the correct time-interval by inserting zero-volt voltage sources, and we got the following results (with C_{gate}=5.6fF):

Simulation Energy @ V_{dd}:	9.88×10^{-12}J	*Hand Calculation Delay:*	9.7×10^{-12}J
Difference:	0.18×10^{-12}J	*% Difference:*	1.8%

Simulation Energy @ nodes: 7.82×10^{-12}J $\Rightarrow$ big discrepancy (we realized that this current does not include the currents charging intrinsic capacitors, but only those charging C_{gate})

Phase II:

Simulation Delay:	468.2ps	*Hand Calculation Delay:*	561.73ps
Difference:	93.52ps	*% Difference:*	16.65%

The simulation results of phase II are similar to phase I, in that the discrepancy between hand calculations and SPICE simulations result from differences in fan-in and fan-out of particular inverters. As the shown in the following table, the largest differences between fan-in and fan-out occur at inverters X_{in1} and X_{C2} in phase II. *If I would change one thing to make my circuit behaves closer to my hand calculations, I would make fan-in and fan-out of first and third inverter closer to each other*. The energy simulation and hand calculations are also shown below:

Simulation Energy @ V_{dd}:	7.98×10^{-12}J	*Hand Calculation Delay:*	8.25×10^{-12}J
Difference:	0.27×10^{-12}J	*% Difference:*	3.3%

in \ *node*	***in***	***d0***	***d5***	***d6***
Low-High	Rise: 2.8×10^{-10} Slope: 2.68×10^{10}	Fall: 4.8×10^{-10} Slope: -1.83×10^{10}	Rise: 6.8×10^{-10} Slope: 9.95×10^{9}	Fall: 7.7×10^{-10} Slope: -6.0×10^{9}
High-Low	Fall: 1.11×10^{-10} Slope: -3.85×10^{10}	Rise: 4.43×10^{-10} Slope: 1.34×10^{9}	Fall: 3.14×10^{-10} Slope: -1.29×10^{10}	Rise: 7.95×10^{-10} Slope: 4.71×10^{9}

Difference **Difference** **Difference**

in \ *Inverters*	X_{in1}	X_{C1}	X_{C2}
Difference of Rise and Fall (s)	2.0×10^{-10}	2.0×10^{-11}	$.9\times10^{-10}$
	3.32×10^{-10}	-1.29×10^{-10}	4.81×10^{-10}
HSPICE DELAY (s)	$.875\times10^{-10}$	1.32×10^{-10}	2.50×10^{-10}
Hand Cal DELAY (s)	1.11×10^{-10}	1.40×10^{-10}	2.86×10^{-10}
Fan-in / Fan-out	1 / 3.77	3.77 / 5.05	5.05 / 12.6

Accuracy of hand calculations can be improved by taking: **1.** *Slope Effect*, **2.** *Signal arrival times* into account.