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TuTh9:30-11am

## EECS 141: SPRING 03—MIDTERM 1 SOLUTIONS

|             |                 |
|-------------|-----------------|
| <b>NAME</b> | <b>SOLUTION</b> |
| Last        | First           |

|            |  |
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| <b>SID</b> |  |
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**Problem 1 (on 12):**

**Problem 2 (on 9):**

**Problem 3 (on 9):**

|                          |           |
|--------------------------|-----------|
| <b>Total<br/>(on 30)</b> | <b>30</b> |
|--------------------------|-----------|

**PROBLEM 1: Power (12 pts)**

Consider the circuit of Fig. 1. The signal waveforms of each signal within one period are shown in Fig. 2. You may assume that these signals are repeated with a frequency of 1 MHz (or  $T = 1 \mu s$ ). Use the following device parameters:  $V_T = 0.5 \text{ V}$ ;  $\gamma = 0$ ;  $R_{on} = 10 \text{ k}\Omega$ ;  $R_{off} = \infty$ . You may ignore the parasitic capacitances of the transistors.

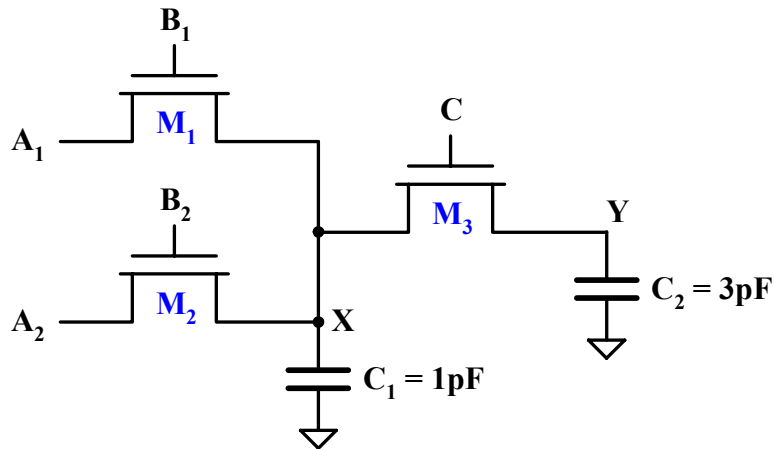


Fig. 1

a. Draw the waveform of the signals on nodes  $X$  and  $Y$ , assuming that all input signals are switching between 0 and 2.0 V. (4 pts)

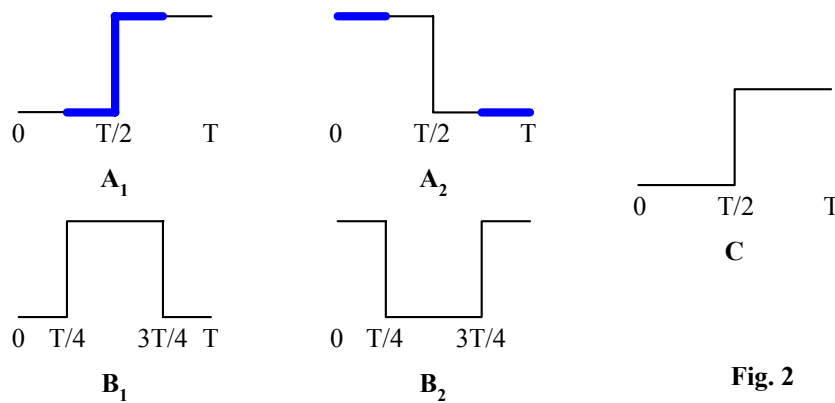
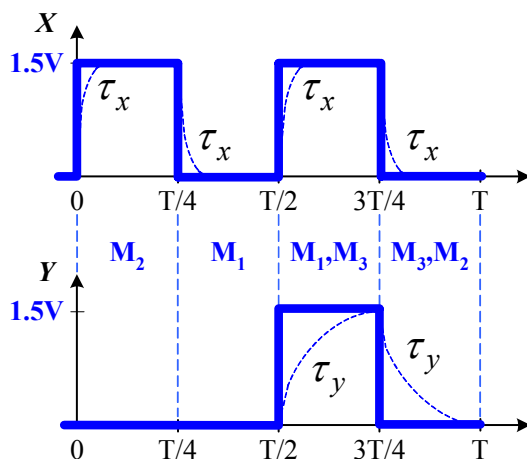


Fig. 2



**Signals of nodes X and Y reach  $V_{DD} - V_T = 1.5V$ .**

**Conducting devices are labeled in the graph.**

**Full credit for square waveforms on the left! Extra points if you considered time constants as indicated by thin lines. ( $T/4 = 250ns$ ).**

$$\tau_x = R_{on} C_1 = 10ns$$

$$\tau_y = R_{on} C_1 + (R_{on} + R_{on}) C_3 = 70ns$$

**Resulting waveforms are shown on the left.**

b. Calculate the dynamic power dissipation of this circuit. (2 pts)

**Dynamic power consumption is given by:**  $P_{dyn} = \alpha \cdot f \cdot C \cdot V_{DD} \cdot (V_{DD} - V_T)$

**Signal at node X makes two transitions during one clock period, so the energy per transition at node X has to be doubled. The total dynamic power consumption is therefore given by:**

$$P_{dyn} = f \cdot (2C_1 + C_3) \cdot V_{DD} \cdot (V_{DD} - V_T) = 15 \mu W$$

**$P_{dyn} = 15 \mu W$**

c. The power consumption of the CMOS inverter can be minimized through circuit optimizations. Determine how each circuit parameter mentioned in the table should be changed to reduce the different inverter power consumption components (6 pts)

**For each parameter, fill in one of the following choices in the blanks:**

**A** – Increase    **B** – Decrease    **C** – Doesn't affect this type of power consumption

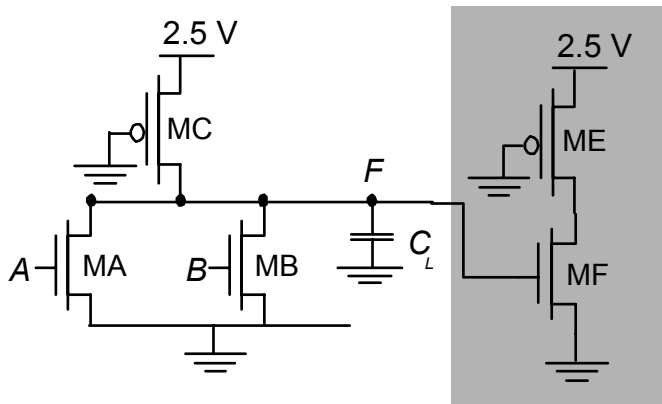
| Goal  | Circuit Parameter Optimization  | A, B or C |
|---|---------------------------------|-----------|
| Minimize the dynamic power consumption due to CL charging and discharging                   | Vdd                             | <b>B</b>  |
|   | CL                              | <b>B</b>  |
|   | Transistor  Vth                 | <b>C</b>  |
|   | Transistor widths (first order) | <b>C</b>  |
| Minimize the direct-path power consumption (assume a fixed rise and fall time at the input) | Vdd                             | <b>B</b>  |
|   | CL                              | <b>A</b>  |
|   | Transistor  Vth                 | <b>A</b>  |
|   | Transistor widths               | <b>B</b>  |
| Minimize the static power dissipation   | Vdd                             | <b>B</b>  |
|   | CL                              | <b>C</b>  |
|   | Transistor  Vth                 | <b>A</b>  |
|   | Transistor widths               | <b>B</b>  |

**PROBLEM 2: VTC and propagation delay (9 pts)**

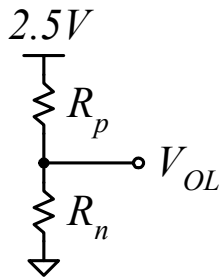
Consider the digital circuit shown below. It pictures an alternative 2-input NOR gate followed by a single fanout inverter. To make the analysis of this circuit easy, we are using simplified transistor models. First of all, we assume that the transistor can be represented by a linear resistor, this is

NMOS (for  $W/L = 1$ ):  $R_{N_{on}} = 10\text{ k}\Omega$ ;  $R_{N_{off}} = \infty$ ;  $V_{TN} = 0.75\text{V}$ .

PMOS (for  $W/L = 1$ ):  $R_{P_{on}} = 20\text{ k}\Omega$ ;  $R_{P_{off}} = \infty$ ;  $V_{TP} = -0.75\text{V}$ .



a. Assume that the PMOS is of minimum size (this is,  $W/L = 1$ ). Determine the sizes of the two NMOS transistors MA and MB so that the  $V_{OL}$  of the NOR gate is **at most** 0.5 V. Also describe under what conditions this happens. (2pts).



**Worst case  $V_{OL}$  occurs when only one NMOS is “on”**

$$\frac{R_n}{R_n + R_p} V_{DD} = V_{OL} \Rightarrow R_n = 5\text{ k}\Omega \Rightarrow \left(\frac{W}{L}\right)_n = 2$$

$(W/L)_{MA} = 2$   
 $(W/L)_{MB} = 2$

b. The parasitic capacitances of a unit size NMOS and PMOS transistor are given in the table below. You may assume that **all capacitances are constant and linear over the operation range**. Determine the equivalent load capacitance  $C_L$  at the output of the NOR gate (i) for  $A$  switching from  $0 \rightarrow 1$ , and  $B = 0$ ; (ii) for  $A$  and  $B$  switching simultaneously from  $0 \rightarrow 1$ . You should use the sizes derived in a. for both the NOR gate and the fanout inverter. (4 pts)

Hint: In case you are not sure about your answer in a, use  $(W/L)_{NMOS} = 3$ .

**Table 1: Transistor capacitances (for W/L = 1)**

| Cap in fF | $C_{gs}$ | $C_{gd}$ | $C_{gb}$ | $C_{sb}$ | $C_{db}$ |
|-----------|----------|----------|----------|----------|----------|
| NMOS      | 0.1      | 0.15     | 0.2      | 0.25     | 0.3      |
| PMOS      | 0.12     | 0.17     | 0.22     | 0.27     | 0.32     |

Table below summarizes contribution from each transistor (factor 2 is due to Miller effect):

| Transistor (size W/L) | (i) A: 0→1, B = 0          | (ii) A, B: 0→1     |
|-----------------------|----------------------------|--------------------|
| MA (2)                | $C_{db} + 2C_{gd}$         | same               |
| MB (2)                | $C_{db} + C_{dg}$          | $C_{db} + 2C_{gd}$ |
| MC (1)                | $C_{db} + C_{dg}$          | same               |
| MF (2)                | $C_{gs} + C_{gb} + C_{gd}$ | same               |
| Total CL              | 3.49 fF                    | 3.79 fF            |

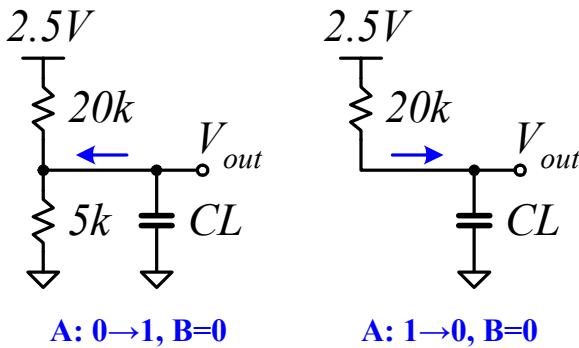
For total C, you need to multiply numbers from Table 1 by (W/L) of each transistor

$CL_{(A: 0 \rightarrow 1; B=0)} = 3.49 \text{ fF}$   
 $CL_{(A,B: 0 \rightarrow 1)} = 3.79 \text{ fF}$

(4.99 fF for  $W_n = 3$ )

(5.44 fF for  $W_n = 3$ )

c. Determine the propagation delay of the NOR gate for A switching from 0→1 and 1→0, while B=0. For  $C_L$ , use the answer you got in b. If not sure, use  $C_L = 8 \text{ fF}$ . You may assume that the VM of the gate is approximately at  $V_{DD}/2$ . (3 pts)



**A: 0→1, worst case (longest) delay occurs when only one NMOS is "on"**

$$t_{p0 \rightarrow 1} = CL \cdot (20k \parallel 5k) \cdot \ln \left( \frac{V_{DD} - V_{OL}}{V_{DD}/2} \right)$$

$$t_{p0 \rightarrow 1} = 0.69 \cdot CL \cdot (20k \parallel 5k) \text{ (also OK)}$$

**A: 1→0**

$$t_{p1 \rightarrow 0} = 0.69 \cdot CL \cdot 20k = 52.30 \text{ ps}$$

These are acceptable answers:

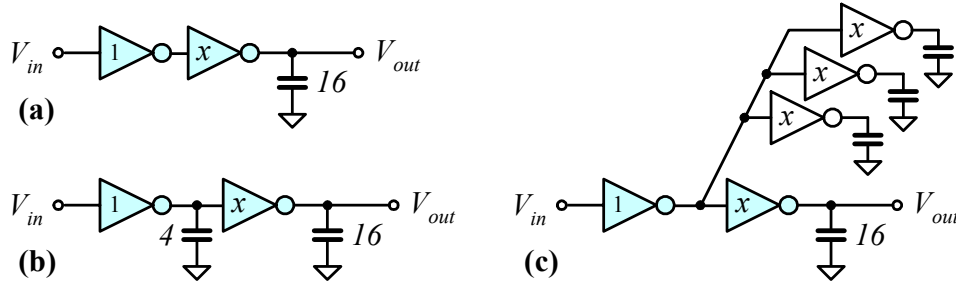
$t_{p0 \rightarrow 1} = 6.6 \text{ ps}$  (also OK: 9.4ps)  
 $t_{p1 \rightarrow 0} = 48.2 \text{ ps}$

$CL = 8\text{fF}$ : 15.0 ps (also OK: 22.1ps)

$CL = 8\text{fF}$ : 110.4 ps

**PROBLEM 3: Sizing (9 pts)**

The circuits shown in the figure below illustrate the impact of small topological changes on the delay and energy, when driving a fixed load at the output. You may assume that  $\gamma = 1$  (or  $C_{intrinsic} = C_{gate}$ ). For each of the circuits in the Figure, calculate following:



a. Size  $x$  of the second inverter in the chain to minimize propagation delay from input  $V_{in}$  to output  $V_{out}$ . (6 pts)

Hint: do not blindly use the equations given in the book.

**Gate delay is given by:**

$$t_p = t_{p0} \cdot (1 + f/\gamma)$$

**Using this equation, we can obtain total delay as follows:**

(a)  $d_{tot} = (1 + x/1) + (1 + 16/x) \Rightarrow \partial d_{tot} / \partial x = 1 - 16/x^2 \Rightarrow x = 4$

**note: this is well-known geometric mean result.**

(b)  $d_{tot} = (1 + (4 + x)/1) + (1 + 16/x) \Rightarrow \partial d_{tot} / \partial x = 1 - 16/x^2 \Rightarrow x = 4$

**note: geometric mean result ( $x = 2.5$ ) is wrong in this case! For exercise, plug in  $x = 2.5$  and  $x = 4$  in the delay formula and check which result gives smaller delay.**

(c)  $d_{tot} = (1 + 4x/1) + (1 + 16/x) \Rightarrow \partial d_{tot} / \partial x = 4 - 16/x^2 \Rightarrow x = 2$

**note: geometric mean result is valid again (no fixed side-loads).**

$x$  (a) = 4  
 $x$  (b) = 4  
 $x$  (c) = 2

b. Energy consumed by the shaded path in all three cases (3 pts). You may assume that  $V_{DD} = 1$  V, and that the capacitances are given in fF. (3pts).

**Total energy of a gate can be simply obtained with following formula:**

$$E = (C_{intrinsic} + C_{gate}) \cdot V_{DD}^2$$

**Using this result, simply plug in the numbers from (a):**

$$E(a) = [(1+x) + (x+16)] \cdot V_{DD}^2 = 25 \text{ fJ}$$

$$E(b) = [(1+x+4) + (x+16)] \cdot V_{DD}^2 = 29 \text{ fJ}$$

$$E(c) = [(1+4x) + (x+16)] \cdot V_{DD}^2 = 27 \text{ fJ}$$

$$E(a) = 25 \text{ fJ}$$

$$E(b) = 29 \text{ fJ}$$

$$E(c) = 27 \text{ fJ}$$

**Note:** Although not correct, it is also acceptable if you included  $C_{in}$  of the first stage. (+ 1fJ to these numbers)