

UNIVERSITY OF CALIFORNIA
College of Engineering
Department of Electrical Engineering and Computer Sciences
Last modified on March 10, 2003 by Dejan Markovic (dejan@eecs.berkeley.edu)

Prof. Jan Rabaey

Lab #6: Buffer Design

EECS 141

1. Objective

As you have learned in class, there are numerous capacitive and resistive parasitic effects that are intrinsically present in digital circuits due to interconnections and parasitic loads. In this lab, you will examine various ways to cope with these parasitic effects and lessen their negative impact on your circuit. In this lab, you will design or rather choose buffers to improve the timing of a circuit. By doing so, you will begin to develop a feel for the tradeoffs involved with buffer design and hopefully better understand their usefulness.

Prelab: - Look through the lab and perform the hand calculations before entering your lab section.

- A library of buffers can be found in EE141 directory at [~ee141/LAB6/](#). Please copy the contents of the directory to your own lab6 directory.
`cp -r ~ee141/LAB6/ .`

Spend some time becoming familiar with the various library components, as you will be using these buffers extensively.

**Note:* The buffer names are in units of 0.1microns

2. Tasks

Part I:

- The minimum sized inverter in the library is not up to date. Please create an inverter in max with the same dimensions as shown in the first stage of Figure 1a below.
- Our design calls for a minimum sized inverter to drive a lumped capacitive load $C_L = 2.0$ pF with $V_{DD} = 2.5V$. In order to achieve better performance, two buffer stages are introduced as shown in Figure 1a below.

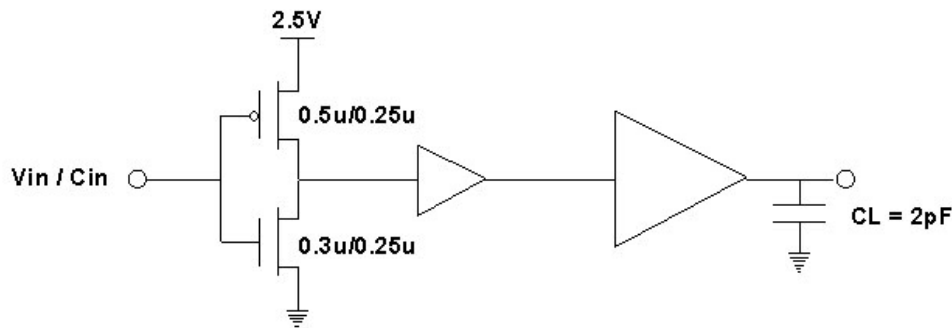


Figure 1a – Minimum Sized Inverter and Buffer Circuitry for driving a large load capacitance

- c. Extract the gate capacitance C_{in} of the minimum sized inverter (labeled *mininv.max*) Using this information, determine the propagation delay when it is driving an identical minimum sized inverter.

This is most easily accomplished using MAX to extract a layout and then simulating your resulting circuit using HSPICE (as you did in Lab 4: Circuit Extraction). For each part in the library, make sure to label V_{DD} and GND as previous discussed (referring to the project, set them as locals, and label them V_{DD} ! And GND !), and label vin as an input and $vout$ as an output so that MAX can create the subcircuit ports correctly.

- d. Using the information obtained in part c, select the two buffers from the library that would yield the best response (i.e. gives the fastest performance) for the circuit shown in Figure 1a. You may use the same buffer twice if you so decide. Please show your hand calculations to justify your choice of buffers (i.e. find t_{delay} through the whole circuit).
- e. In MAX, construct the circuit that you just designed in part d and simulate it. Remember to create a SPICE netlist from your layout using the extraction tool in MAX.

Drive the first inverter with a signal that has 0.1 ns rise and fall times. The propagation delay of the circuit should be measured as the time from the 50% point of the input to the 50% point of the output.

Did your simulated results match your hand analysis? Explain why or why not.

***Turn in:** Please turn in the answer to the above question, your hand calculations, your SPICE decks and the relevant AWAVES plots.

Part II: Extra credit (f-h)

- f. In reality, the resistance due to interconnects is also a problem. This effect gets increasingly worse with scaling, as wires widths shrink, causing the characteristic impedance to increase.

Consider a problem where a series of buffers are distributed across a chip to help drive a signal along a long trace with a TOTAL length = 10mm of polysilicon with width=1.8um and then onto the same 2pF load capacitor as above.

We will try to minimize the delay in this circuit by routinely inserting buffers, as indicated below in Figure 1b. Also note that the design is a mixture of the buffer and repeater approaches as described in your reader.

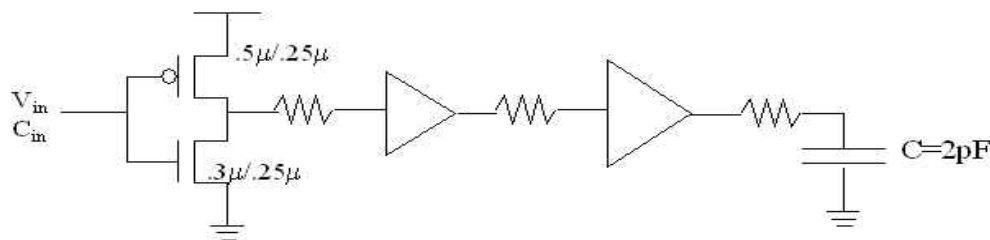


Figure 1b – Minimum Sized Inverter with Buffer Circuitry along a long trace

For the above diagram, use the parameters defined in your reader to determine the resistance and capacitance of the poly wire. Using these hand calculations, which you hopefully did for pre-lab, determine which buffers to utilize and where to place them such that your total delay time is minimized. Remember that the buffers may be placed anywhere along the trace!

- g. Simulate your new circuit by extracting the MAX layouts for each of the inverters and constructing the SPICE file corresponding to the schematic shown in Figure 1b.

Introduce the distributed delay line using the π 3 model (textbook, pg.171). How well did your simulated results match your hand calculations?

**Turn in:* Please turn in the answer to the above question, your hand calculations, your SPICE decks and the relevant AWAVES plots.

- h. Given what you have learned in this lab, class, and from your readings, toy around with the design by substituting different buffers and placing them in different spots along the line to see if you can further minimize your delay.

How does your final design differ from the one you determined using hand analysis?

**Turn in:* Please turn in the answer to the above question, your hand calculations, your SPICE decks and the relevant AWAVES plots for the design in part g. Also include your original dimensions and placement, and the results of your final experimentation.

3. Report

For your report, please hand in the following:

- Explanation and documentation of your design choices
- Printouts of your SPICE input decks and relevant AWAVES plots
- Answers to the questions posed in part I of the lab and hand analysis