

Low-Power Silicon Architectures for Wireless Communications

Embedded Tutorial , ASP-DAC 00

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Compelling Issues in Wireless (1)

Ubiquitous services put wireless spectrum at a premium

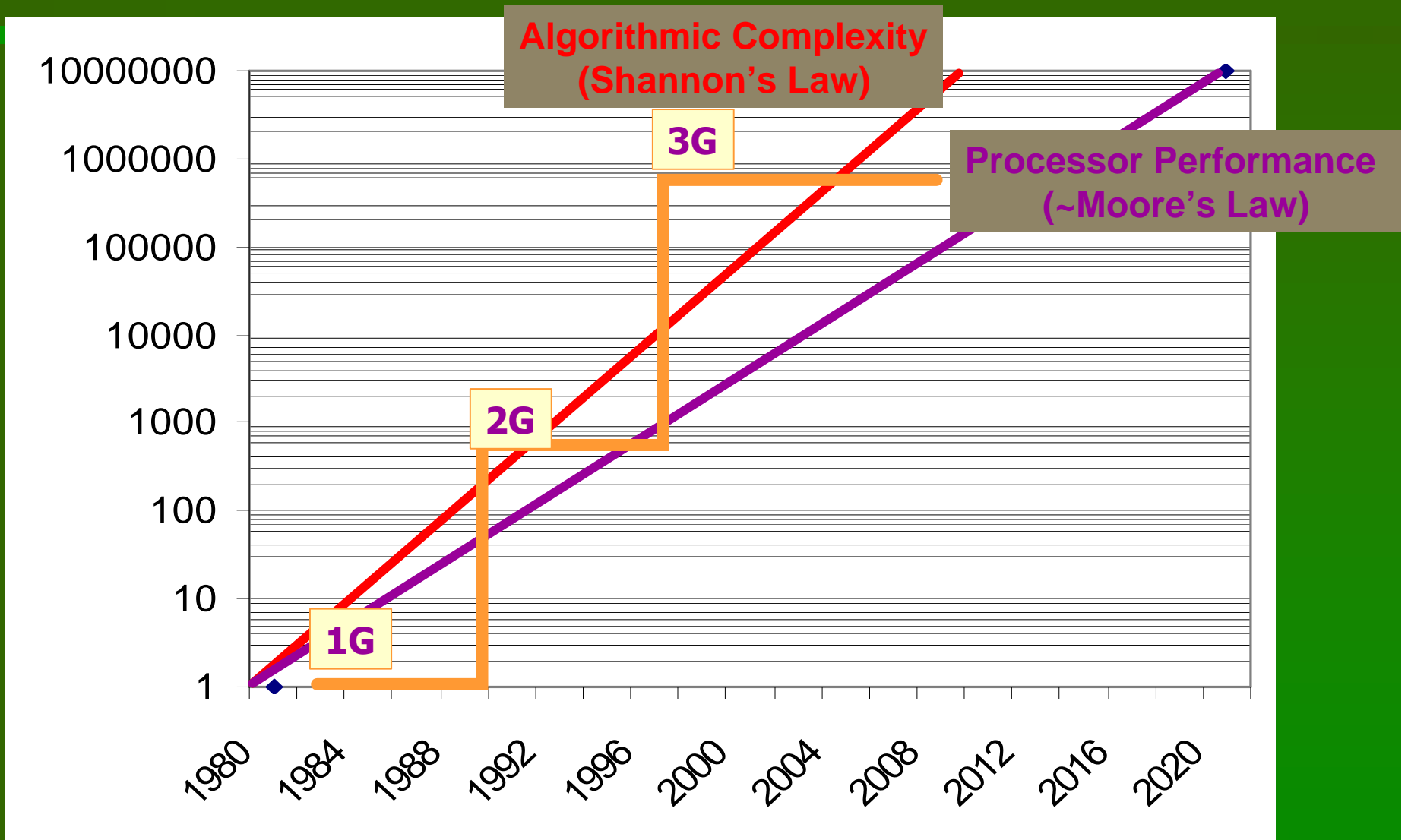
- Effective use of aether hampered by standardization and fragmentation
- Current spectral efficiency far below theoretical limits
- Emerging Solutions
 - Adoption of better spectrum utilization techniques (interference cancellation, multi-path fading mitigation and exploitation)
 - multi-functional, adaptive systems

Improving Spectral Density Comes at a Performance Cost

Digital Baseband Processing Requirements

	Wide-band CDMA			FDMA Multiple Antenna
	Matched Filter	Blind MMSE	Exact Decorrelator	SVD
Performance Bits/sec/Hz	1	2	2	6
Multiplications	124	496	230,000	736
Memory	248	1240	640,000	2120
ALU	124	502	240,000	800
Word Length	8-bit	12-bit	16-bit	16-bit

Shannon beats Moore's law



Courtesy: Ravi Subramanian, morphICs Tech. Inc

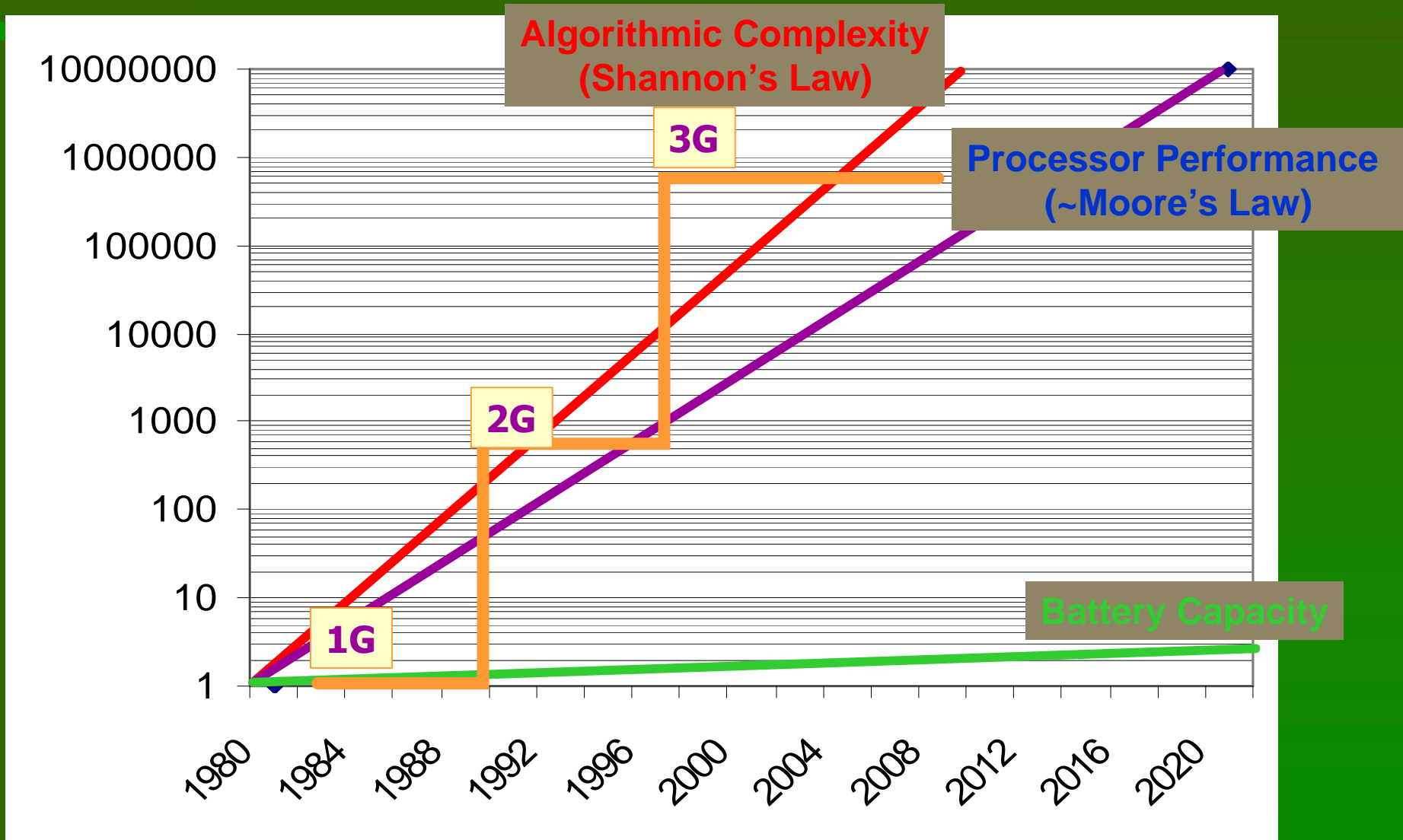
Compelling Issues in Wireless (2)

“The Last Meter Problem”

Ubiquitous wireless networking requires steep reduction in cost and energy dissipation

- To be acceptable, radio cost has to be between 50 cents and 5\$
- Frequent battery replacement on 100's of devices unacceptable
- Possible solutions
 - Intelligent self-configuring distributed networks optimize energy
 - System-on-a-chip

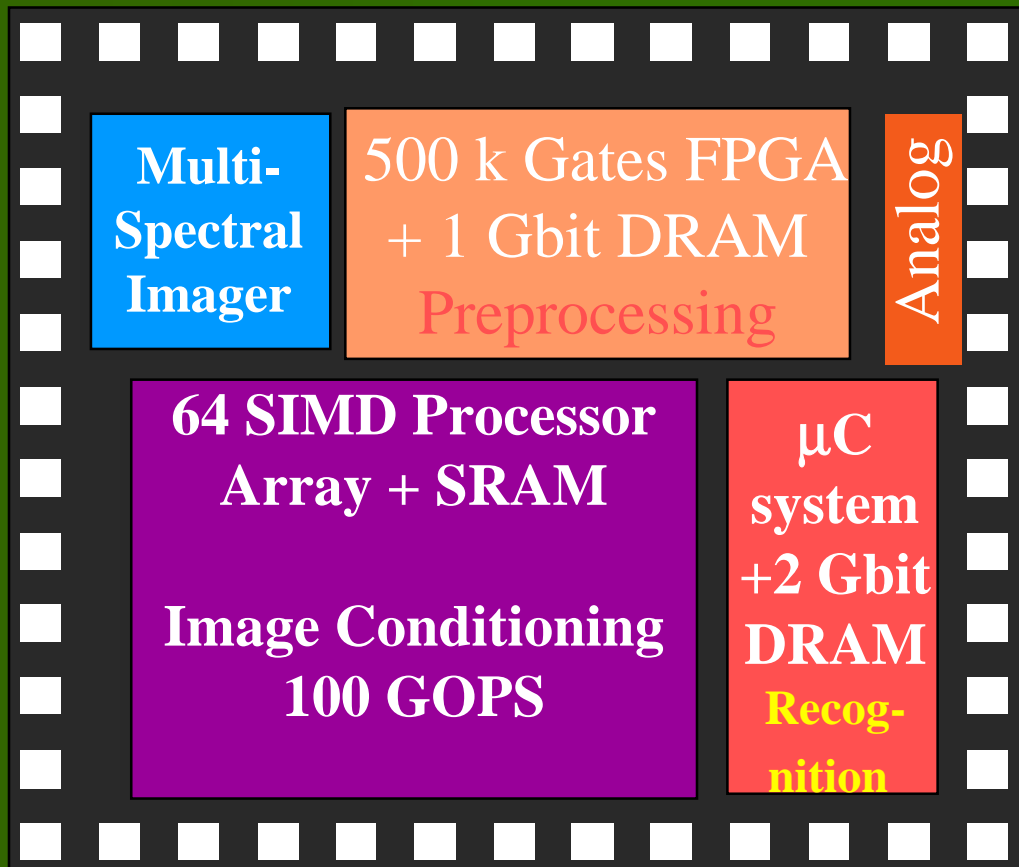
Energy to Play a Major Role



Courtesy: Ravi Subramanian, morphICs Tech. Inc

Design at a crossroad

System-on-a-Chip



- Embedded applications where **cost, performance, and energy** are the real issues!
- DSP and control intensive
- Mixed-mode
- Combines programmable and application-specific modules
- **Software plays crucial role**

The Changing Metrics

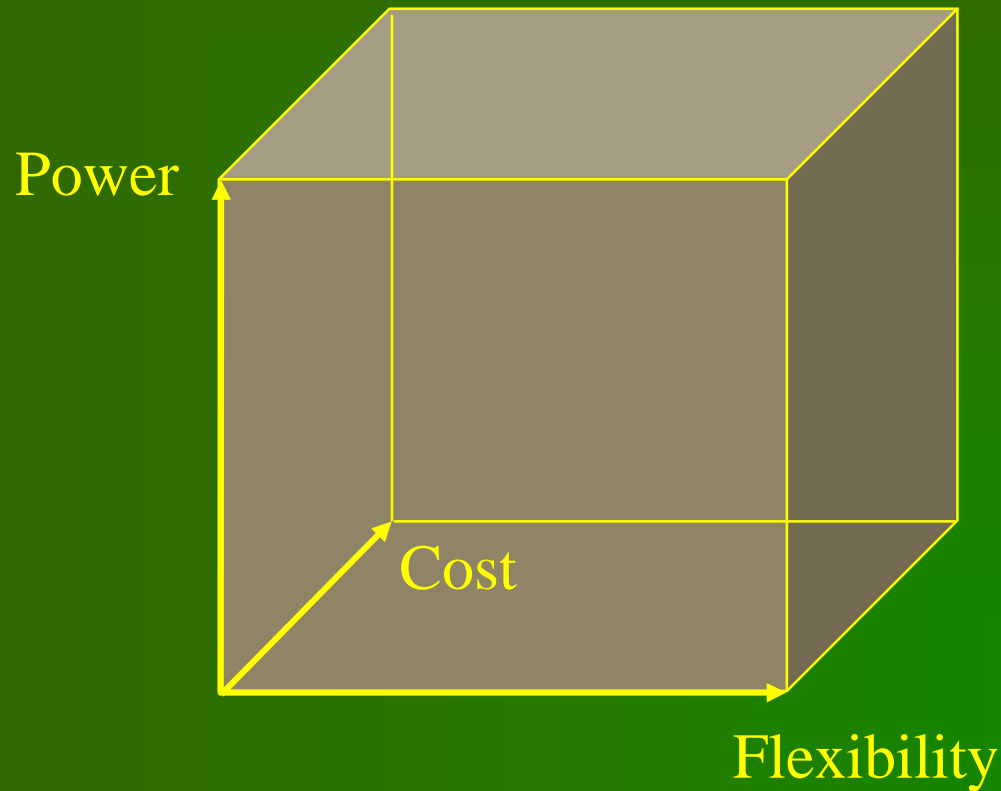
- **Power and/or Energy** have become dominant drivers
 - Limiting factor for performance and reliability in wall-plugged applications
 - Enabler for wide-spread use of distributed computing and data access
- Energy reduction requires joint optimization process between application and implementation

The Changing Metrics

- Cost of fabrication facilities and mask making has increased significantly
 - NRE cost of new design has increased significantly
- Physical effects (parasitics, reliability issues, power management) are increasingly significant in the design process
 - These must now be considered explicitly at the circuit level
- Design complexity, and “context complexity” is sufficiently high that design verification is a major limitation on time-to-market

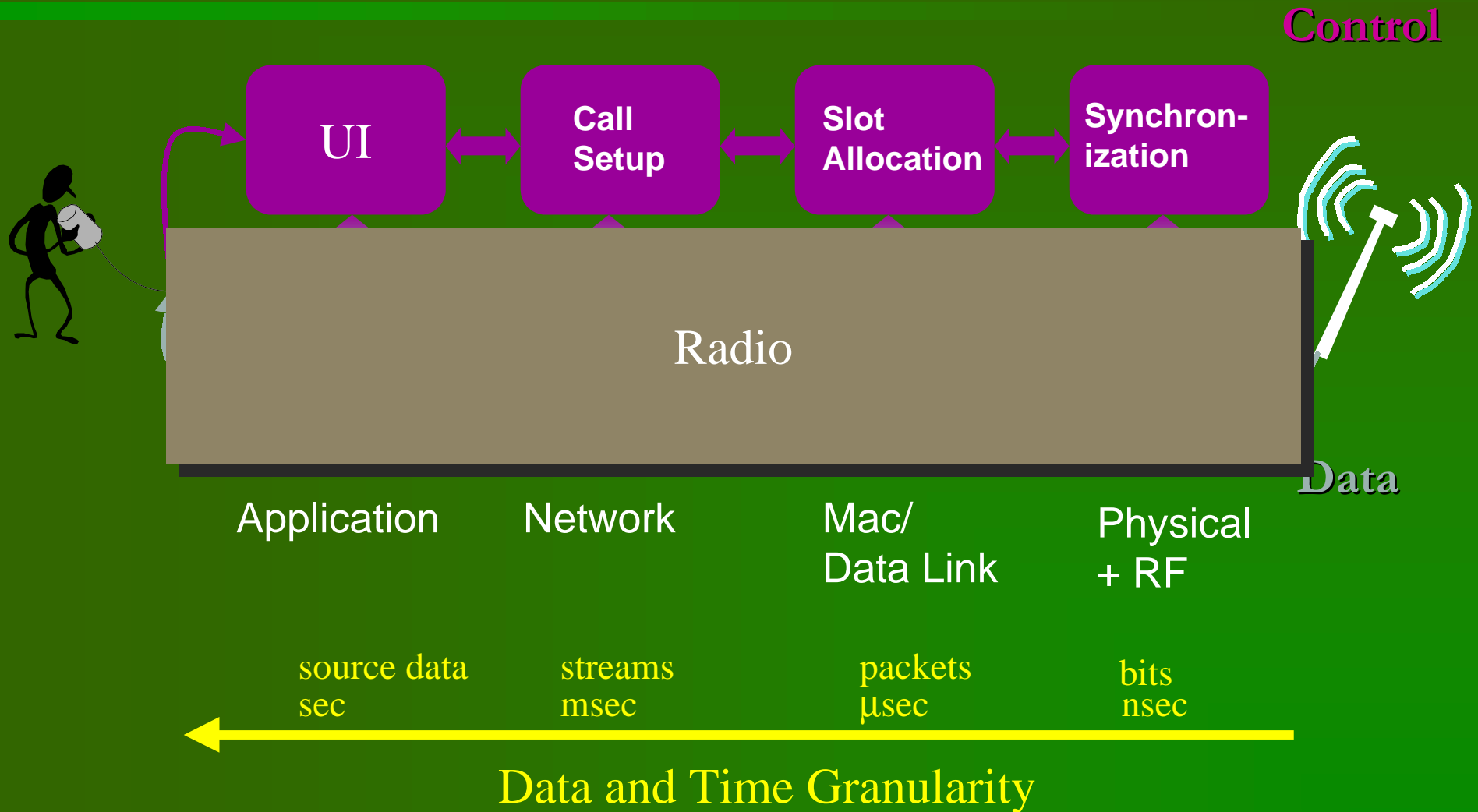
**Towards Fewer, but more Flexible
and Reusable Silicon Platforms**

The Changing Metrics

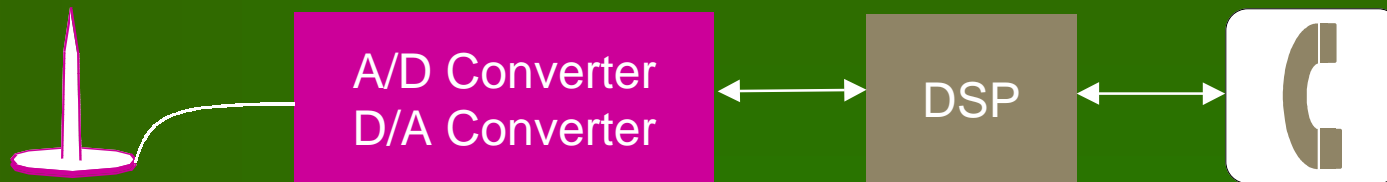


Performance as a Functionality Constraint
("Just-in-Time Computing")

Issues in Single-Chip Radio Design

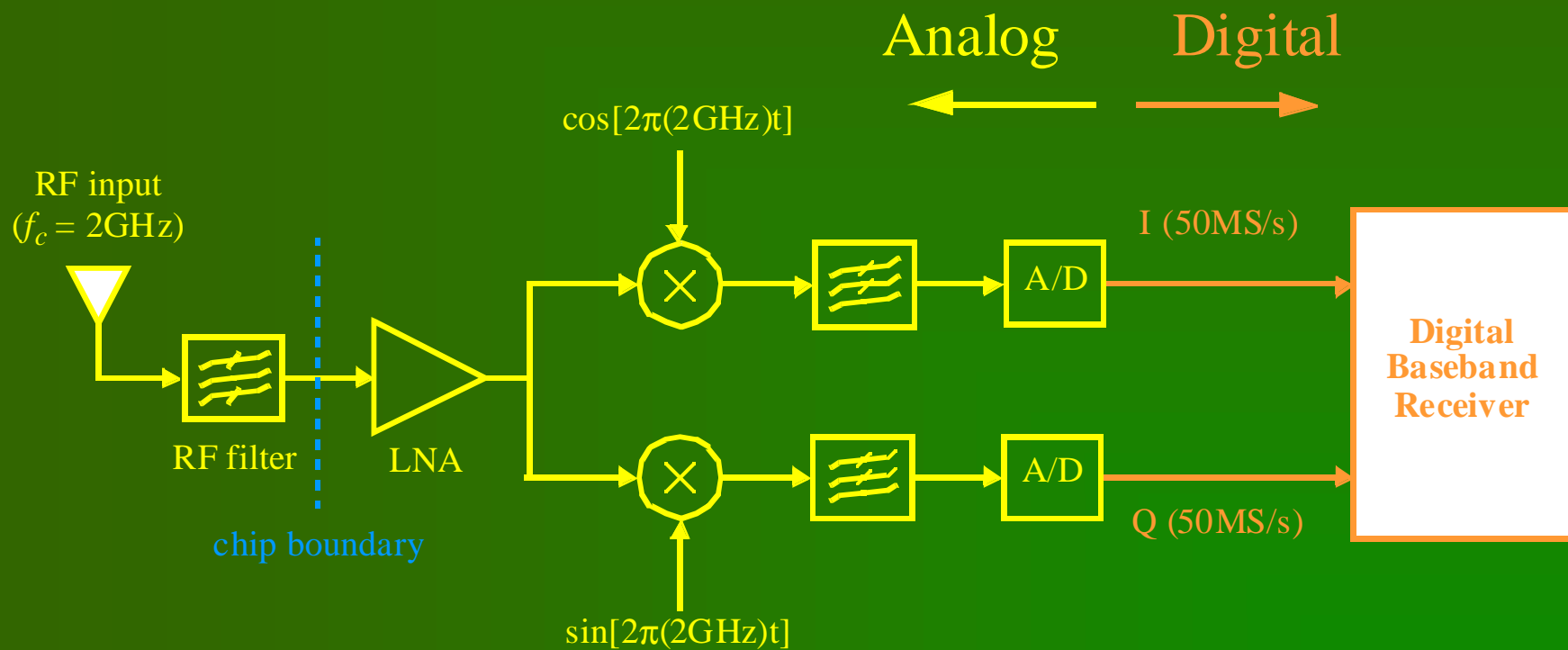


The Software Radio

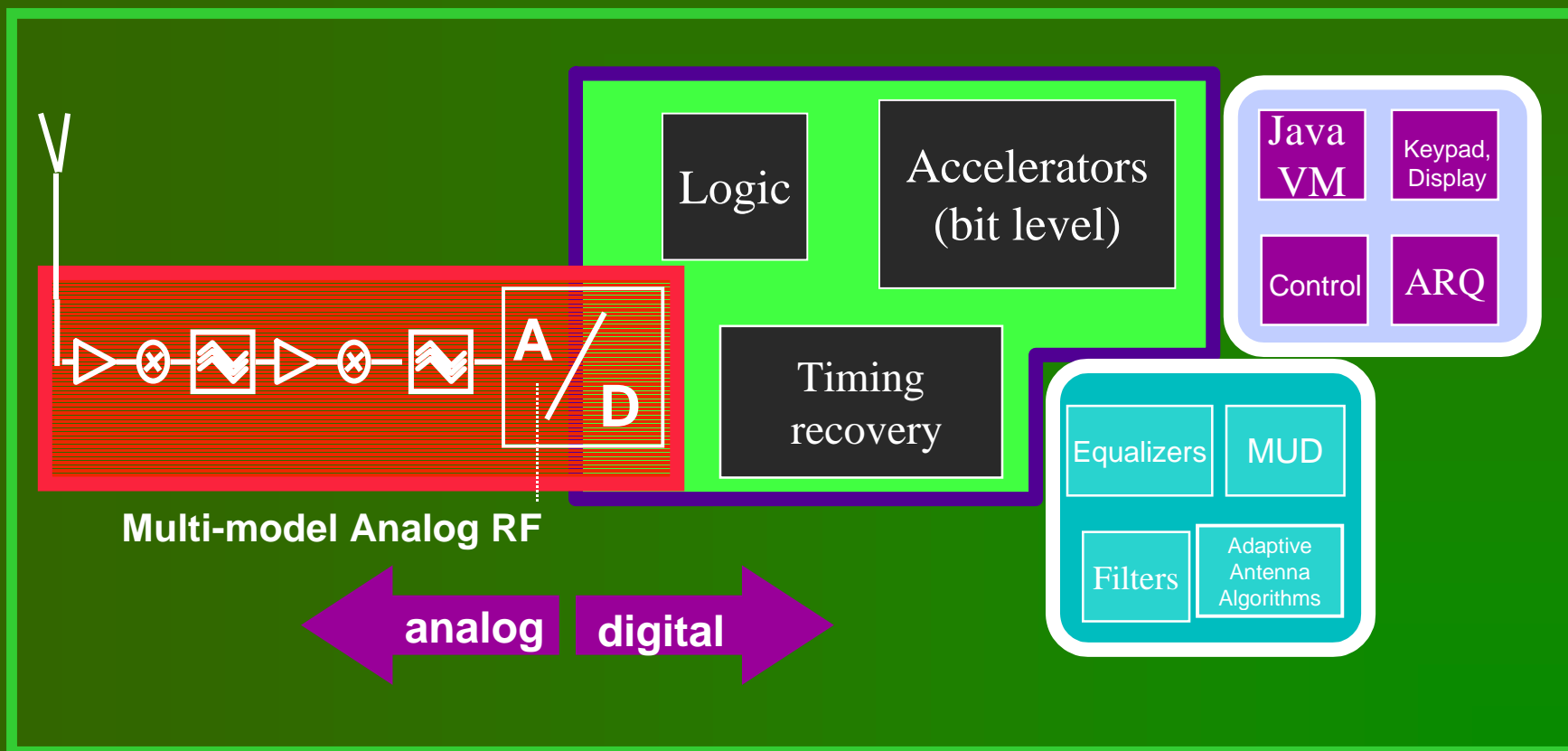


- Idea: Digitize (wideband) signal at antenna and use signal processing to extract desired signal
- Leverages of advances in technology, circuit design, and signal processing
- Software solution enables flexibility and adaptivity, but at huge price in power and cost
- 16 bit A/D converter at 2.2 GHz dissipates 1 to 10 W

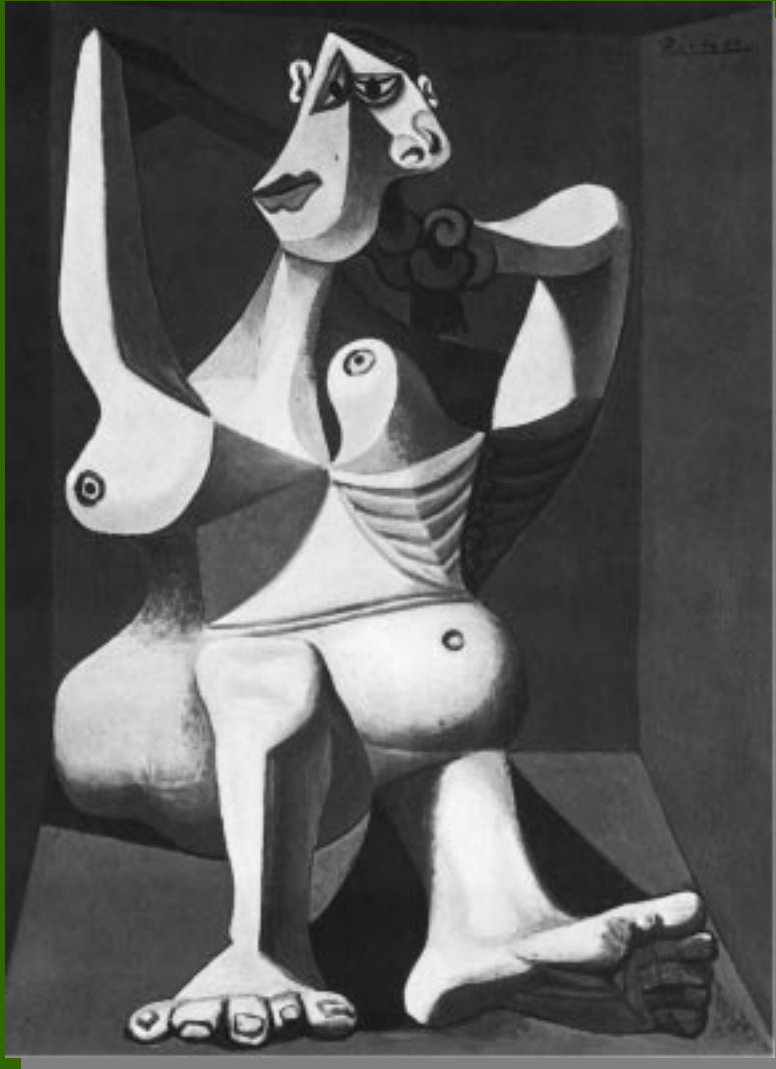
The Mostly Digital Radio



The Software-Definable Radio

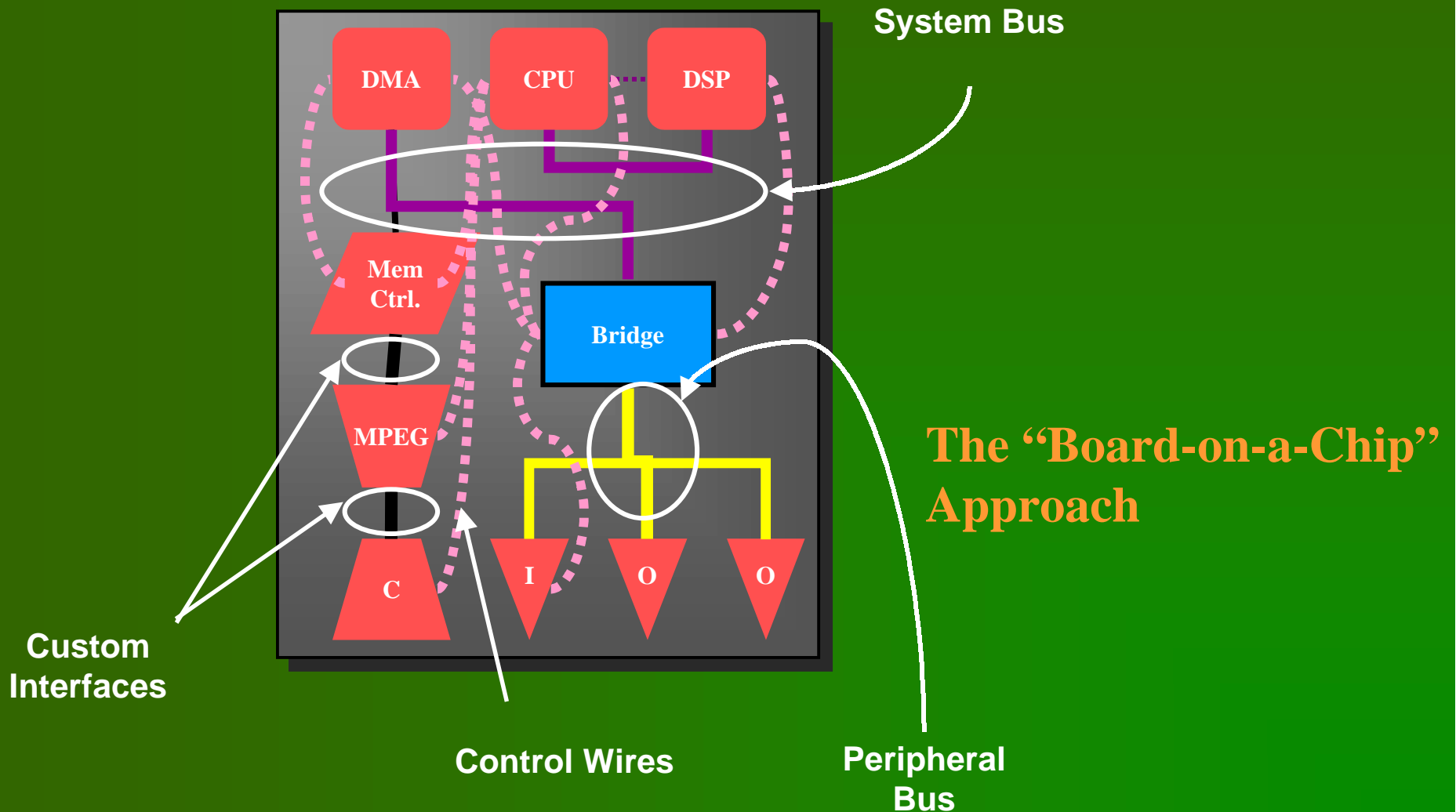


The System-on-a-Chip Nightmare



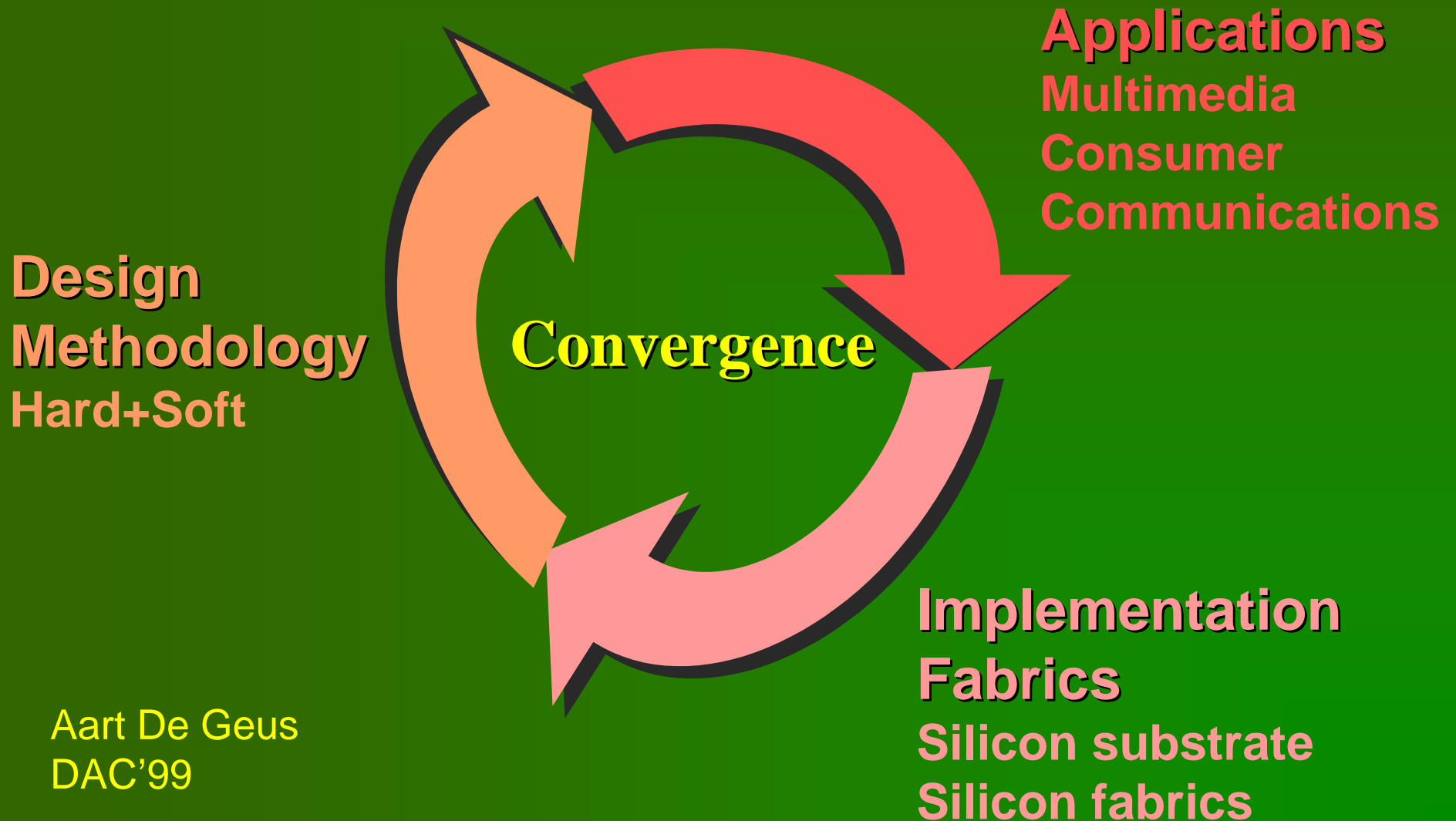
“Femme se coiffant”
Pablo Ruiz Picasso
1940

The System-on-a-Chip Nightmare



System-on-a-Chip

A Renaissance in Design



Aart De Geus
DAC'99

Platform-Based Design

“Only the consumer gets freedom of choice;
designers need freedom *from* choice”
(Orfali, et al, 1996, p.522)

- A platform is a *restriction on the space of possible implementation choices*, providing a well-defined abstraction of the underlying technology for the application developer
- New platforms will be defined at the *architecture-micro-architecture boundary*
- They will be *component-based*, and will provide a range of choices from structured-custom to fully programmable implementations
- Key to such approaches is the *representation of communication* in the platform model

Source:R.Newton

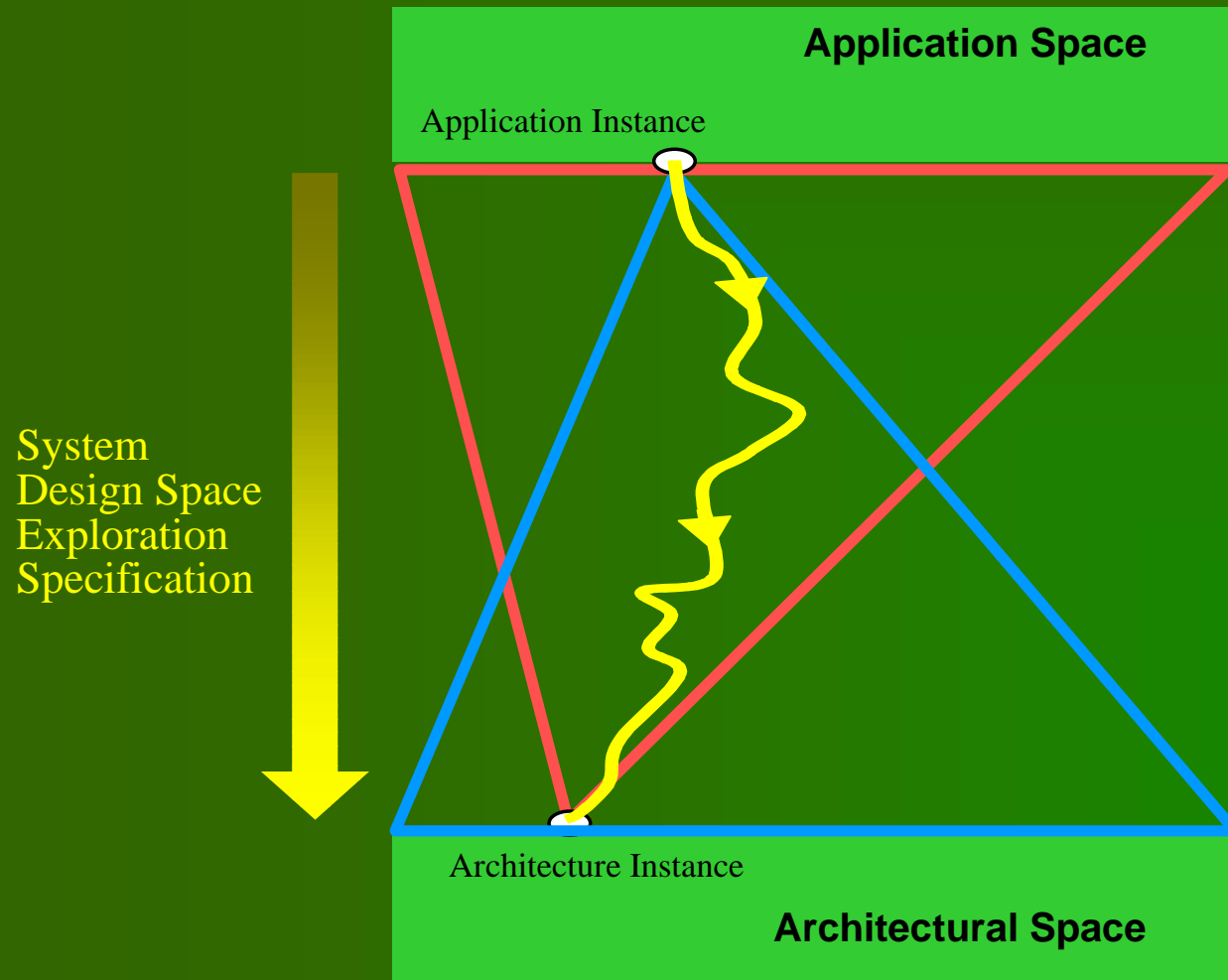
Hardware Platforms

Hardware Platform: not only a fully specified SoC but also *a family of architectures that share some common feature:*

A Hardware Platform is a family of architectures that satisfy a set of architectural constraints imposed to allow the re-use of hardware and software components.

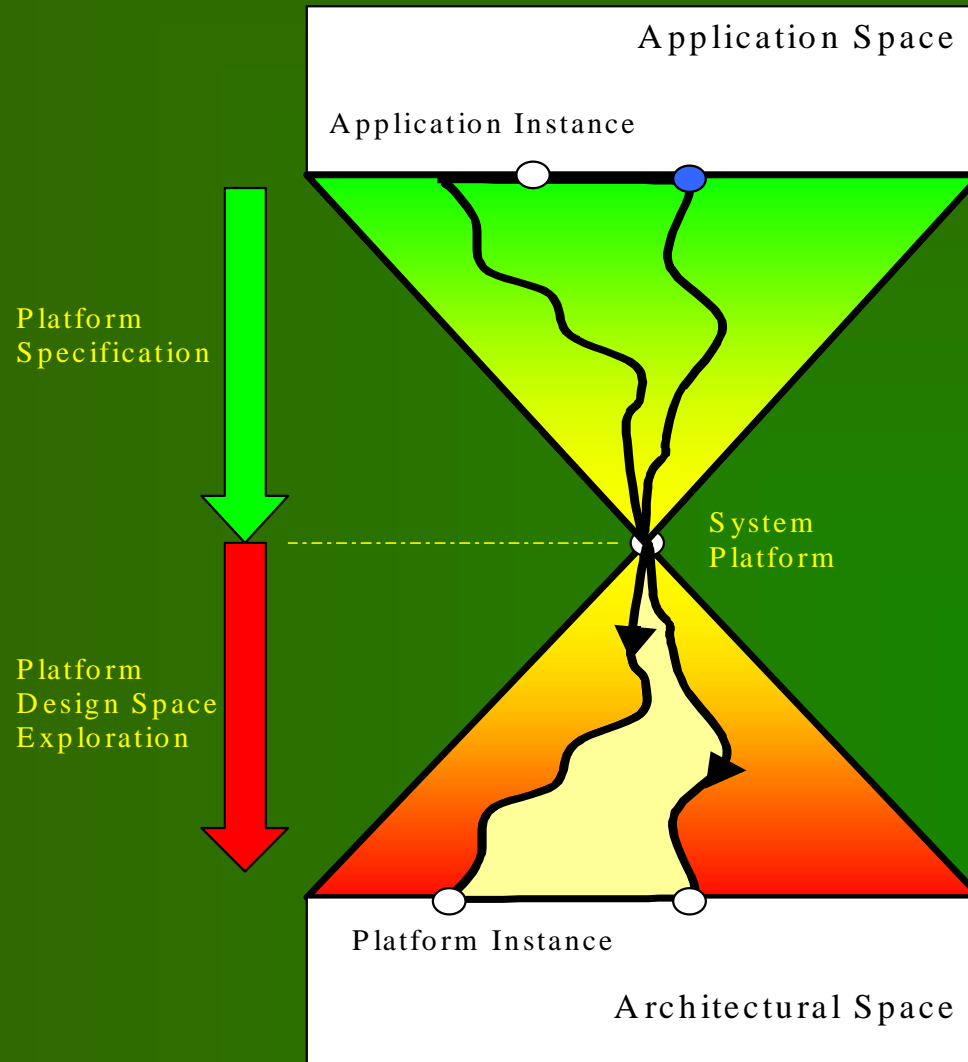
The stronger the constraints the more component re-use but stronger constraints imply fewer architectures to choose from!

The Platform Tension

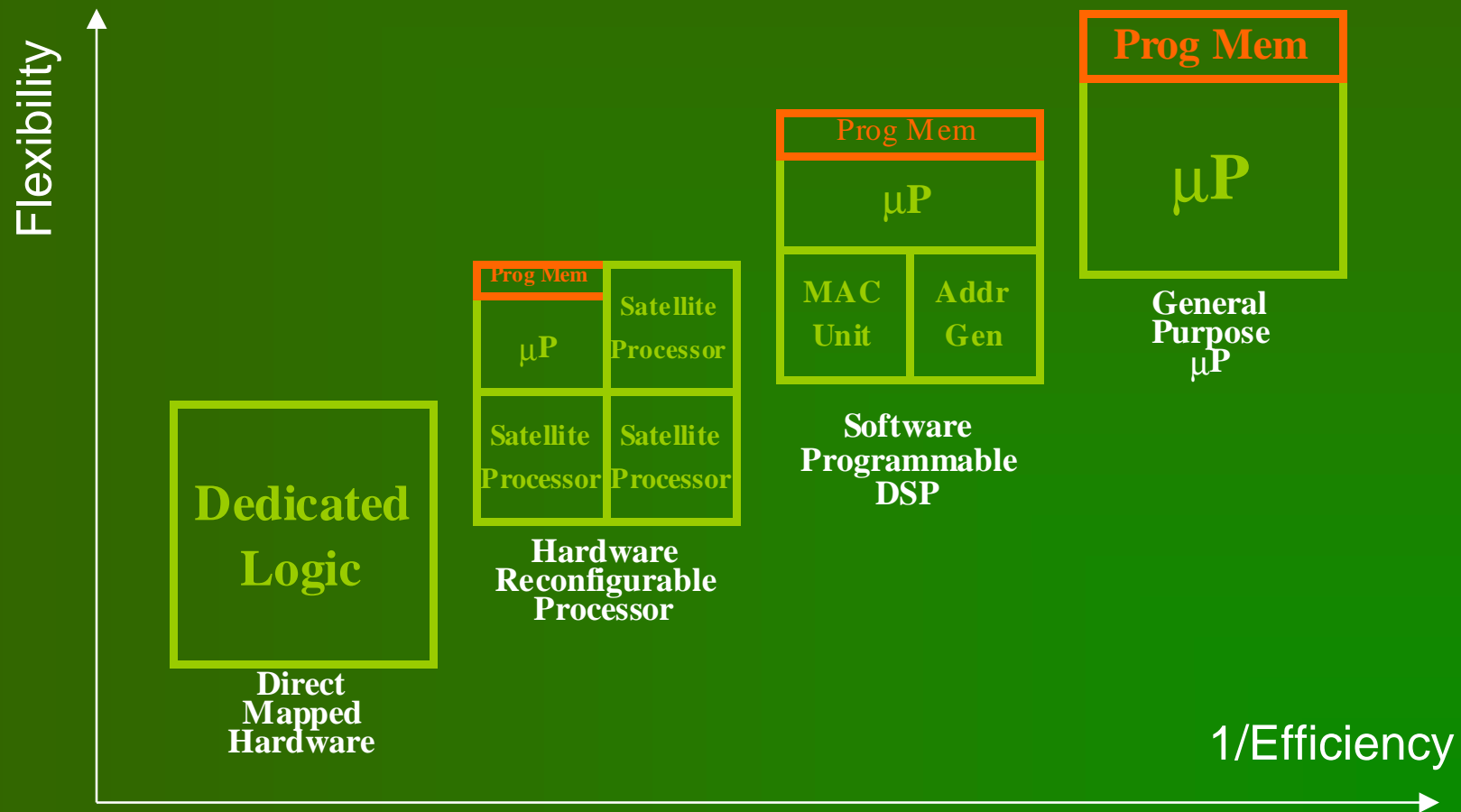


Source:
Alberto Sangiovanni-Vincentelli

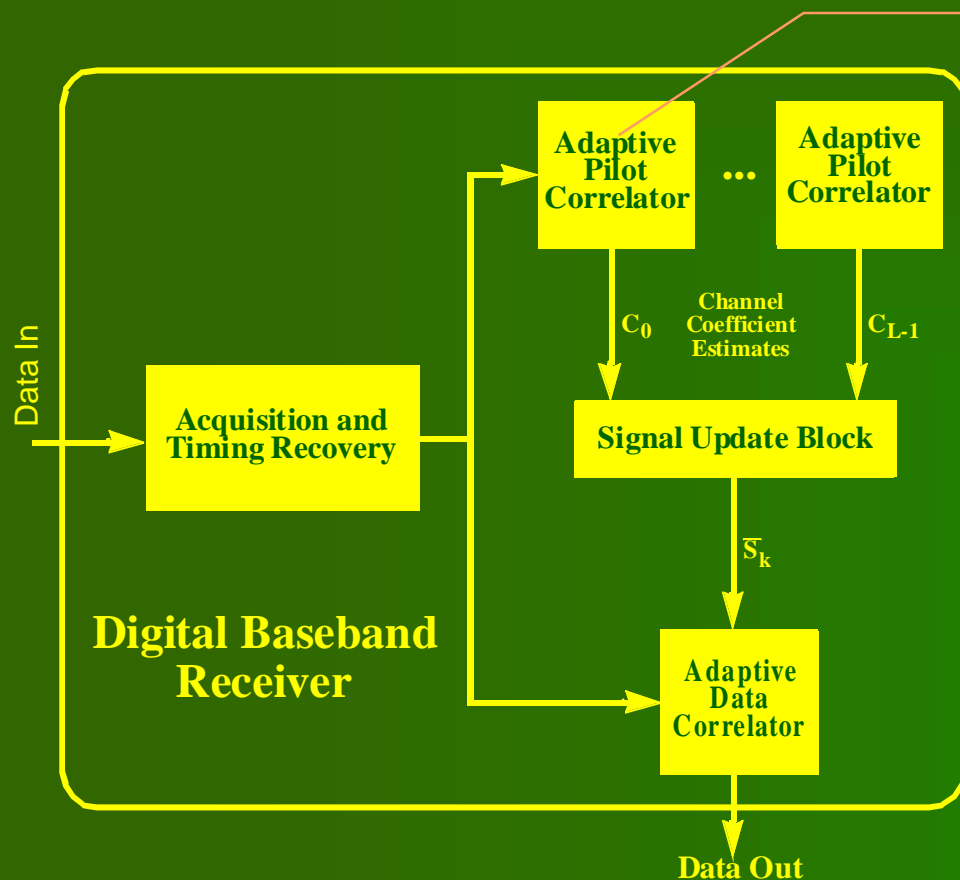
The Platform Approach



Architectural Choices



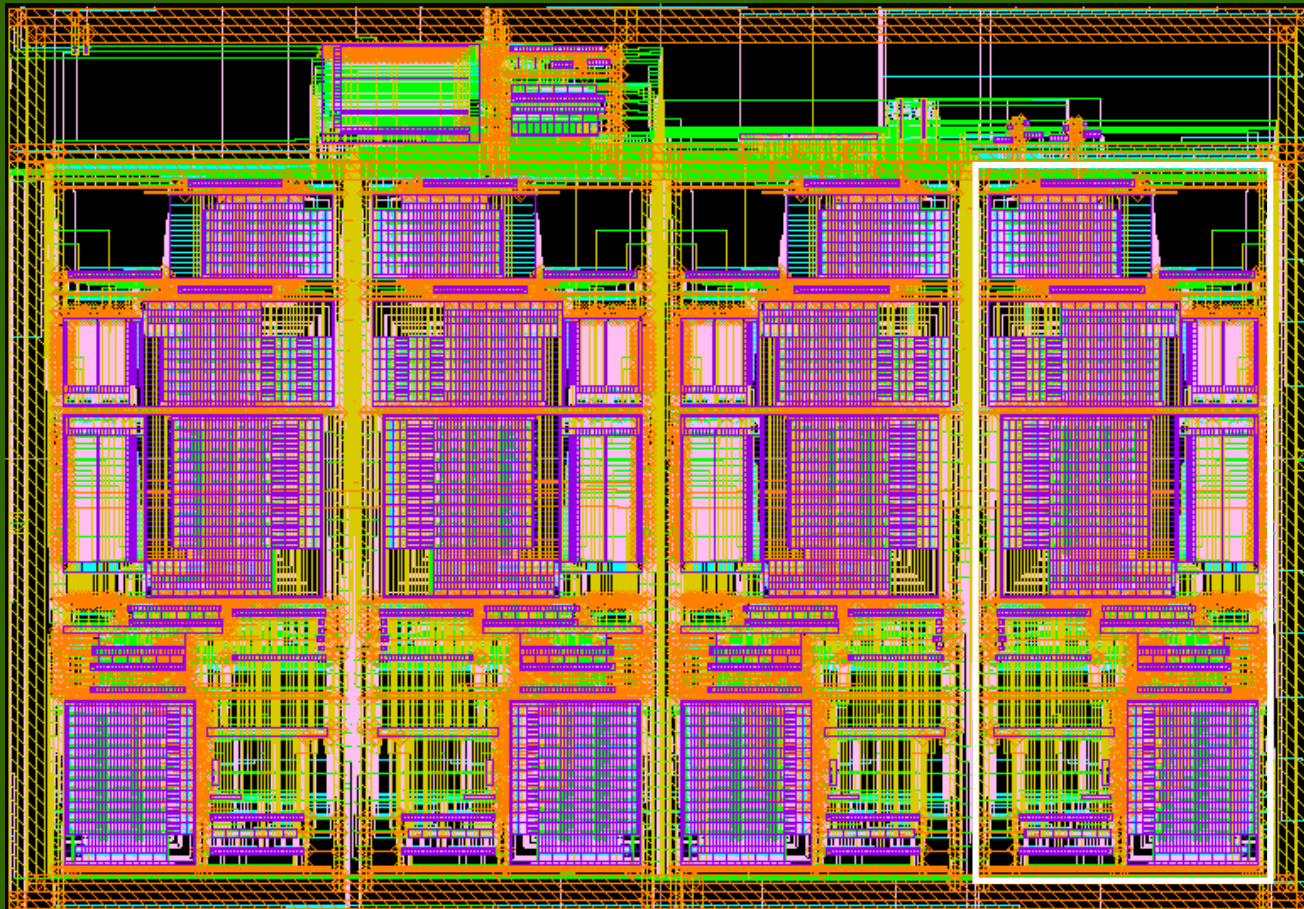
The Implementation Trade-off



300 million multiplications/sec
357 million add-sub's/sec

	DSP Implementation	Direct Mapped Implementation
Adaptive Pilot Correlator	Power Consumption: 460mW Area: 1089mm ²	Power Consumption: 3mW Area: 1.3mm ²
Digital Baseband Receiver	Power Consumption: 1500mW Area: 3600mm ²	Power Consumption: 10mW Area: 5mm ²

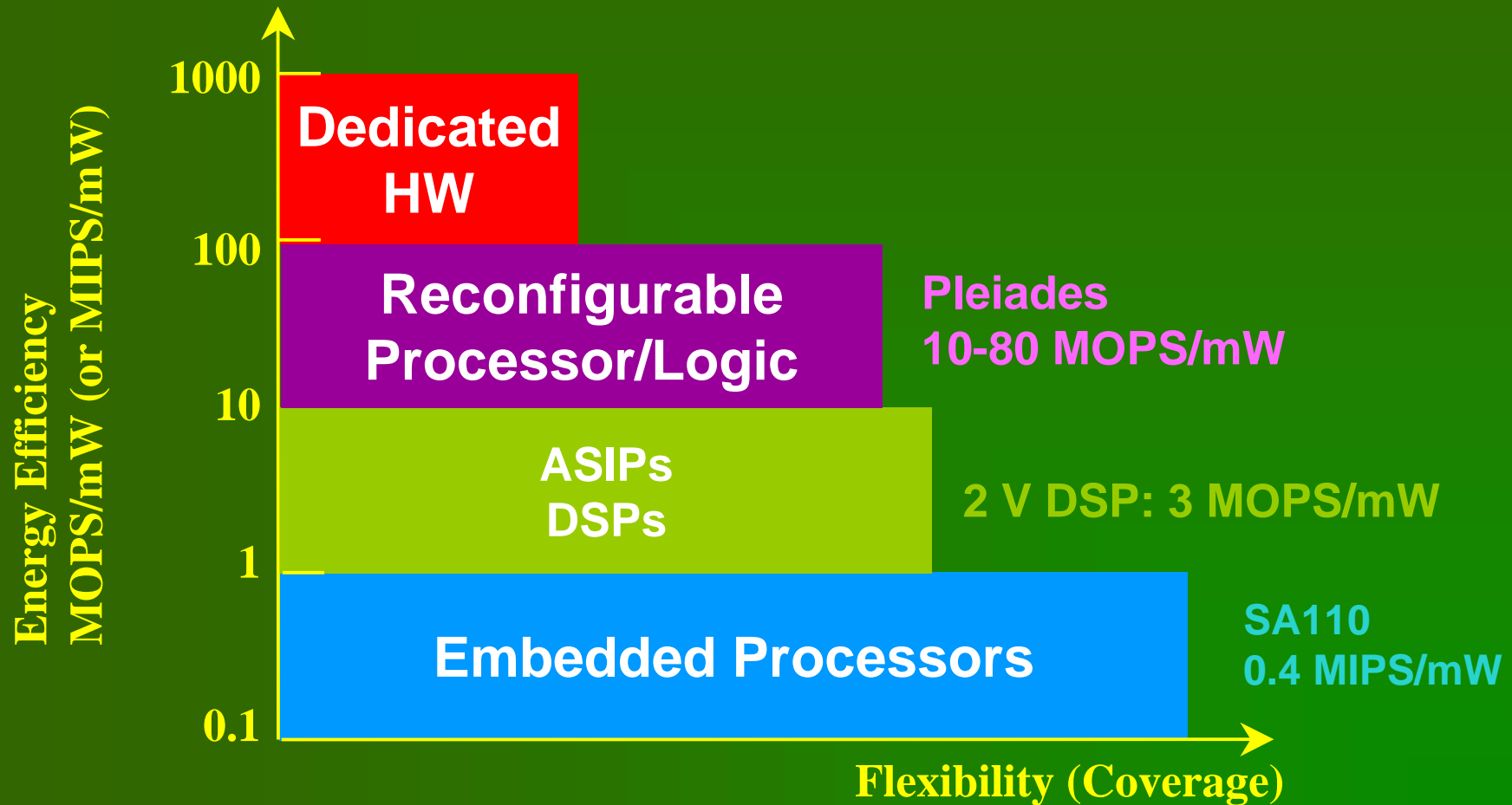
Adaptive Multi-User Detection A Direct Mapping Approach



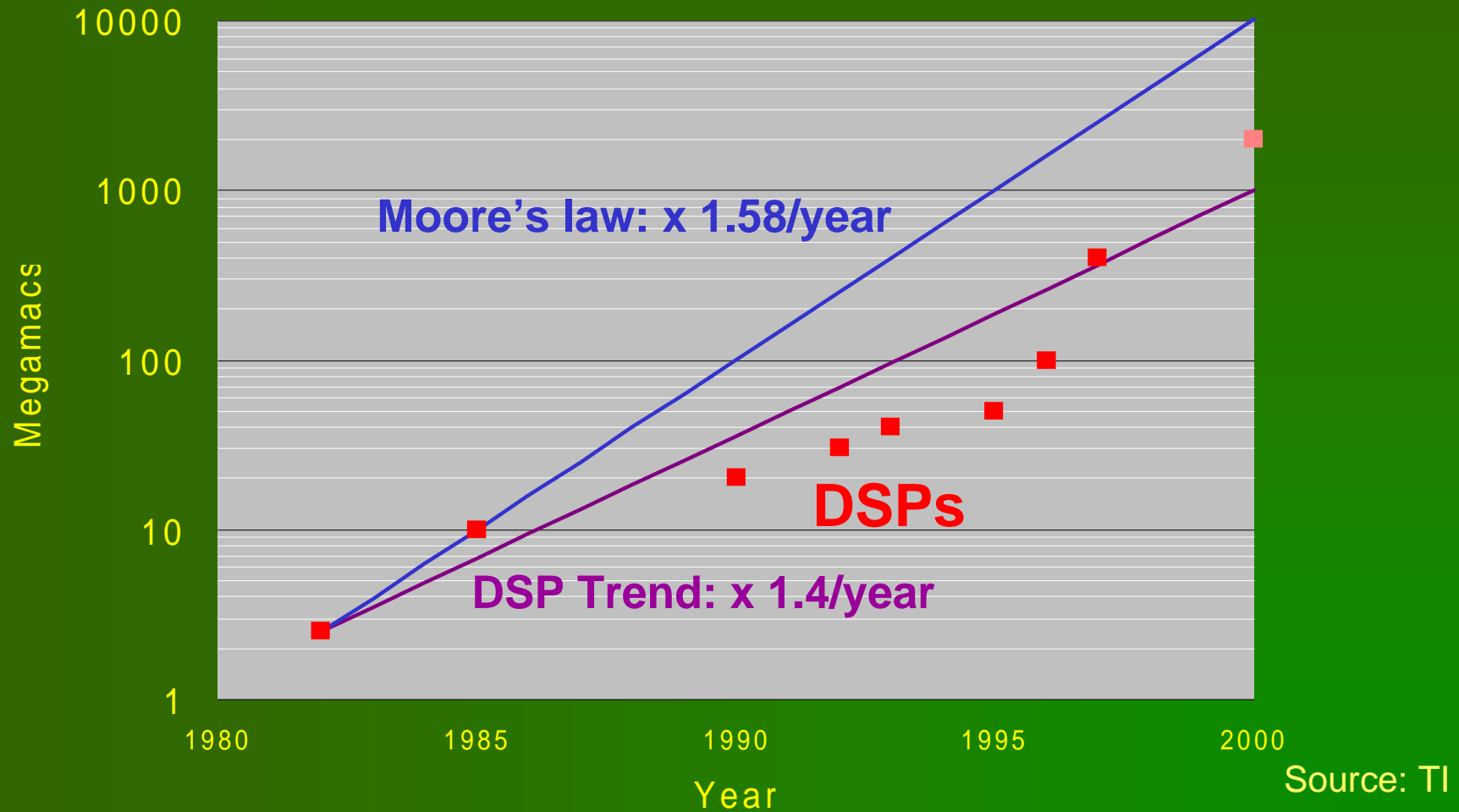
Correlator

Power and area are dominated by MACs and multiplies
Only 36% of power of DSP-processor solution going into arithmetic

The Energy-Flexibility Gap

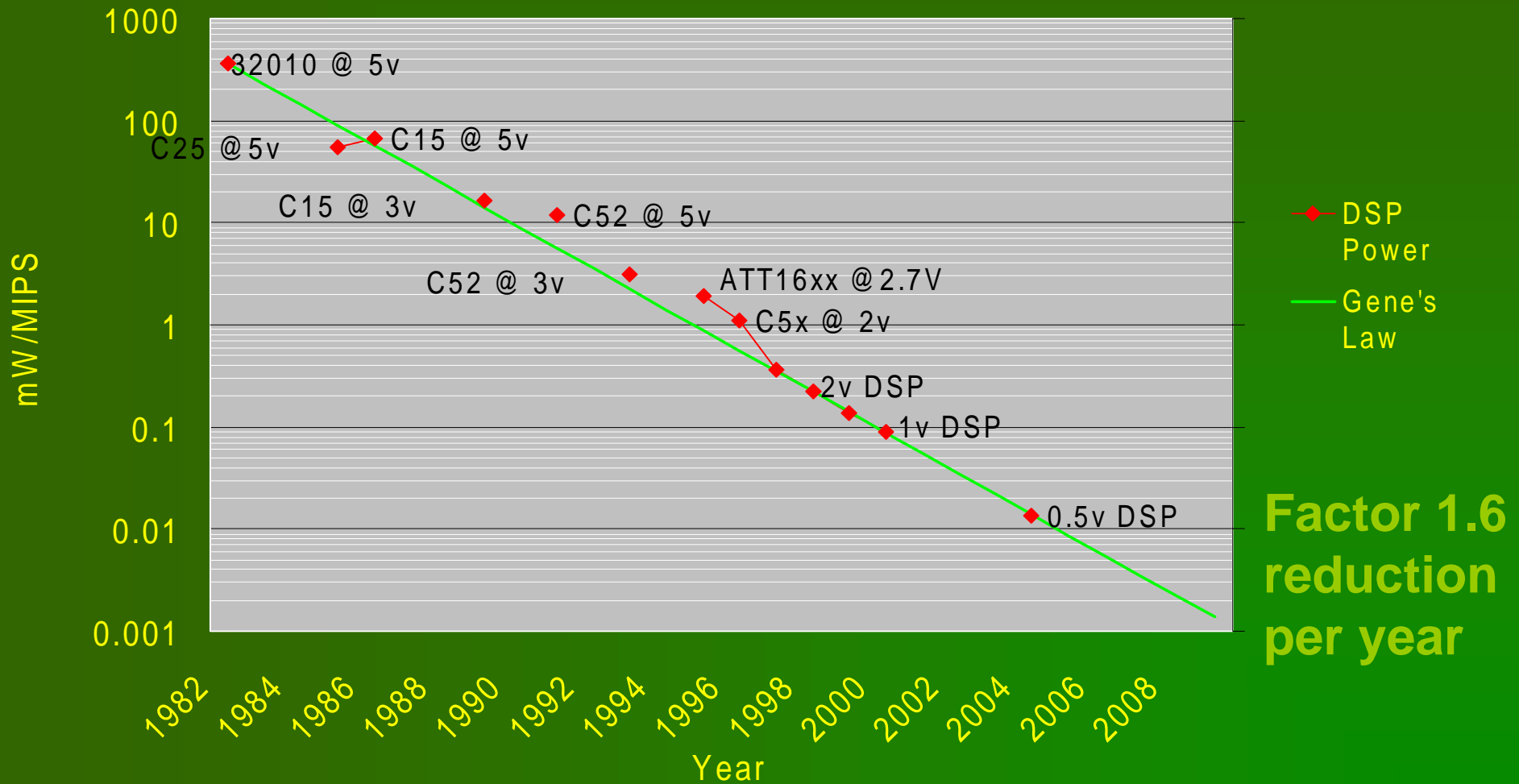


Single-Chip DSPs are Lagging ...



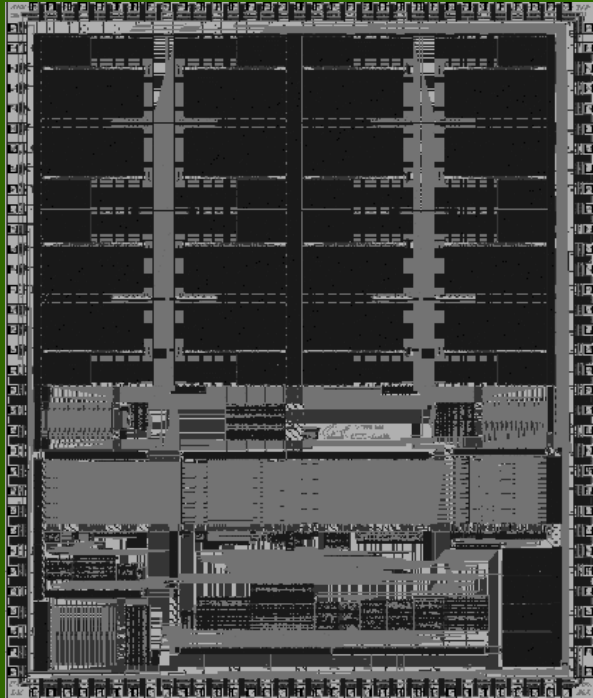
While algorithms are beating Moore's law!

Energy Trends in DSPs



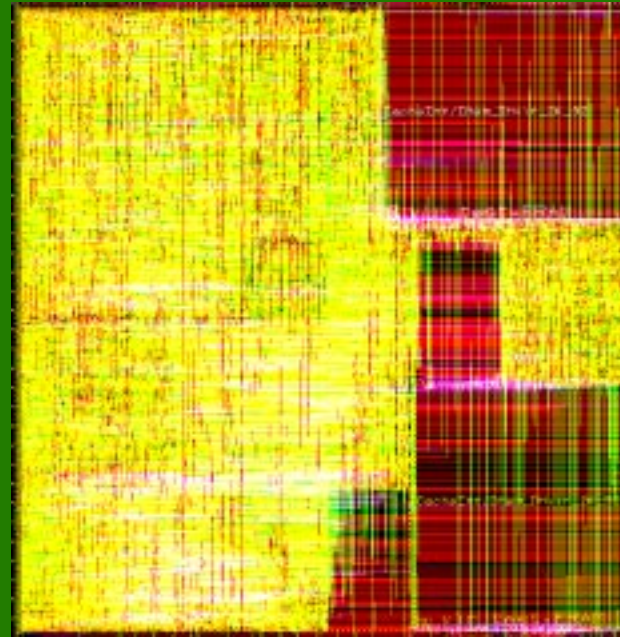
Source: TI

An Architectural Renaissance

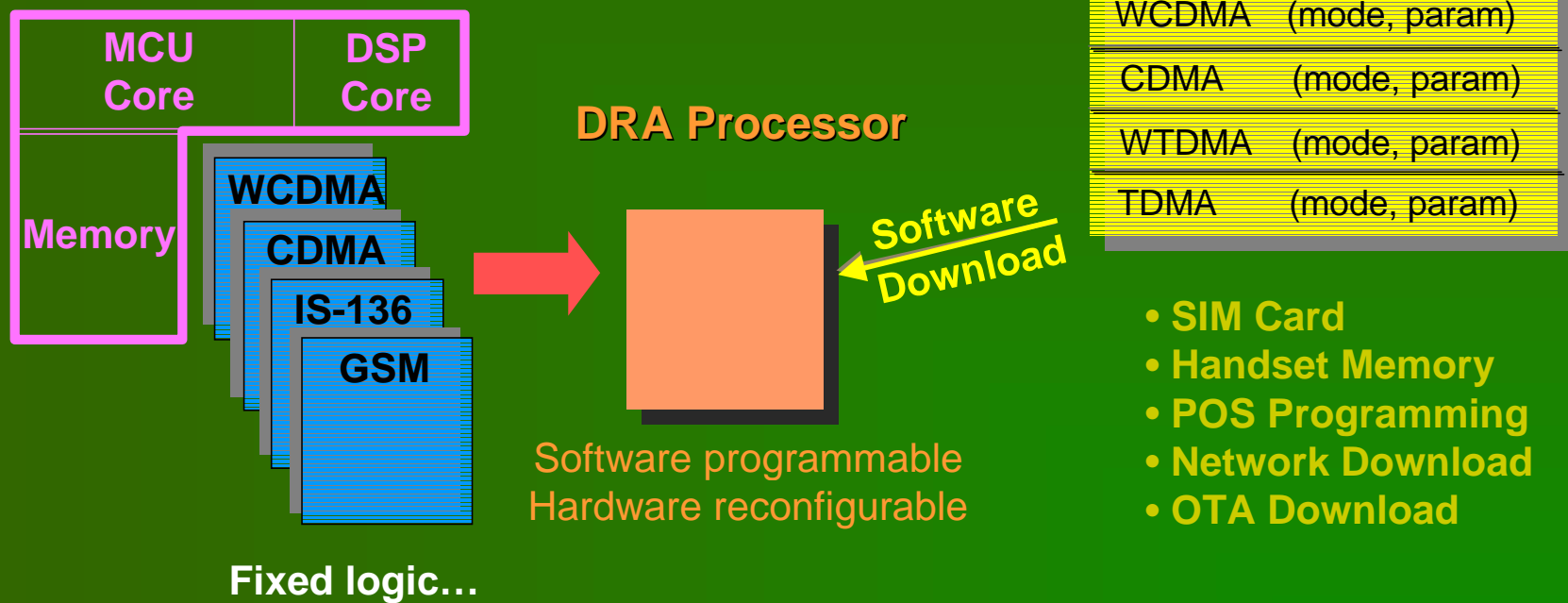


Embedded ARM-8
Microprocessor
(Hard IP)

Tensilica Synthesized and
Configurable μ Processor
(Soft IP)



An Architectural Renaissance

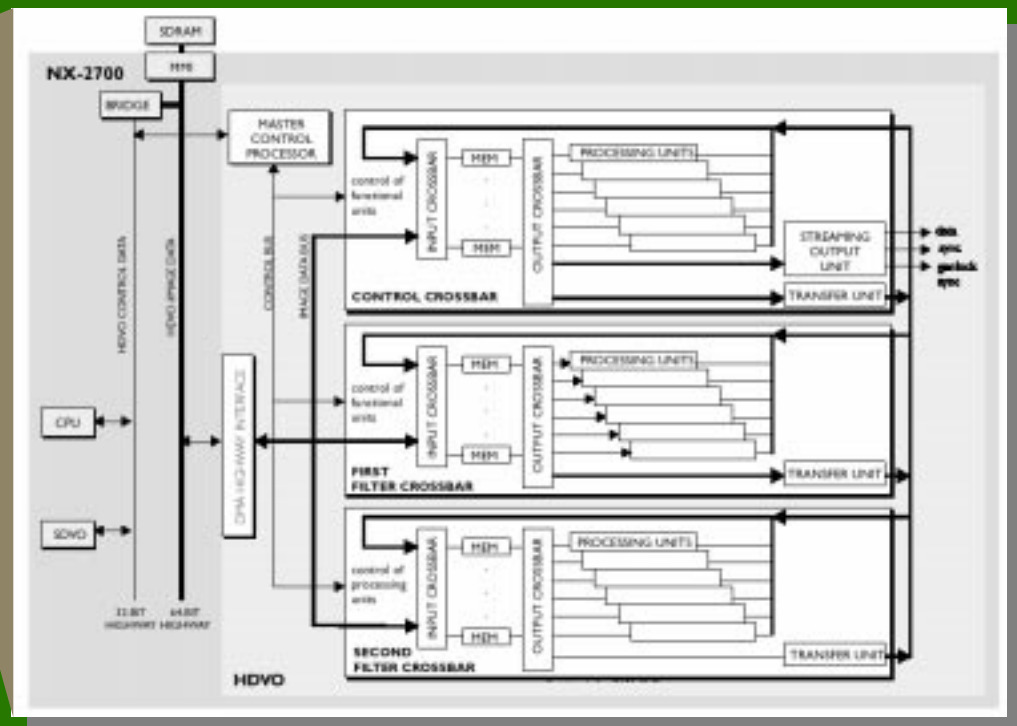
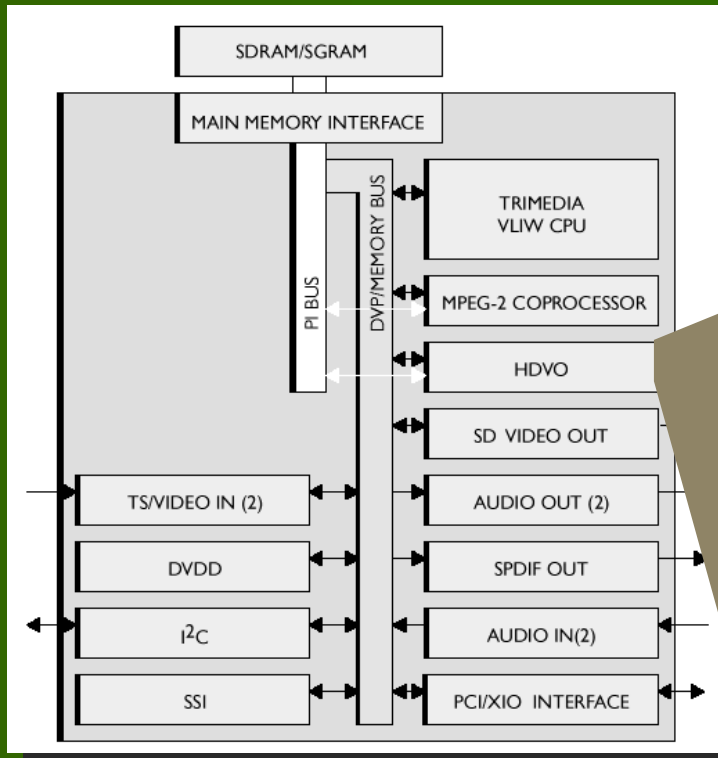


Realizes cost, size and power targets similar to traditional core+hardwired

MorphICs Dynamically Reconfigurable Architecture (DRA) Processor

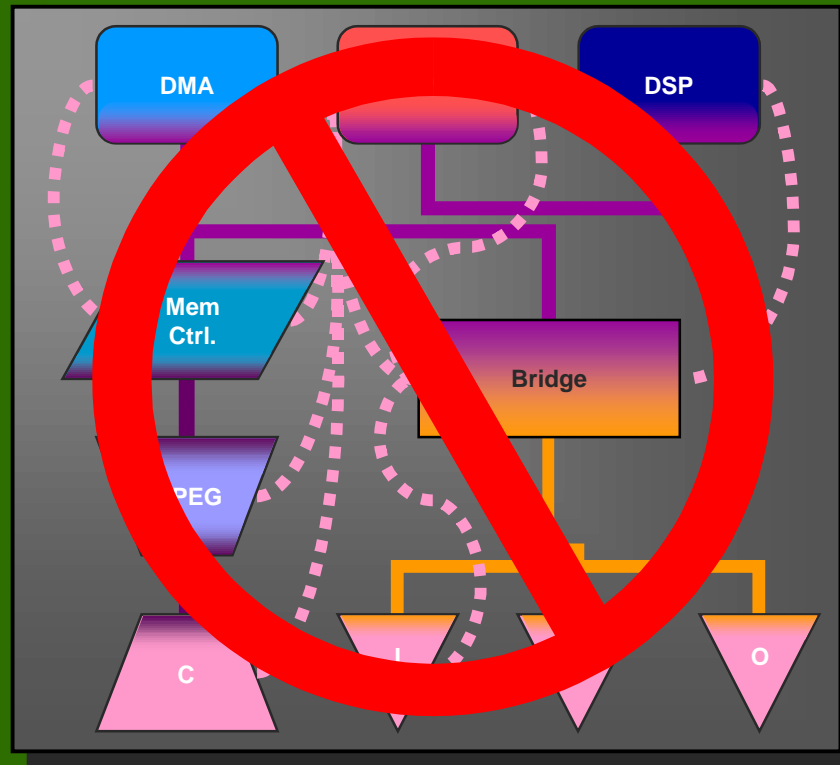
An Architectural Renaissance

Combines Trimedia VLIW with Configurable media co-processors



Philips Nexperia NX-2700
A programmable HDTV
media processor

Communication-Based Design

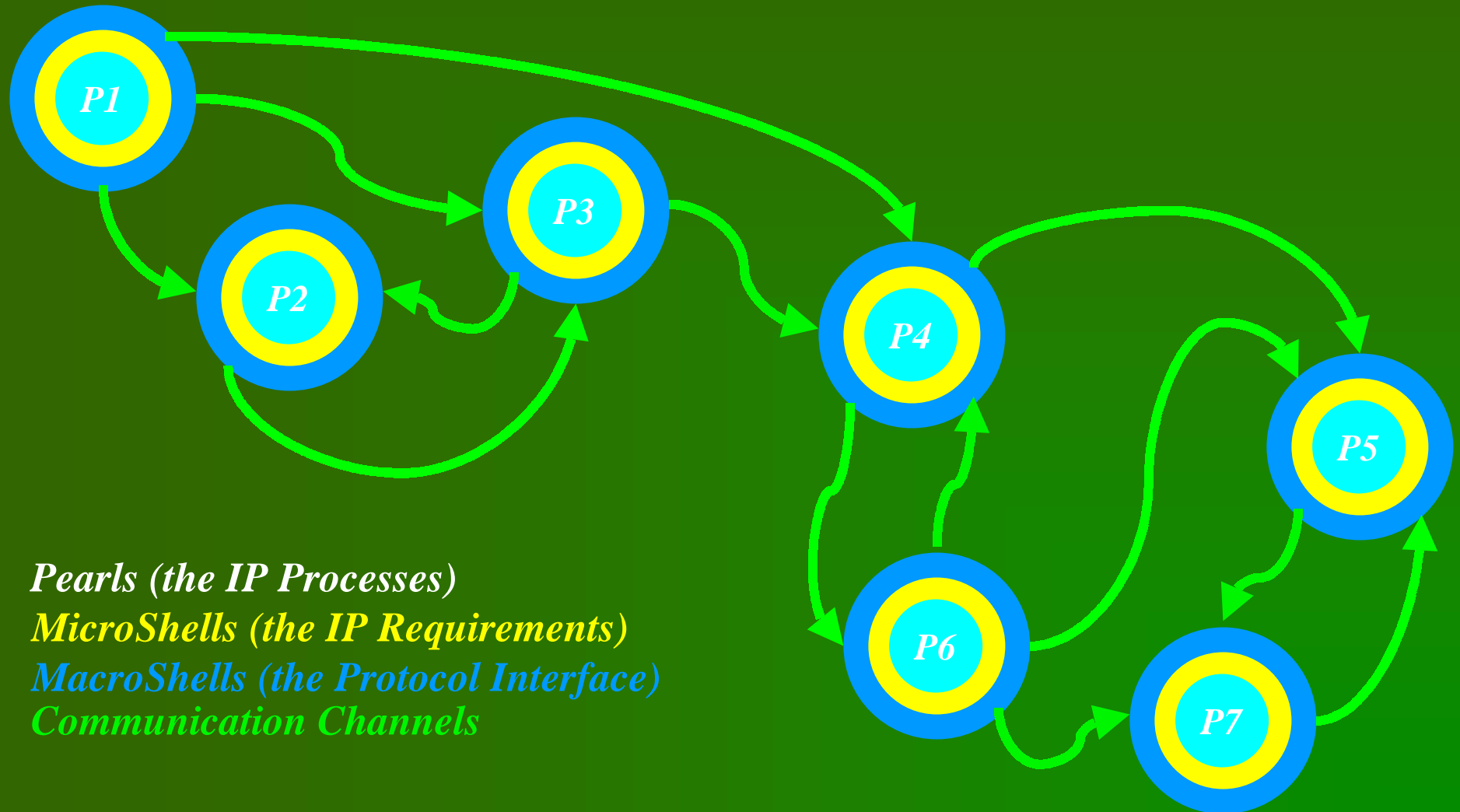


Orthogonalizing Communication from Behavior

- Historically lots of work on Behavior
 - hierarchy well established
 - several descriptions available (with variable levels of precision)
 - synthesis available
- Communication less well investigated
 - hard to separate from behavior, usually intertwined
 - telecomm protocols are the best existing example
- Need to understand Formalism, Abstraction, and Decomposition for communication

DEFINED BY MODELS OF COMPUTATION!

Communication-based Design



Pearls (the IP Processes)

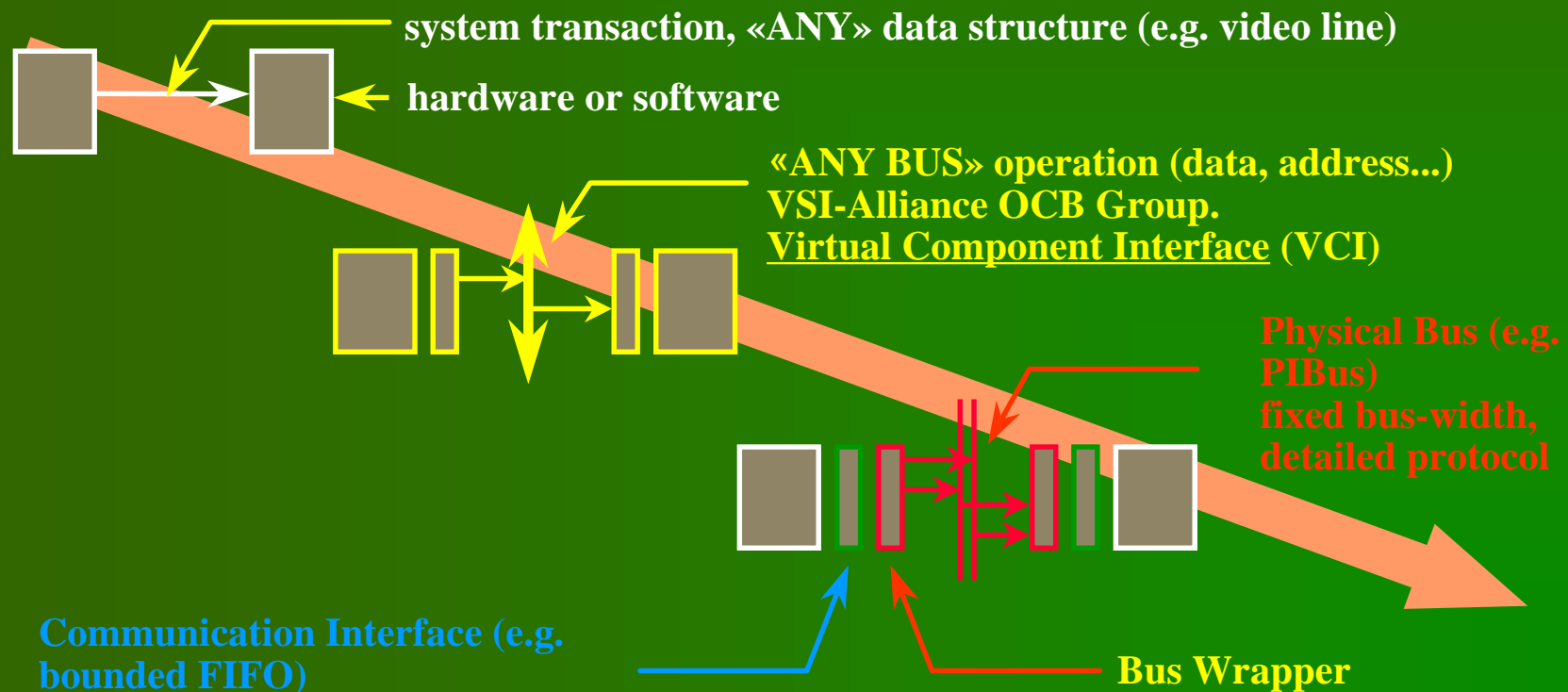
MicroShells (the IP Requirements)

MacroShells (the Protocol Interface)

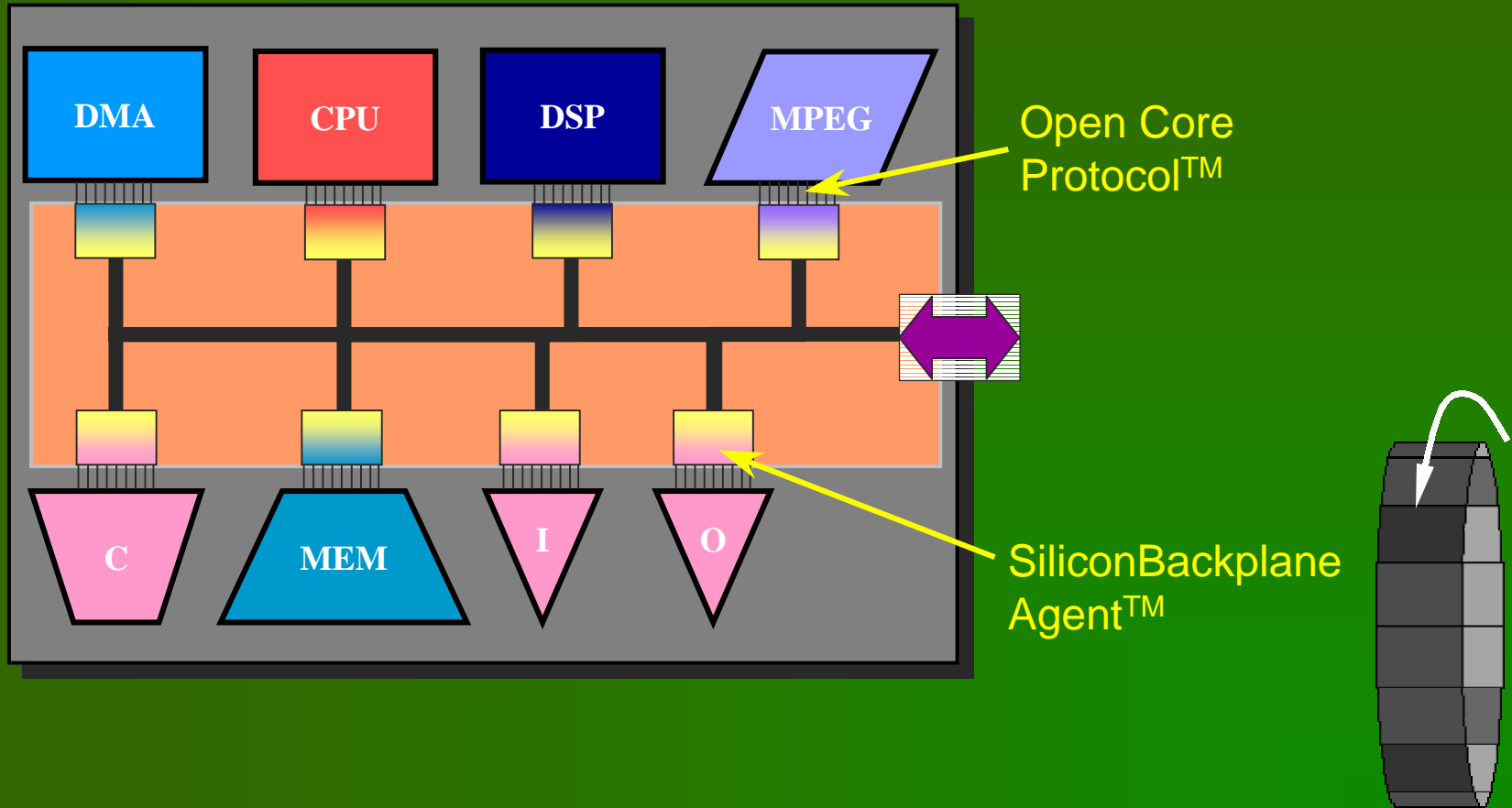
Communication Channels

Communication Refinement

Standard interfaces constitute the backbone of an IP market: abstract from the concerns of hardware implementation (multi-target VC), abstract from the concerns of a particular bus (bus-independent VC)



Communication-based Design

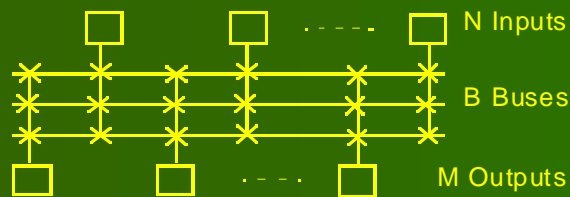


Example: “The Silicon Backplane”
(Sonics, Inc)

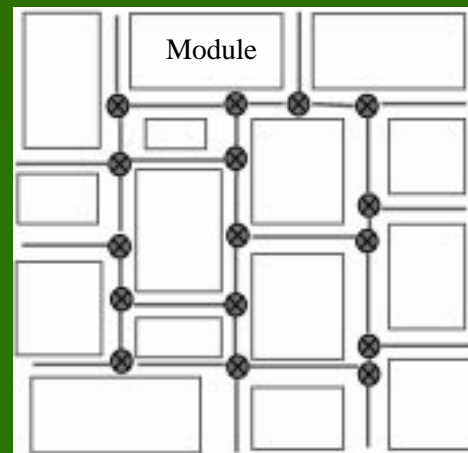
Guaranteed Bandwidth
Arbitration

Interconnect-on-a-Chip

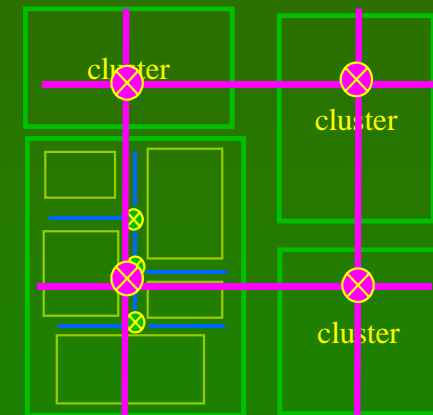
Multi-Bus



Mesh



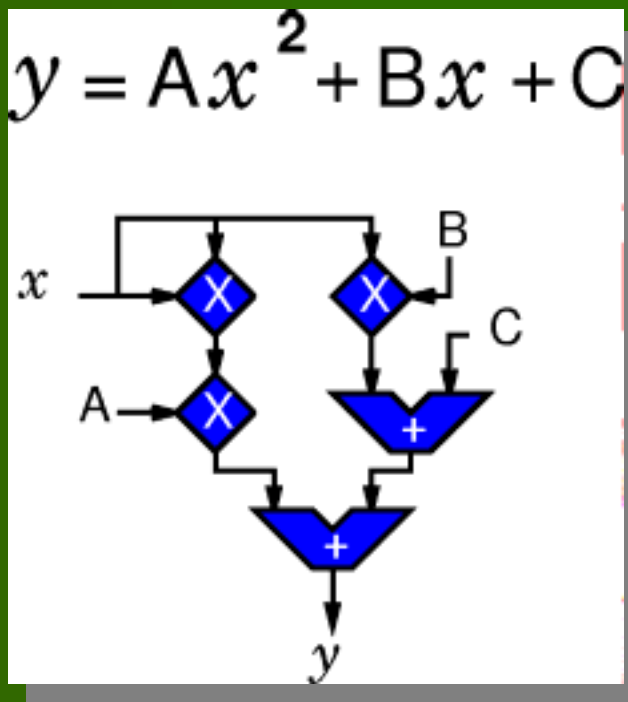
Hierarchical Mesh



		dot_product	vector sum w/ scalar mult.	IIR
Multi-bus		50	50	138
Mesh	<i>Best</i>	8.7	5.2	24.6
	<i>Worst</i>	17.7	14.7	43.4
H. Mesh	<i>Best</i>	4.7	3.8	18.8
	<i>Worst</i>	11.1	10.2	31.3

Reconfigurable Computing: Merging Efficiency and Versatility

Spatially programmed connection of processing elements.



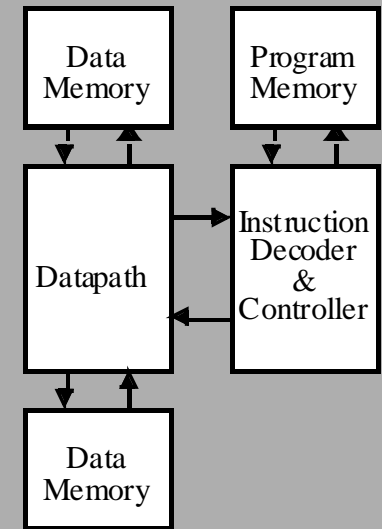
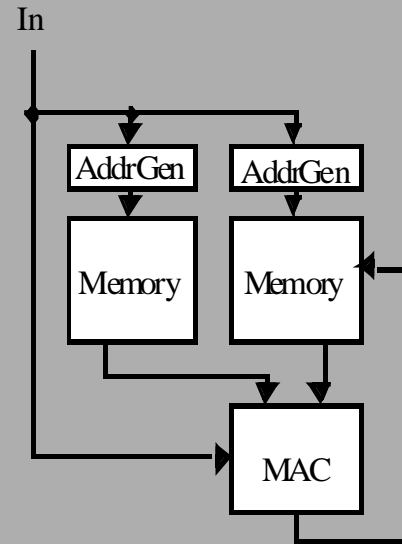
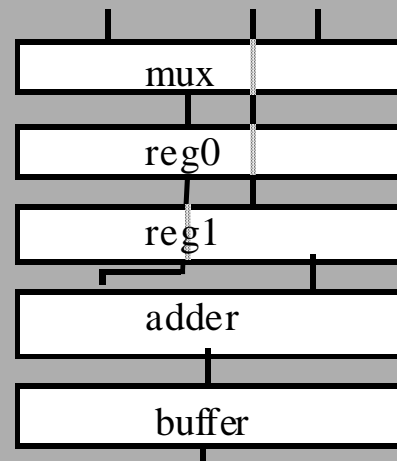
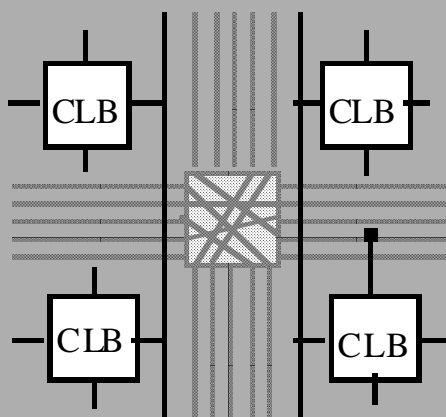
“Hardware” customized to specifics of problem.

Direct map of problem specific dataflow, control.

Circuits “adapted” as problem requirements change.

A New Look at Architectures — Heterogeneous Reconfiguration

Reconfigurable Logic Reconfigurable Datapaths Reconfigurable Arithmetic Reconfigurable Control



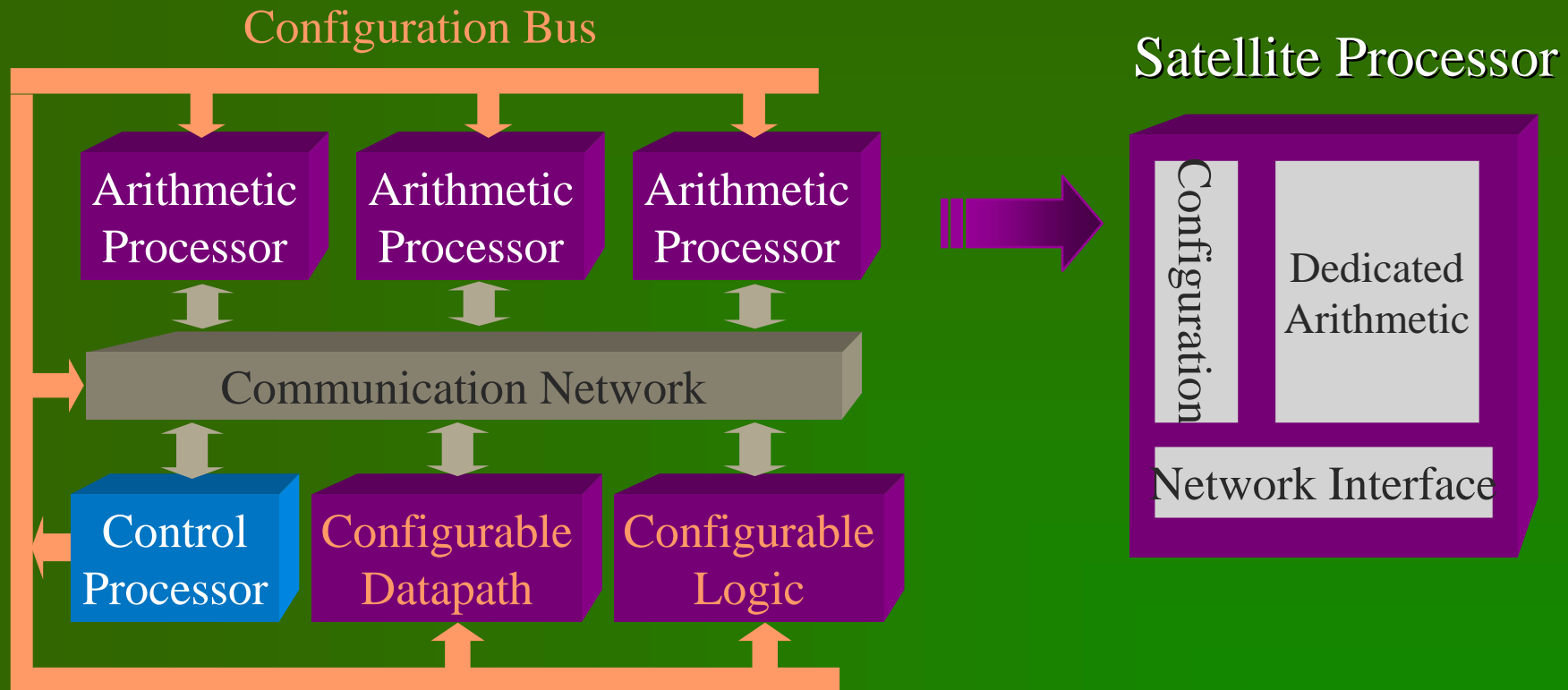
Bit-Level Operations
e.g. encoding

Dedicated data paths
e.g. Filters, AGU

Arithmetic kernels
e.g. Convolution

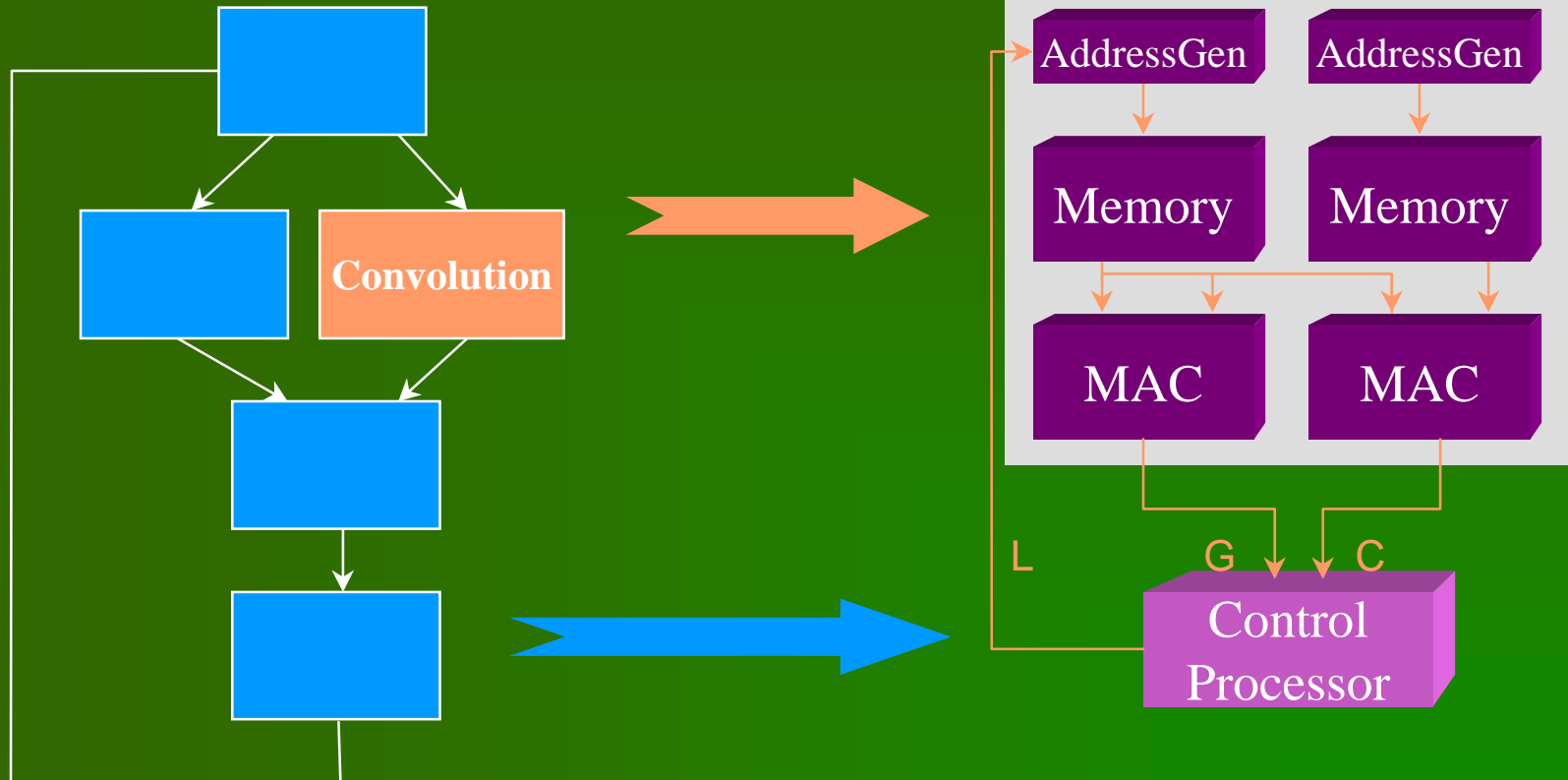
RTOS
Process management

Multi-granularity Reconfigurable Architecture: The Berkeley Pleiades Architecture



- Computational kernels are “spawned” to **satellite processors**
- Control processor supports RTOS and reconfiguration
- Order(s) of magnitude energy-reduction over traditional programmable architectures

Matching Computation and Architecture

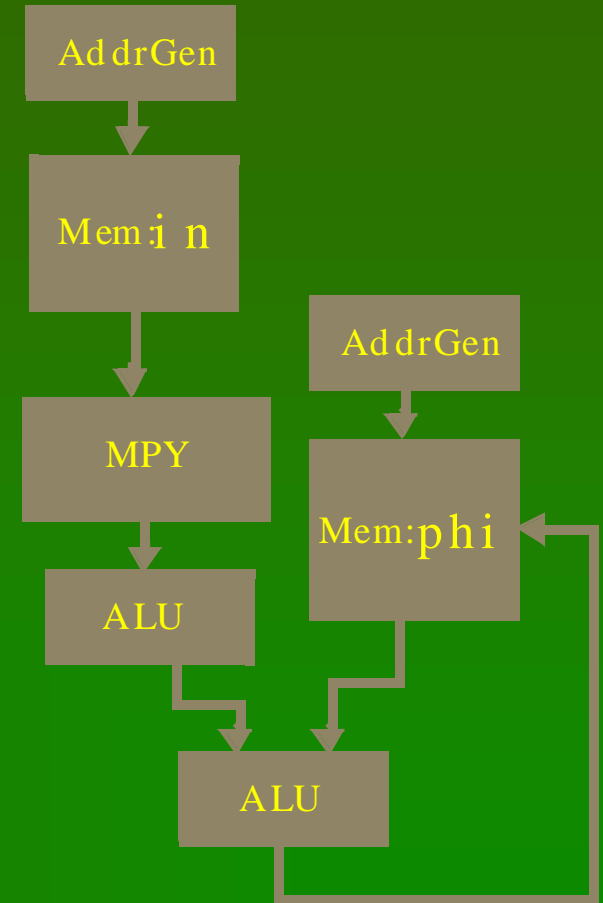


Two models of computation:
communicating processes + data-flow

Two architectural models:
sequential control+ data-driven

Example: Covariance Matrix Computation

```
for (i=1; i<=length; i++) {  
  for (k=i; k<=length; k++) {  
    phi[i][k] = phi[i-1][k-1] +  
      in[NP-i]*in[NP-k] -  
      in[NA-1-i]*in[NA-1-k];  
  }  
}
```



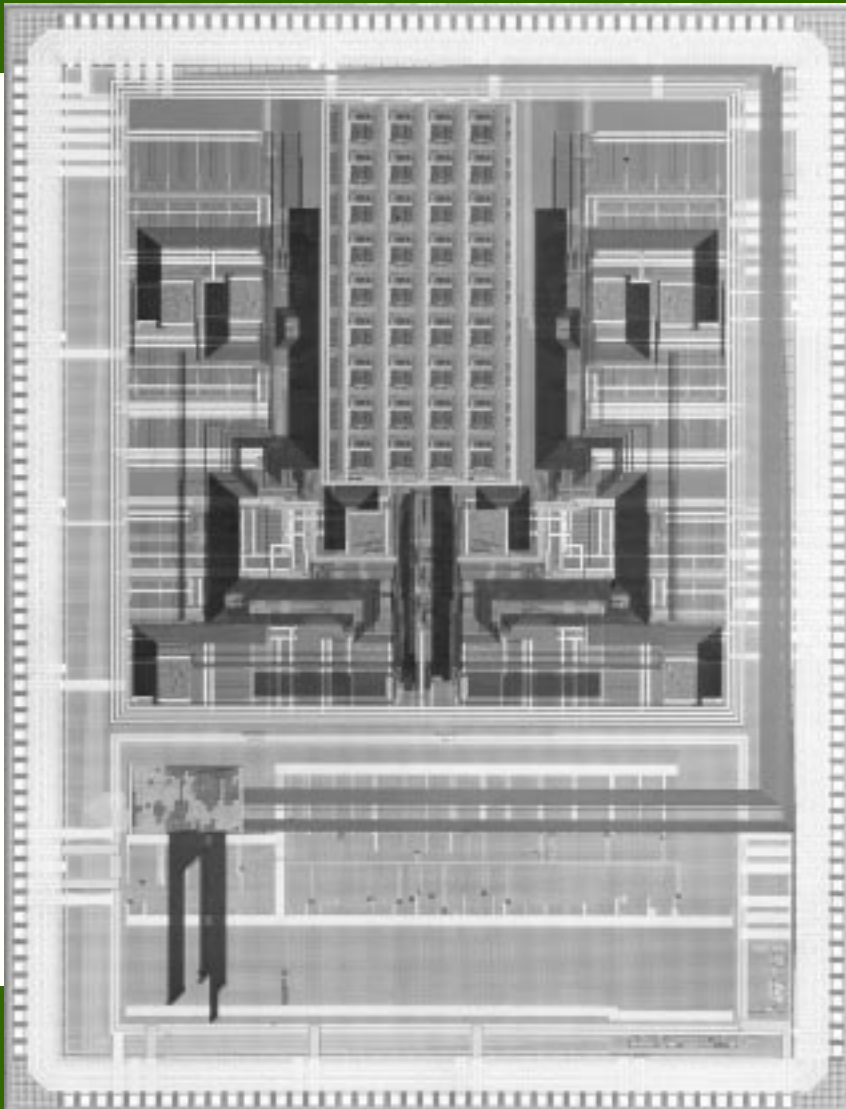
Architecture Comparison

**LMS Correlator at 1.67 MSymbols Data Rate
Complexity: 300 Mmult/sec and 357 Macc/sec**

Type	Power	Area
TMS320C54*	460 mW	1089 mm ²
Pleiades	18.09 mW	5.448 mm ²
ASIC [Zhang]	3 mW	1.5 mm ²

Note: TMS implementation requires 36 parallel processors to meet data rate -
validity questionable

Maia: Reconfigurable Baseband Processor for Wireless



- 0.25um tech: 4.5mm x 6mm
- 1.2 Million transistors
- 40 MHz at 1V
- 1 mW VCELP voice coder
- Hardware
 - 1 ARM-8
 - 8 SRAMs & 8 AGPs
 - 2 MACs
 - 2 ALUs
 - 2 In-Ports and 2 Out-Ports
 - 14x8 FPGA

Protocol Implementation Challenges

TDMA Link and MAC
alternative implementations

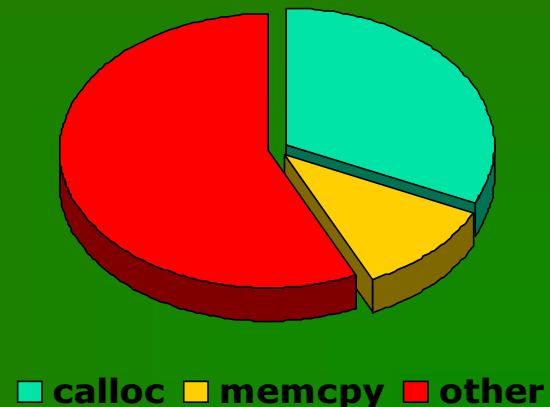
	ASIC	FPGA	ARM8
Power	0.26mW	2.1mW	<i>114mW</i>
Energy	10.2pJ/op	81.4pJ/op	<i>n*457pJ/op</i>

Intercom transport and application
layers on Xtensa processor

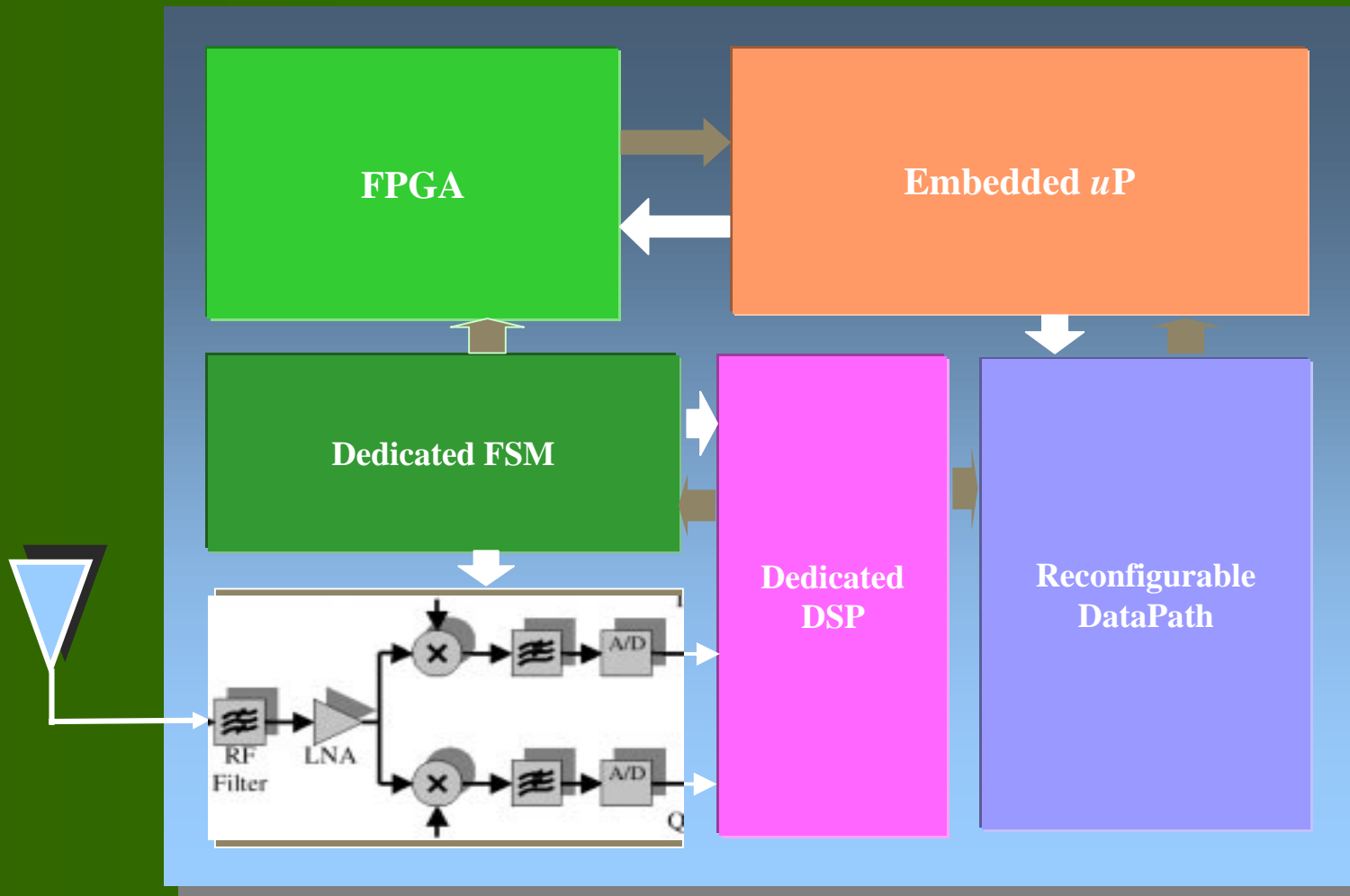
Observations

- Tremendous opportunity for optimization at description and implementation level
- Model of Computation: CFSM
- Major differentiation in functionality between different levels of stack

Total Execution Time



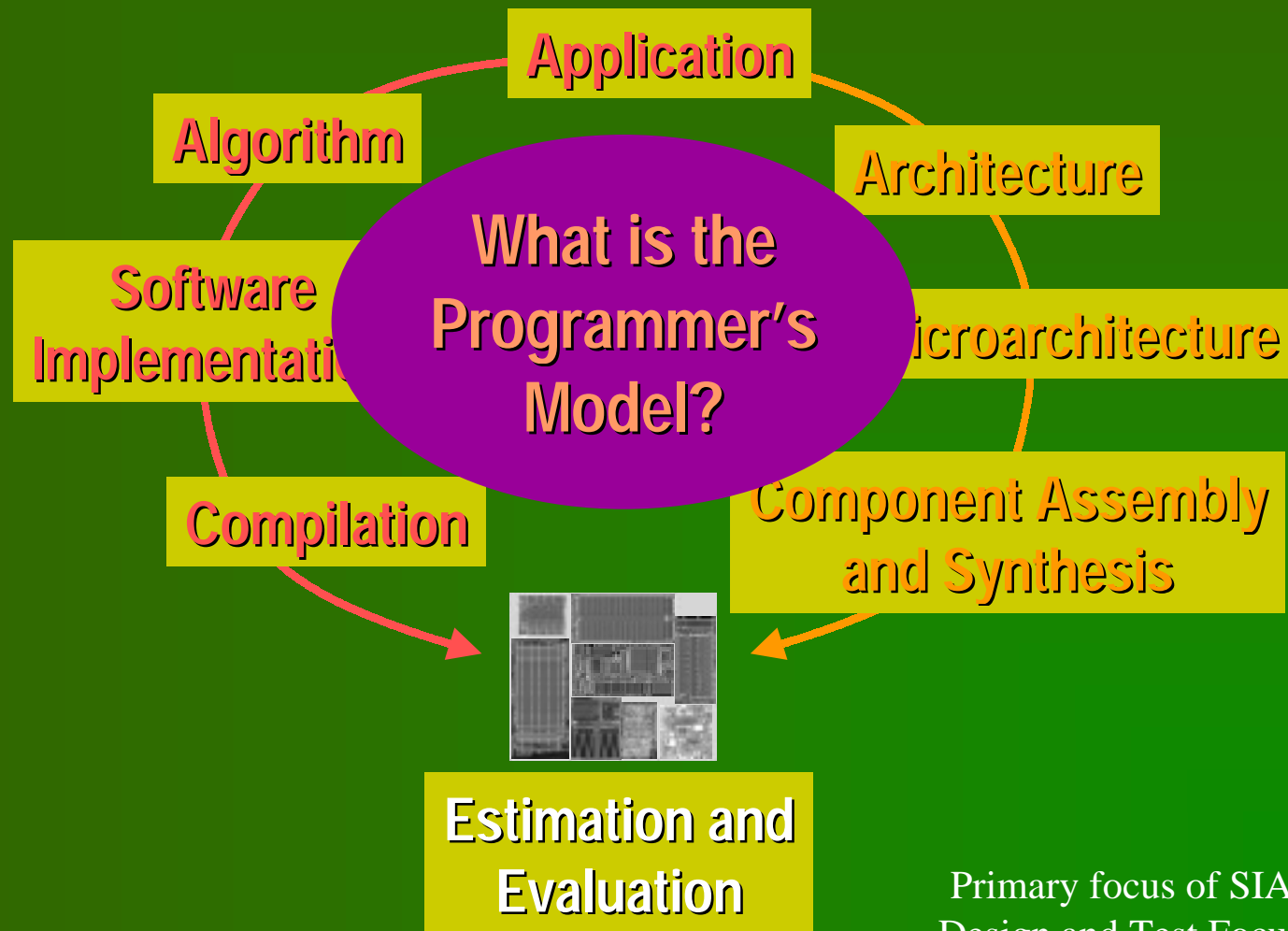
The Software-Defined Radio



Summary and Perspective

- Technology scaling is redefining the term “complexity”
- System-on-a-Chip fosters renaissance in processor architecture, opening the door for new models and combinations thereof:
Component and Communication Based Design
- SOC for wireless driven by new set of metrics: how to simultaneously optimize **flexibility, cost, energy, and performance?**
- **Reconfigurable architectures** provide tantalizing combination of flexibility and efficiency
- Numerous solutions for addressing the data-intensive component of the software-defined radio — **the next challenge is control**

Programming the Platform



Primary focus of SIA GSRC
Design and Test Focus Center