

System-on-a-Chip – A Platform Perspective

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Emerging Societal-Scale Systems

Courtesy: R. Katz, UCB

The 1990s:
Conquering the world
The network revolution

The 2000s:
Extending toward the Small
Enabled by integration
(Moore's Law at Work!)
and wireless connectivity



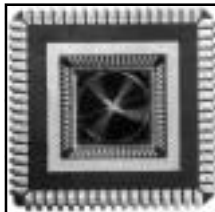
Pre-1990:
Client-Server Systems



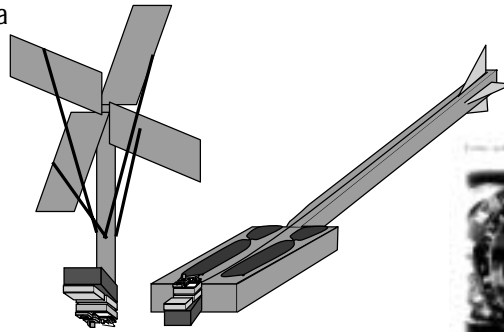
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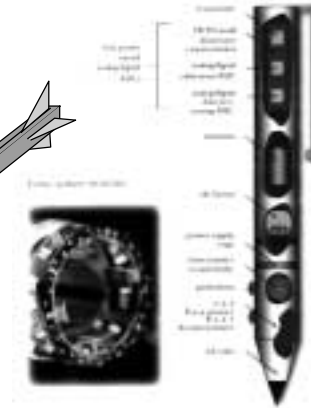
Moore's law in 20xx: The Ubiquitous Chip



CMOS Camera

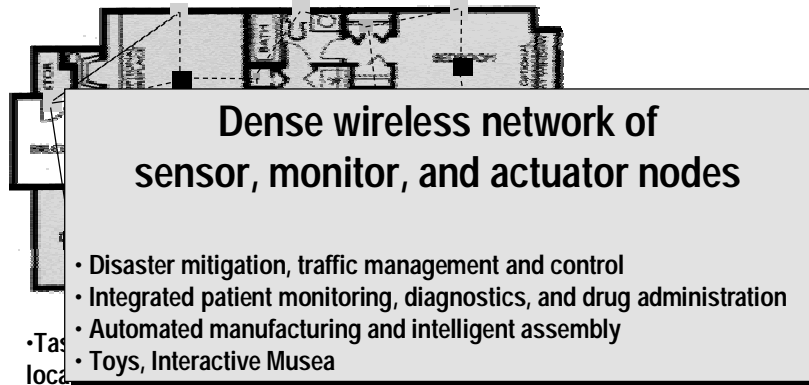


Chips that walk or fly??



SmartPen

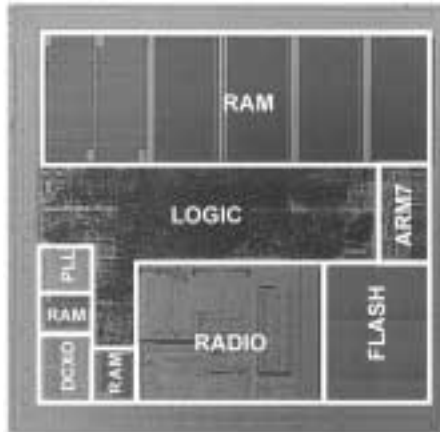
Intelligent Buildings



• Tax local
"micro-climates within a building"

• Other functions: energy management, security, identification and personalization, object tagging, seismic monitoring

The Opportunity: System-on-a-Chip (SOC)



Example: Single-Chip
Bluetooth Radio
(Alcatel, ISSCC2001)

The Challenge

Facts

- Complexity per Design Start is going up
- NRE per Design is increasing
- Total Number of Design Starts will decrease

Shift to

- Reuse Strategy
- Higher Level of Abstractions
- Software !!!

microelectronics group

SoC Landscape 2000+

- Cost of ownership is High
 - Development cost of a high end ASSP can exceed \$5M
 - Cost of fabrication and mask making has increased significantly (\$500k+ for masks alone)
 - = 15x design productivity gap (Spec to Verified Netlist)
- Compounding complexities limiting Time-to-Market, cycle time reduction needed to meet Customer expectations
 - Chip design complexity
 - Silicon process complexity
 - Circuit complexity
 - End-to-end verification
- New "System to Silicon" methodologies are required that recognize > 50% of the system development is software

Lucent Technologies
INTELLECTUAL PROPERTY

Source: Mark Pinto, CTO, Agere

The System-on-a-Chip Nightmare

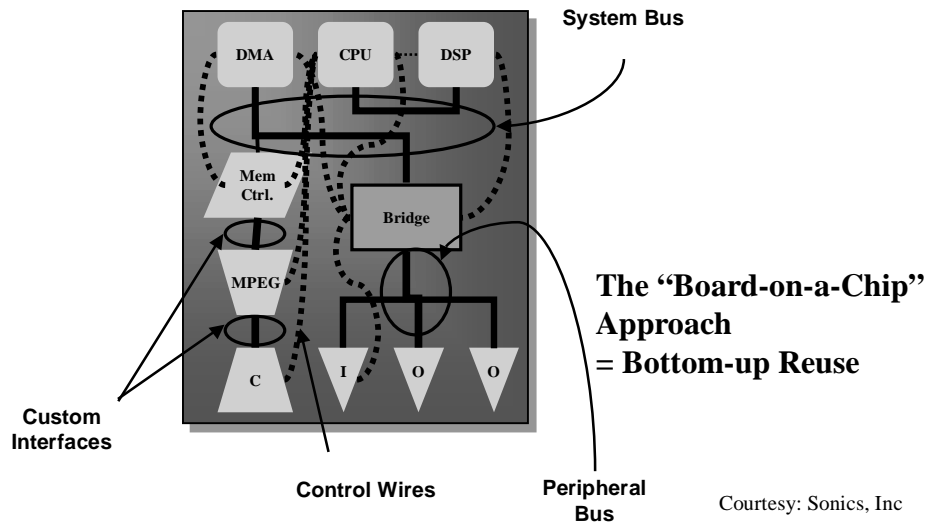


“Femme se coiffant”
Pablo Ruiz Picasso
1940

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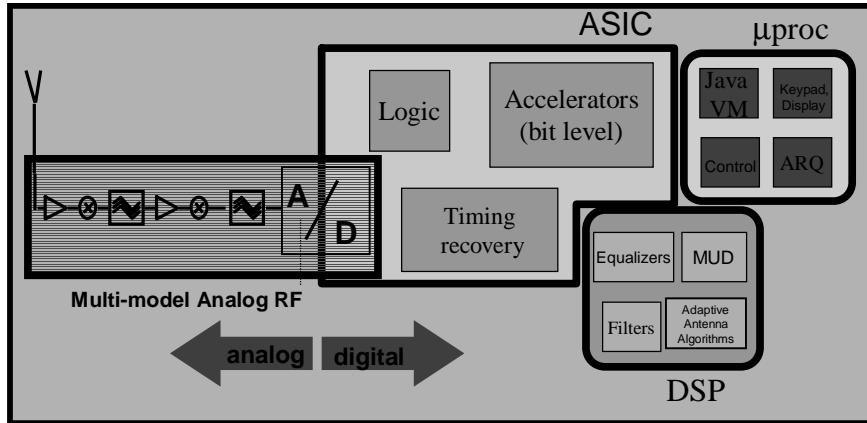
The System-on-a-Chip Nightmare



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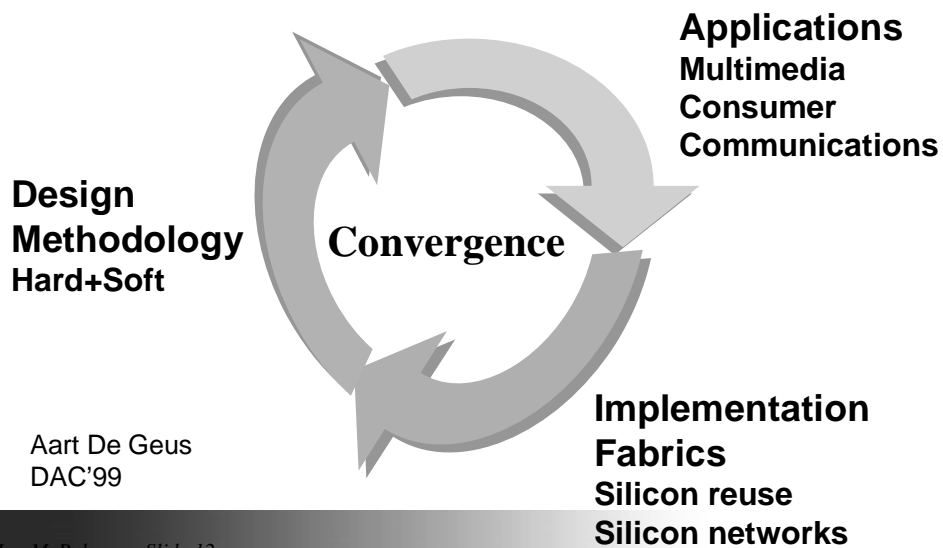
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Current Integrated Wireless Transceivers



A "Board-on-a-Chip" Approach

System-on-a-Chip A Renaissance in Design



Aart De Geus
DAC'99

A Central Theme: Raising the Reuse Factor

Reuse comes in generations

| <i>Generation</i> | <i>Reuse element</i> | <i>Status</i> |
|-----------------------|----------------------|------------------|
| <i>1st</i> | Standard cells | Well established |
| <i>2nd</i> | IP blocks | Being introduced |
| <i>3rd</i> | Architecture | Emerging |
| <i>4th</i> | IC | Early research |

Source: Theo Claasen (Philips) – DAC 00

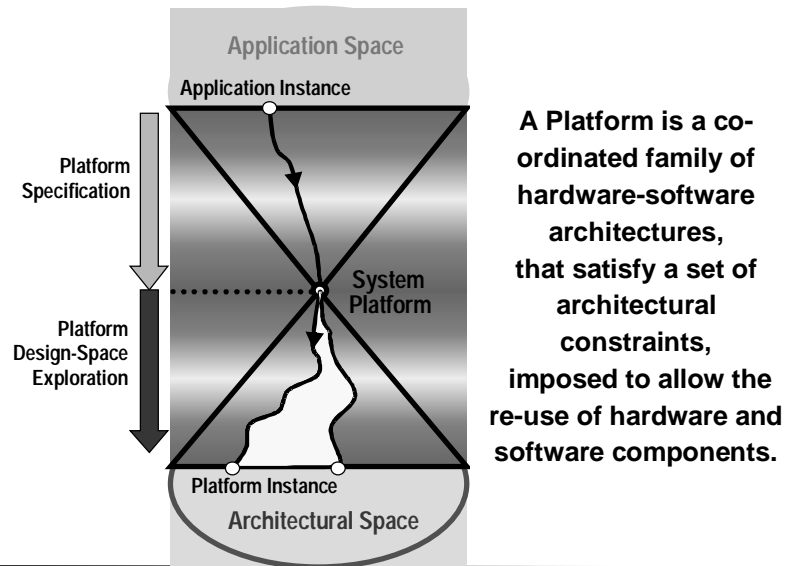
A Hardware Platform

Not a fully specified SoC, but also *a family of architectures that share some common features*
= Architecture Re-use

A Hardware Platform is a family of architectures that satisfy a set of architectural constraints, imposed to allow the re-use of hardware and software components.

The stronger the constraints the more component re-use
but stronger constraints imply fewer architectures to choose from!

The Platform Concept

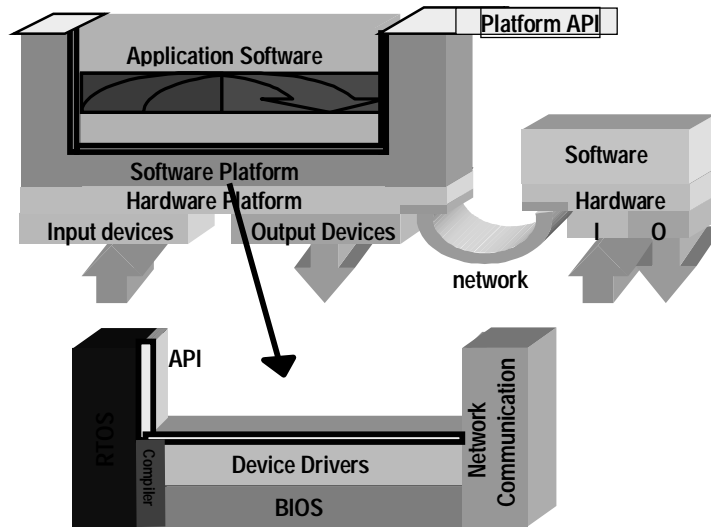


A Platform is a coordinated family of hardware-software architectures, that satisfy a set of architectural constraints, imposed to allow the re-use of hardware and software components.

Hardware Platforms Not Enough!

- Hardware platform has to be abstracted
- Interface to the application software is the “API”
- Software layer performs abstraction:
 - Programmable cores and memory subsystem “hidden” by RTOS and compilers
 - I/O subsystem with Device Drivers
 - Network with Network Communication Software

A Software-Centric View of Platforms



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A Successful System Platform The PC

- Flexible architecture for hardware (x86) and software
- Specific (programmable) components
- Network architecture
- Software modules
- Rules and guidelines for design of HW and SW

Dominated by a few players who specify and control architecture

But Application-Specific SOC Platforms are Harder!

- Cost
- Size
- Real / non-real time data constraints
- Power/energy dissipation

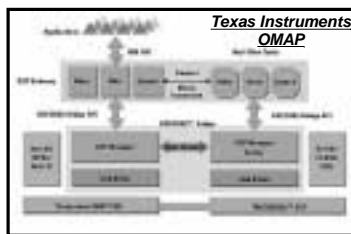
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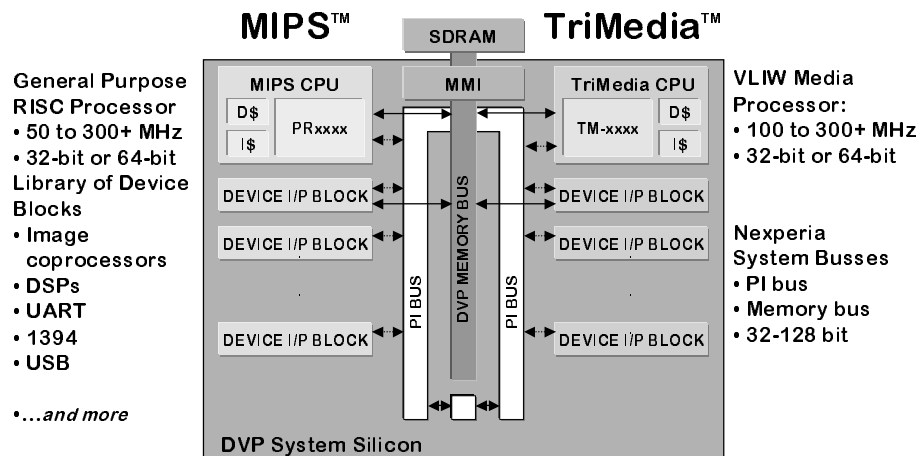
Platform Types

“Full Application Platform”

- Texas Instruments OMAP, Philips Nexperia, Infineon MGold
- Concentrates on full application
 - Delivers comprehensive set of libraries hardware and software
 - Delivers several mapping and application examples
 - Requires biggest modeling effort

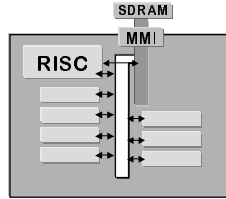


Example: Philips Nexperia™ DVP

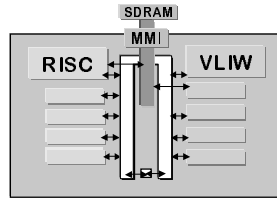


Flexible architecture for digital video applications

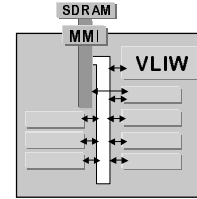
Nexperia™ Scalability



**MIPS CPU +
Device blocks +
Software**



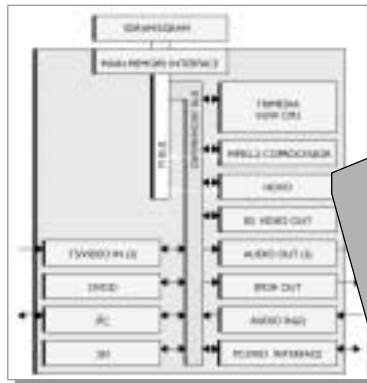
**MIPS CPU +
Trimedia CPU
replacing some
Device blocks**



**TriMedia CPU +
Device blocks when
control functions are
minimal**

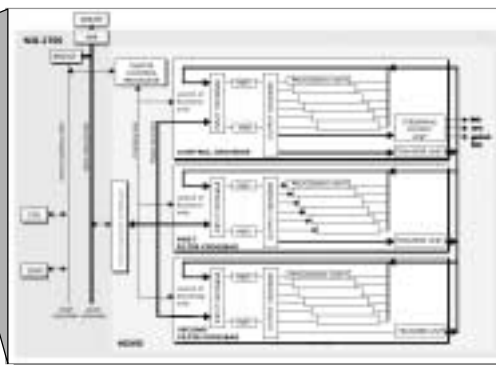
- Single architecture, multiple product configurations
 - Processor core options - TM32, TM64, MIPS32, MIPS64 ...
 - Device block options
- Highly programmable to weakly programmable

An Example of an Instantiation



Philips Nexperia NX-2700
A programmable HDTV
media processor

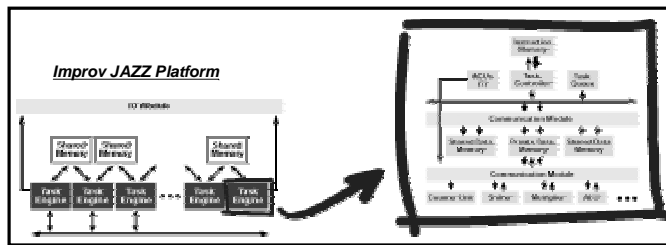
Combines Trimedia VLIW with
configurable media co-processors



Platform Types

“Processor-Centric Platform”

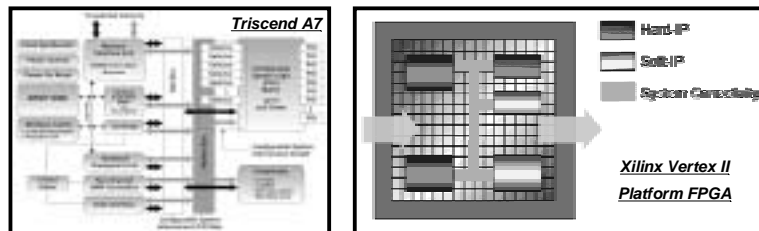
- Improv Jazz Platform, ARM Micropack, ST Micro Starcore Platform
- Concentrates on processor
 - Delivers Processor plus peripherals
 - Delivers Software drivers and basic application routines
 - Limits the modeling efforts



Platform Types

“Highly Programmable Platform”

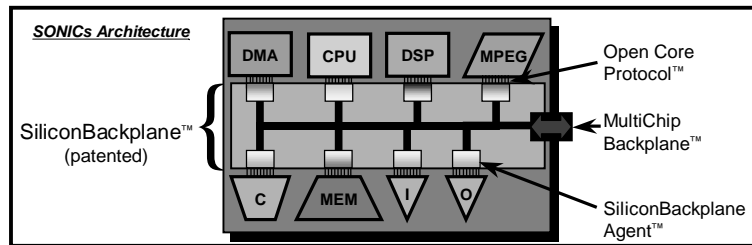
- Triscend A7, Altera Excalibur, Xilinx Platform FPGA, Chameleon
- Concentrates on reconfigurability
 - Delivers reconfigurable processor plus programmable logic
 - Modeling efforts undetermined because of programmable parts



Platform Types

“Communication Centric Platform”

- SONIC, Palmchip
- Concentrates on communication
 - Delivers communication framework plus peripherals
 - Limits the modeling efforts



Platforms: Abstraction

Platform stack {

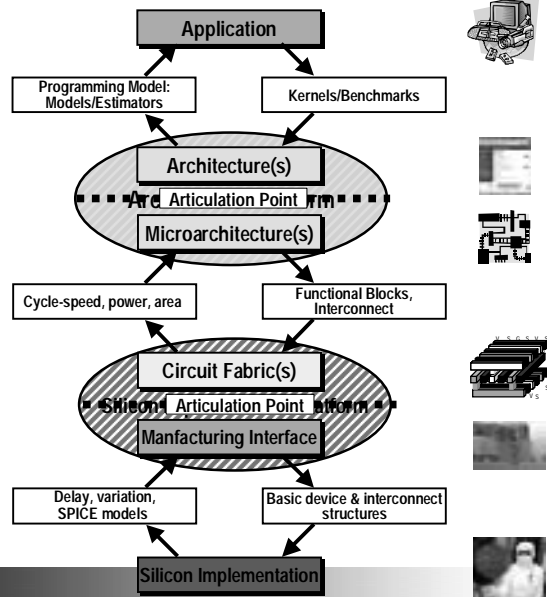


Platform
Mapping Tools
Platform

In general, a platform is an abstraction that covers a number of possible refinements into a lower level.

For every platform, there is a view that is used to map the upper layers of abstraction into the platform and a view that is used to define the class of lower level abstractions implied by the platform.

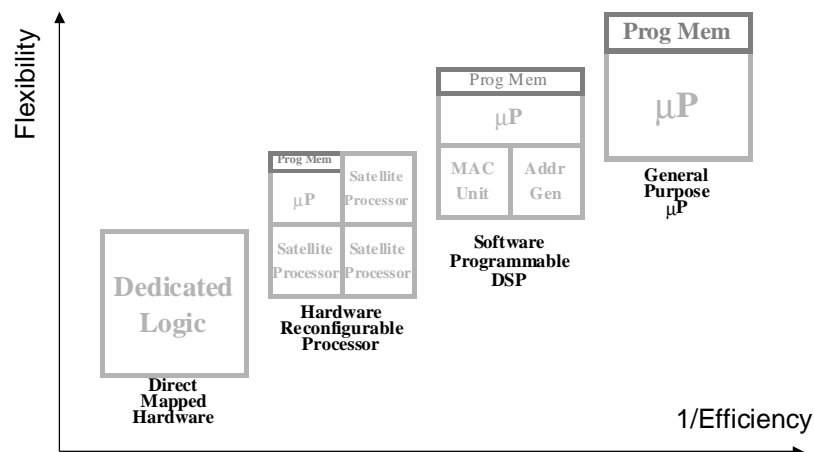
A Discipline of Platform-Based Design



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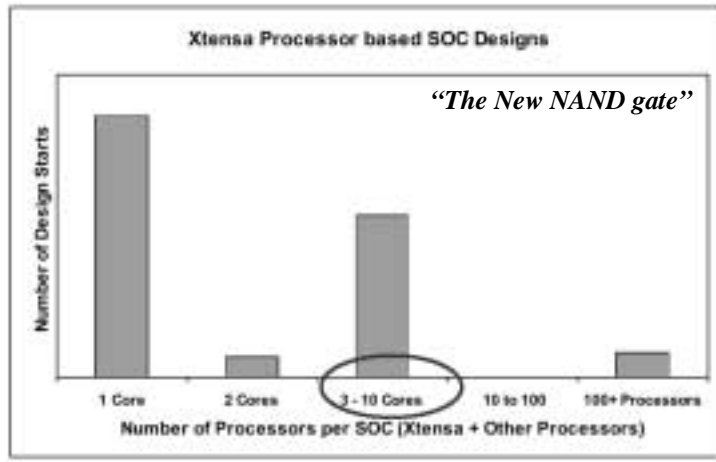
The Implementation Choices



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An Attractive Option: Multi-Processor System-on-a-Chip

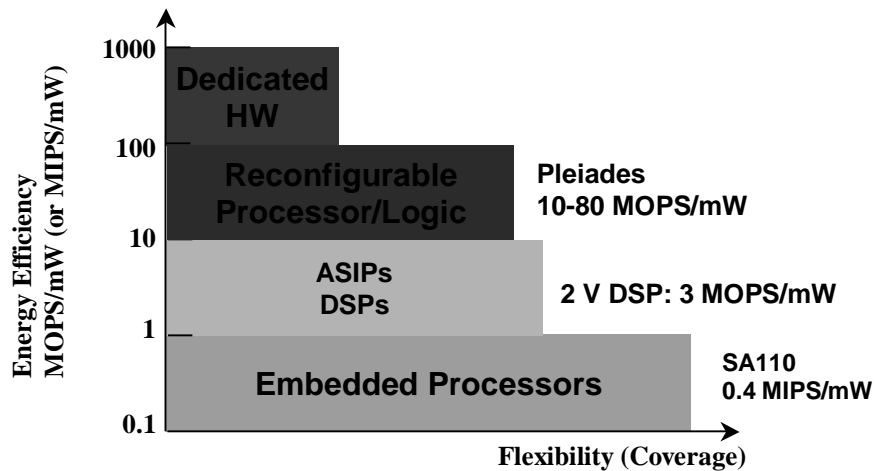


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Courtesy: Chris Rowen, Tensilica

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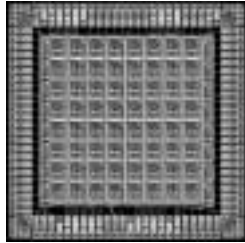
The Energy-Flexibility Gap



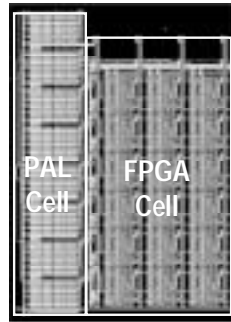
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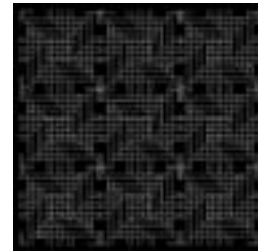
Need for Novel Predictable Implementation Fabrics



Embedded FPGA

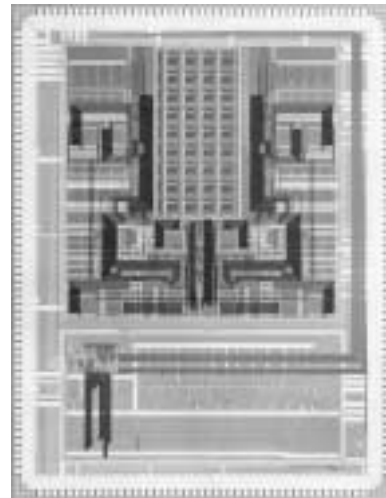


Hybrid PAL-FPGA

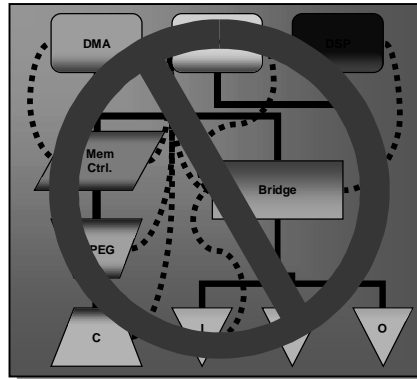


Via-Programmable GA

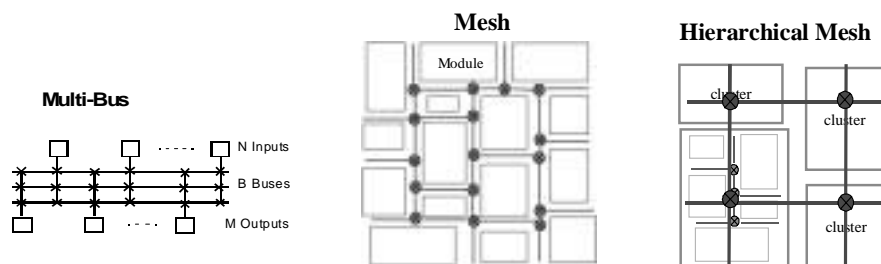
Pleiades: A Platform for Wireless



Communication-Based Design

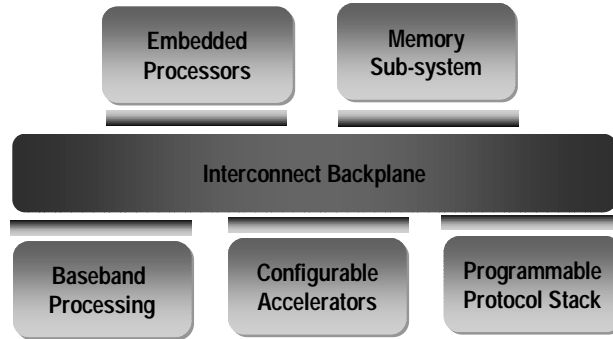


The “Network-on-a-Chip”



Major trade-off's in Performance, Power, and Complexity

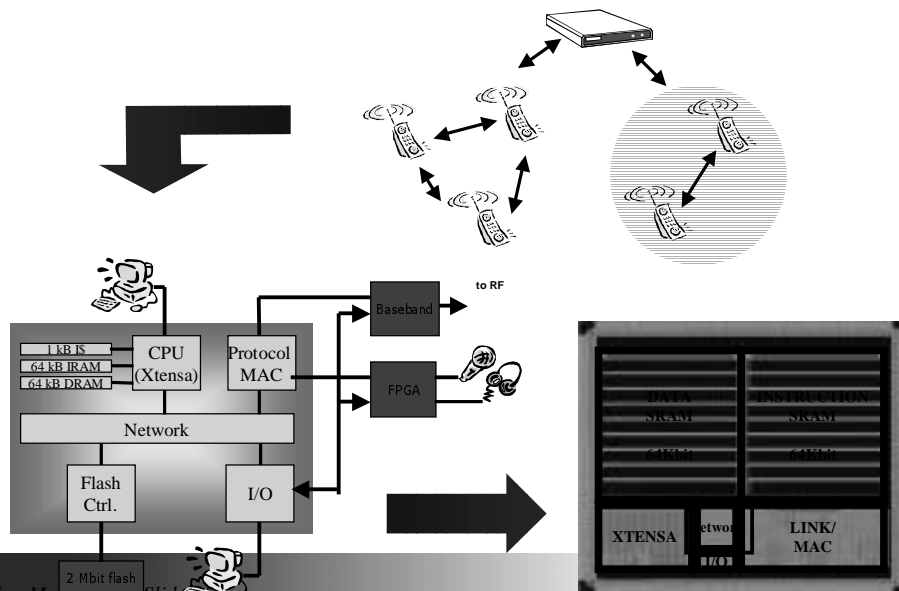
The Network-on-a-Chip Approach



Communication-based Design

- Orthogonalizes function and communication
- Builds on well-known models-of-computation and correct-by-construction synthesis flow
- Parallels layered approach exploited by communications community

Example: The PicoRadio II (TCI) Design



Summary and Perspective

- The successful implementation of Systems-on-a-Chip in the deep-submicron era requires a disciplined approach
- Application-Oriented Platforms need to simultaneously optimize flexibility, cost, energy, and performance.
- A whole new perspective on design methodologies for ICs – the “Post RTL Synthesis Era”
- Active research Agenda – Main focus of GSRC

**“Only the consumer gets freedom of choice;
designers need freedom *from* choice”
(Orfali, et al, 1996)**

**“The 4th Generation in Reuse will be IC ReUse
With Retargetable Fabrics”, Theo Claasen, CTO Philips**