

# A 100 $\mu$ W, 1.9GHz Oscillator with Fully Digital Frequency Tuning

Nathan M. Pletcher and Jan M. Rabaey

Department of Electrical Engineering and Computer Sciences  
 University of California, Berkeley  
 Berkeley, California, USA  
 {pletch, jan}@eecs.berkeley.edu

## Abstract:

A 1.9GHz CMOS digitally controlled oscillator (DCO) is designed in a standard 0.13 $\mu$ m process, targeting ultra low power frequency synthesizers for wireless sensor network transceivers. The oscillator exploits subthreshold device operation and a low 0.5V supply to achieve power consumption of only 100 $\mu$ W. A novel switched capacitor configuration is employed to realize a frequency resolution of 200kHz with a tuning range of 150MHz. High quality bondwire inductors also reduce power consumption. The phase noise is -114dBc/Hz at 1MHz offset, achieving performance competitive with other published work.

## 1. Introduction

Wireless transceivers for sensor networks present unique design challenges; the transceiver must be agile, highly integrated, and most importantly low power. Much progress has been made in this space, yielding high sensitivity transceivers utilizing RF-MEMS with power consumption under a milliwatt [1]. In order to enable fully asynchronous communication between nodes, even when under heavy duty cycling, each transceiver should be able to monitor the channel continuously and wake up only when data is being received. To enable this behavior, a carrier sense receiver is needed to monitor the channel for activity. Since this receiver is always listening, its power consumption should be on the order of 100 $\mu$ W.

This paper presents a tunable oscillator designed for the frequency synthesizer of such a carrier sense receiver. By employing digital tuning, the oscillator may be periodically calibrated to an accurate reference such as a crystal or MEMS-based oscillator [2]. The calibration aligns the oscillator with the system reference, performing channel selection and tuning for the carrier sense receiver. Between calibration cycles, the accompanying tuning loop circuitry is turned off to save power and the oscillator runs free until the next tuning cycle. Re-calibration could occur each time the main transceiver turns on to send and receive data.

The frequency tuning specifications for the digitally controlled oscillator (DCO) are derived from the intended application with periodic calibration, where the MEMS reference tolerance is 500ppm [2]. Accordingly, the target frequency resolution is set at 500kHz, which translates to approximately 1fF of switched capacitance at 1.9GHz. In addition, the total tuning range is chosen to be 200MHz

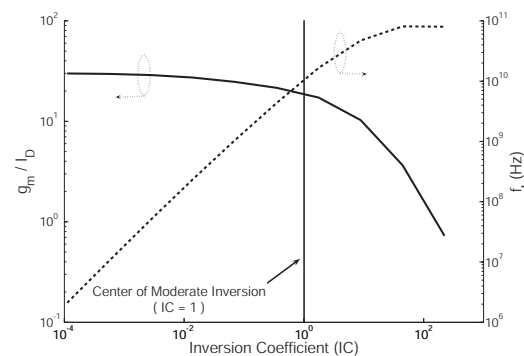


Figure 1: Transconductance efficiency and  $f_T$  for 0.13 $\mu$ m CMOS.

(10%) in order to cover uncertainty in the tank inductance value and other process variations.

In order to minimize the DCO power consumption, two major techniques have been utilized. At the circuit level, the DCO core transistors are designed to run in weak inversion, where more device transconductance is available for a given bias current. The circuit is also designed to run on a supply voltage well below the technology's nominal value to further minimize the power consumption. Recently, there has been interest in operating synthesizer VCOs at low supply voltages. In [3], transformers were used to enable the VCO internal nodes to swing above  $V_{dd}$  and below ground to maximize voltage headroom. In the design presented here, subthreshold device operation simultaneously enables low current and low voltage operation, while still achieving the desired performance.

## 2. Circuit Design

### 2.1 Oscillator Core Design

The use of subthreshold transistor biasing has been successfully employed in low power analog circuits for many years to take advantage of the high transconductance efficiency available in this regime [4]. Unfortunately, weak inversion operation usually results in large devices with substantial parasitics, so this technique has traditionally not been attractive for RF designs. The conflicting trends of transconductance efficiency and device  $f_T$  are illustrated in Fig. 1, where simulated values of these parameters are plotted across the entire range of device operation for a 0.13 $\mu$ m technology. The parameter  $IC$  represents normalized current density, with  $IC = 1$  indicating the

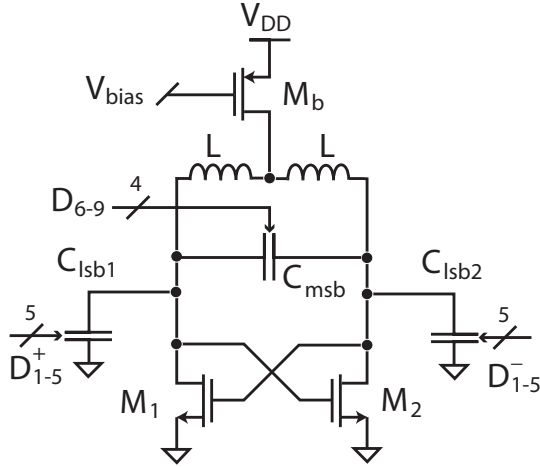


Figure 2: Simplified schematic of oscillator core.

center of moderate inversion. In this scaled technology, peak  $f_T$  is close to 100GHz, meaning that transistors no longer need to be biased for optimal  $f_T$  when low power consumption is one of the chief design goals. The weak inversion regime ( $IC \approx 0.1$ ) may then be used to take advantage of high transconductance efficiency, which may be more than a factor of two higher than in strong inversion.

The simplified schematic of the oscillator core is shown in Fig. 2. In order to reduce power consumption, the oscillator is designed to operate on a 0.5V supply, exploiting the trend towards low supply voltages in scaled CMOS technologies. A differential NMOS-only topology is adopted because it provides higher output swing for low supply voltages. With only two stacked transistors, the chosen oscillator topology is able to operate on very low supply voltages. Although the low supply reduces the maximum possible voltage swing ( $2V_{dd}$ ), this is not a large disadvantage because the ultra low power oscillator is designed to run in the current-limited regime.

Devices  $M_1$  and  $M_2$  are sized with large  $W/L = 300\mu\text{m}/0.13\mu\text{m}$  for a design bias current of  $100\mu\text{A}$  in each device. At this bias point, the device inversion coefficient is approximately 0.1, providing  $g_m/I_d \approx 25$  while still yielding manageable parasitics. An additional benefit of subthreshold operation for this design is that  $V_{dsat}$  and  $V_{gs}$  are both much lower than in strong inversion, which conserves valuable voltage headroom. The current source PMOS transistor  $M_b$  provides bias current to the core and is sized to operate in saturation for supply voltages of 0.5V and below.

## 2.2 Tuning Capacitor Bank Design

The oscillation frequency of the DCO is given by (1):

$$f_0 = \frac{1}{2\pi\sqrt{L(C_0 + C_{var})}} \quad (1)$$

where  $L$  is the tank inductance,  $C_0$  is the constant capacitance due to device and wiring parasitics, and  $C_{var}$  represents the variable capacitance used to tune the frequency. Given the specifications for tuning range and resolution in Section 1., the approximate required number of frequency

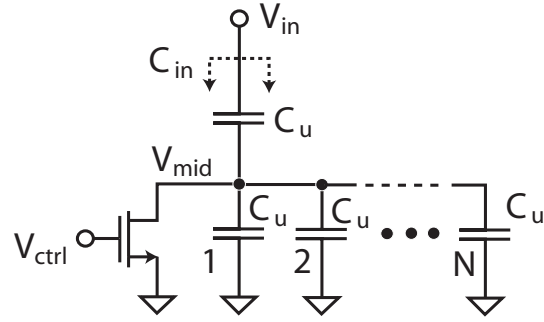


Figure 3: Schematic of switched capacitor LSB implementation.

steps  $M$  is calculated from (2):

$$M \geq \frac{\text{Tuning Range}}{\text{Resolution}} = \frac{200\text{MHz}}{500\text{kHz}} = 400 \quad (2)$$

which corresponds to at least 9 bits of tuning. Although the oscillation frequency varies with the square root of tank capacitance, the nonlinearity is small over the 10% tuning range. Accordingly, the capacitor banks are designed with linear capacitance steps to simplify the layout.

The implementation of a 1fF least significant bit (LSB) capacitance poses a challenge, because wiring parasitics are on the same order of magnitude. Capacitor matching is also a concern for such small unit capacitors. One possibility is to use small MOS varactors switched between high and low capacitance states [5]. This approach, however, requires testing to determine the high and low capacitance control voltages, and the nonlinear capacitance allows noise on the control voltages to couple into the tank as phase noise. A switched capacitor implementation using linear capacitors avoids this problem and allows standard digital outputs to control the capacitor bank.

In order to implement an effective capacitance step of 1fF, a ratioing scheme is used with larger unit capacitors  $C_u$ . The architecture is shown in Fig. 3. The change in capacitance  $C_{in}$  when the switch changes from off to on is denoted by  $\Delta C$  (3):

$$\Delta C = \frac{C_u}{N + 1} \quad (3)$$

The ratio scheme has several beneficial features. First, routing parasitics at the input node  $V_{in}$  do not affect  $\Delta C$ . In addition, any routing or switch parasitics at the intermediate node  $V_{mid}$  may be lumped into the array of  $N$  capacitors and some explicit capacitors may then be removed to maintain the desired  $1/(N + 1)$  ratio. In this implementation, the unit capacitors are realized as interdigitated fingers using metal layers 1 through 5, which are available in the CMOS process without any special options. The unit capacitor  $C_u$  is chosen to be 20fF, which is larger than minimum size in order to maintain reasonable matching and accuracy. Using  $N = 19$  then results in  $\Delta C = 1\text{fF}$ , and the entire structure is repeated in a binary-weighted array. The parasitics at node  $V_{mid}$  were estimated from layout extraction, indicating that the parasitics were roughly equal to  $2C_u$ . Therefore, two unit capacitors were removed from the array in order to maintain the desired  $N$  ratio.

The major disadvantage of the architecture in Fig. 3 is that the unswitched capacitance, given by (4), is much larger than  $\Delta C$ :

$$C_{unswitched} = C_u \frac{N}{N+1} \gg \Delta C \quad (4)$$

In order to avoid a large unswitched capacitance for the higher bits, the capacitor bank is segmented into separate LSB and MSB banks. The segmentation scheme implements the 5 least significant bits with the ratio structure in Fig. 3, while the 4 most significant bits are realized as standard binary-weighted switched capacitor structures with an effective switched capacitance of 29fF.

Finally, the effective LSB capacitance step has been further reduced by implementing the tuning capacitor as two individual banks  $C_{lsb1}$  and  $C_{lsb2}$ , one on each output of the differential oscillator as shown in Fig. 3. The banks are controlled independently and are incremented one at a time instead of simultaneously. In this mode of operation, it can be shown that the effective capacitance step is  $\frac{1}{2}\Delta C$  if  $\Delta C$  is small compared to the overall tank capacitance, which is clearly true in this case. Using this simple algorithm, the effective number of bits becomes 10 and the minimum frequency step is reduced by a factor of two without decreasing the physical capacitor size.

### 2.3 Inductor Implementation

For a low power oscillator, the quality factor  $Q$  of the tank inductance is critical because it normally limits the overall  $Q$ . In this case, the critical transconductance for oscillator startup depends on the effective parallel impedance of the tank at resonance as follows:

$$g_{m,crit} = \frac{1}{R_p} = \frac{1}{Q\omega_0 L} \quad (5)$$

where  $R_p$  is the equivalent parallel resistance of the tank at resonance and  $Q$  represents the quality factor of the inductor. Since  $R_p$  is directly proportional to  $Q$ , achieving a high inductor quality factor is critical to minimizing the startup current and power consumption. The unswitched capacitance from the capacitor bank and device parasitics is quite large, meaning that the required inductance is only about 3nH at 1.9GHz. For this relatively small inductance, bondwire inductors offer a good compromise, with higher quality factor than integrated coils but lower parasitics than off-chip components [6]. Bondwires of length 3.2mm were used here to provide approximately 3nH of inductance each, which agreed well with calculations from first-order formulas. The oscillator tuning range is large enough to cover variation in bondwire inductance from chip to chip.

### 3. Experimental Results

The oscillator was fabricated in a standard 0.13 $\mu$ m CMOS process with 6 metal layers; the chip area is  $2 \times 2$  mm<sup>2</sup>. The CMOS die was epoxied directly to a printed circuit board and wirebonded to pads on the board, with longer bonds forming the inductors. A die photograph illustrating the final assembly is shown in Fig. 4.

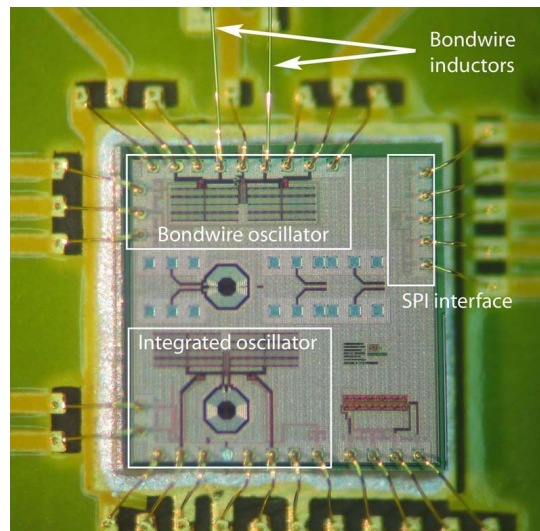


Figure 4: Chip photograph.

A fully integrated version of the oscillator was also fabricated employing an on-chip, 3nH center-tapped inductor. Both versions were laid out to match closely with the exception of the inductor implementation. An integrated inductor test structure was measured in isolation to extract an experimental model, thereby allowing a more accurate characterization of the tuning capacitor array without the uncertainty of the bondwire inductance and parasitics.

Performance comparisons between the two versions highlight the large benefit in quality factor from the bondwire inductor. At 1.9GHz, the measured  $Q$  for the on-chip inductor was 11, but the bondwire  $Q$  is estimated at 30, which leads directly to lower power consumption and better phase noise performance. A summary of the measured performance for both oscillators is given in Table 1.

To facilitate the testing of both oscillators, a digital SPI interface is included to control the capacitor banks. An HP8563E spectrum analyzer was used to measure the oscillation frequency while sweeping the frequency tuning word using the half step method outlined in Section 2.2. For all measurements, the supply voltage and bias current were set to the nominal values of 0.5V and 200 $\mu$ A, respectively. The frequency sweep results are shown in Fig. 5, where the overlapping bands are evident at the MSB switch points (code multiples of 64). The differential peak-to-peak output swing is 250mV, which remains constant within 25mV across the entire frequency range. Supply pushing is measured to be 27 MHz/V.

The capacitor bank performance is calculated from the measured frequency using the known model parameters of the integrated inductor. A frequency resolution of 200kHz is achieved, with a tuning range of 155MHz. The effective capacitance resolution with both LSB banks operated in tandem is 500aF.

The measured phase noise spectrum is shown in Fig. 6, acquired from an Agilent E5052A Signal Source Analyzer. The spectrum is plotted with all switches off (highest frequency) and all switches on (lowest frequency). The phase noise plot exhibits the classical shape with a  $1/f^3$  dependence close to the carrier and rolls off with  $f^2$  at higher offsets. The corner frequency is at approx-

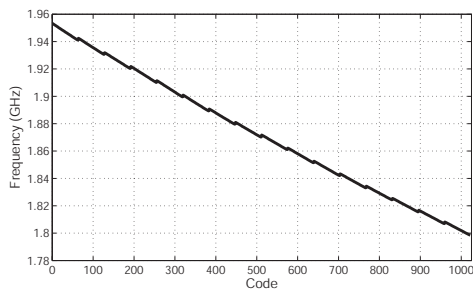


Figure 5: Measured frequency tuning across code range.

Table 1: DCO Performance Summary.

Parameter	Bondwire	Integrated
Power consumption	100 $\mu$ W	186 $\mu$ W
Supply voltage	0.5 V	0.5 V
Center frequency	1.87 GHz	1.7 GHz
Frequency resolution	200 kHz	150 kHz
Tuning range	155 MHz	132 MHz
Phase noise @ 1MHz offset	-114 dBc/Hz	-109 dBc/Hz

imately 10kHz. At 1MHz offset, the spot phase noise is -114dBc/Hz. The phase noise displays little dependence on the frequency tuning; the small difference is likely due to the small change in tank quality factor with frequency.

The DCO presented here targets somewhat different specifications from VCOs for traditional wireless systems. In order to compare this oscillator performance to other published work, it is useful to employ a figure-of-merit (FOM) that captures two important performance parameters for oscillators: phase noise and power consumption. The formula (6) is presented in [3] and is repeated here for convenience:

$$FOM = 10 \log \left[ \left( \frac{f_0}{\Delta f} \right)^2 \frac{1}{L\{\Delta f\} \times V_{dd} \times I_{dd}} \right] \quad (6)$$

The calculated FOM for this oscillator is 190dB, which compares favorably with the other published low power VCOs in Table 2.

#### 4. Conclusion

This paper presents an ultra low power, digitally tuned oscillator implemented in 0.13 $\mu$ m CMOS. Bondwire inductors are employed for high  $Q$  and no external components are used. Subthreshold device operation is shown to be a feasible method of increasing transconductance efficiency at RF. The oscillator topology is conducive to operation from low supply voltages and measurements confirm operation well below 0.5V. Fully digital frequency tuning achieves the required resolution and tuning range using only switched linear capacitors. The presented oscillator verifies the feasibility of these techniques for wireless sensing applications, where minimum power consumption is the most important requirement.

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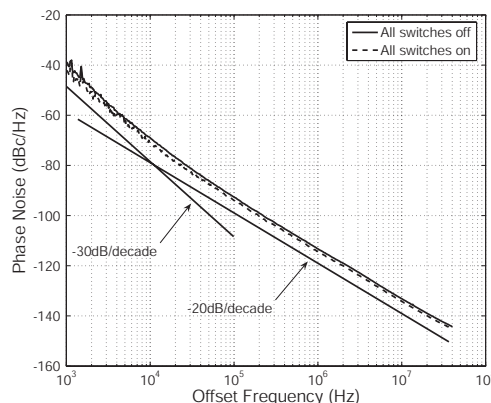


Figure 6: Measured phase noise spectrum.

Table 2: Comparison with published work.

Reference	$V_{dd}$ (V)	$I_{dd}$ ( $\mu$ A)	Freq. (GHz)	FOM (dB)
[6]	3	8000	1.76	181
[7]	1	230	0.4	176
[3]	0.5	1140	3.8	193
This work	0.5	200	1.9	190

valuable discussions and assistance. They also thank B. Gupta and STMicroelectronics for CMOS fabrication.

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