

A 65 μ W, 1.9 GHz RF to Digital Baseband Wakeup Receiver for Wireless Sensor Nodes

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Abstract—A complete 1.9GHz receiver, with BAW resonator-referenced input matching network, is designed as a wakeup receiver for wireless sensor networks. The 90nm CMOS chip includes RF amplifier, PGA, ADC, and reference generation, while consuming 65 μ W from a single 0.5V supply. The input RF bandwidth of the receiver is 7MHz, while the maximum data rate is 100kbps. When detecting a 31-bit sequence, the receiver exhibits -56dBm sensitivity for 90% probability of detection.

I. INTRODUCTION

In wireless sensor networks (WSN) individual nodes are heavily duty-cycled in order to save power, with the result that nodes spend most of the time in sleep mode. Typically, each node periodically monitors the wireless channel to listen for potential incoming traffic. Alternatively, a “wakeup” receiver (WuRx) can be used to monitor the channel continuously and activate the node only when neighboring nodes request to send packets. However, the WuRx power consumption must be small compared to the node’s main transceiver because it remains active at all times. For typical sensor network environments the allowable power budget for the WuRx is less than 100 μ W [1], which is significantly lower than that of state-of-the-art transceivers [2, 3]. With such a low power budget, even components that consume only a few microwatts of power become significant. Therefore, this paper addresses the design of a complete WuRx, including baseband circuitry and reference generation.

II. RECEIVER ARCHITECTURE AND CIRCUIT DESIGN

A. Receiver Architecture

A tuned RF (TRF) architecture with on-off keying (OOK) is selected in order to simplify the receiver circuits as much as possible. Most importantly, the TRF architecture eliminates the local RF oscillator, whose power consumption alone would easily exceed the entire budget. Furthermore, throughout the receiver, circuit architectures are chosen to enable all components to operate from an aggressively scaled 0.5V supply. A block diagram of the entire receive chain is shown in Fig. 1.

The front-end amplifier (FEA) and matching network serve as the antenna interface for the receiver and amplify the input signal at RF. Next, the envelope detector downconverts the OOK RF signal to baseband. Finally, the analog baseband signal is amplified again by a programmable gain amplifier (PGA) before being converted to digital form by the ADC. The baseband signal may then be further processed in the digital domain to detect the incoming bits.

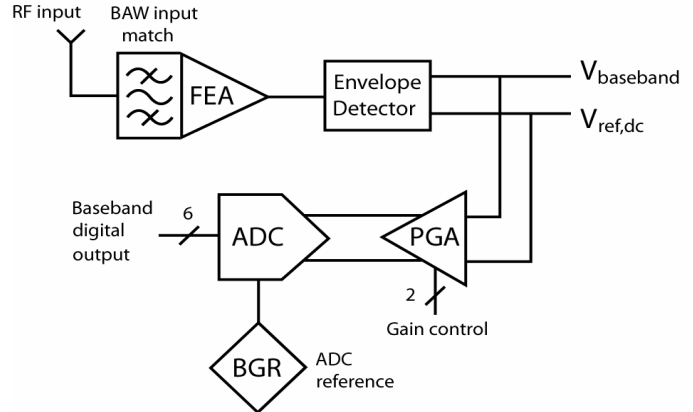


Fig. 1. Block diagram of complete receiver.

B. RF Front-end Circuitry

The front-end amplifier (FEA) at the input of the receiver must provide both precise input matching and maximum gain at the signal frequency to overcome the noise of the envelope detector. The FEA schematic is shown in Fig. 2. The amplifier’s antenna interface integrates a 1.9GHz bulk acoustic wave (BAW) resonator [4] and on-chip capacitive transformer (C_1 , C_2), which matches the high impedance of the BAW at resonance to the 50 Ω resistance of the antenna port. The high quality factor (Q) of the BAW resonator allows sharp filtering of the input signal, reducing out-of-band interferers which would otherwise be downconverted by the envelope detector.

Devices M_1 and M_2 form a standard cascode transconductor with an active inductor load comprised of M_3 , M_4 , and M_5 . The active inductor can synthesize higher impedance at 2 GHz

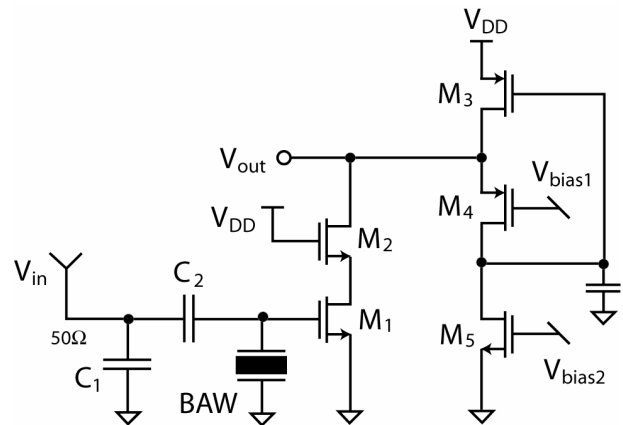


Fig. 2. Frontend amplifier schematic with BAW input network

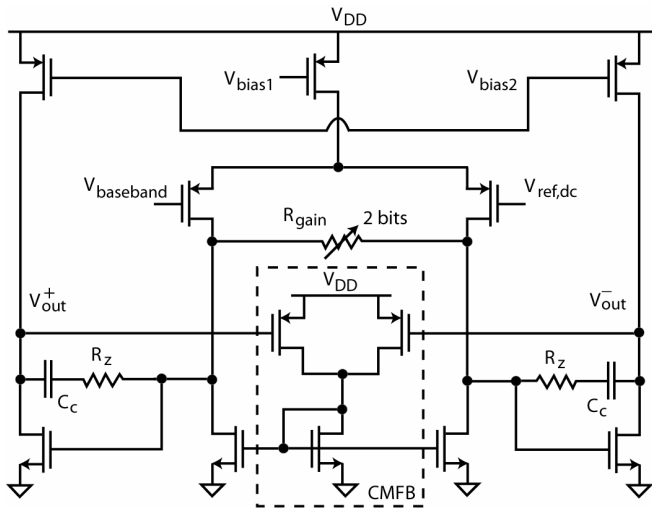


Fig. 3. Schematic of baseband programmable gain amplifier.

than an on-chip spiral inductor, which helps increase the gain. The benefit of higher gain outweighs the excess noise of the active inductor in this design because the receiver noise figure is limited by the envelope detector instead of the FEA. The bulk terminals of several devices are tied to $V_{DD}/2$ in order to reduce the threshold voltages and maximize voltage headroom under the low supply voltage. The FEA is coupled directly to the envelope detector, which is implemented with an MOSFET biased in the subthreshold region contributes the nonlinear transfer function, downconverting the RF signal from the FEA to baseband. A replica path generates a DC reference voltage for the following stages.

C. Baseband Section

In the baseband section of the receiver, a fully differential PGA amplifies the pseudo-differential envelope detector output and drives the ADC. The PGA design employs a two-stage architecture in order to accommodate the low supply voltage; the schematic is shown in Fig. 3. Gain control is accomplished through switched resistor loading of the first stage, providing 4 digitally programmable gain settings between 18 and 50dB.

The ADC architecture is a 6-bit successive approximation register (SAR) based on [6] and optimized for low power and low supply voltage. The ADC, capable of sampling up to 1 Msample/s, draws less than $5\mu\text{W}$ from the 0.5V supply. A fully-differential bandgap reference (BGR) generator (Fig. 4), which also operates from the global 0.5V, supplies all ADC reference voltages. In order to achieve operation with a supply voltage below a diode drop, the reference combines the current-scaling technique of [7] with the use of subthreshold MOSFETs (Q_1 , Q_2) in place of bipolar transistors to replace the V_{be} dependence of a bipolar BGR. Furthermore, the BGR voltage can be scaled down digitally by selecting different taps from the $R_{3/4}$ resistor string, effectively reducing the LSB size in the ADC. Because the ADC dynamic range is not limited

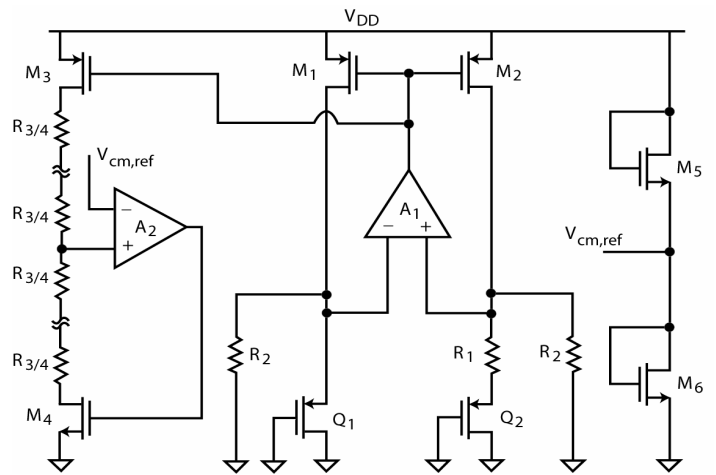


Fig. 4. Schematic of reference generator circuit.

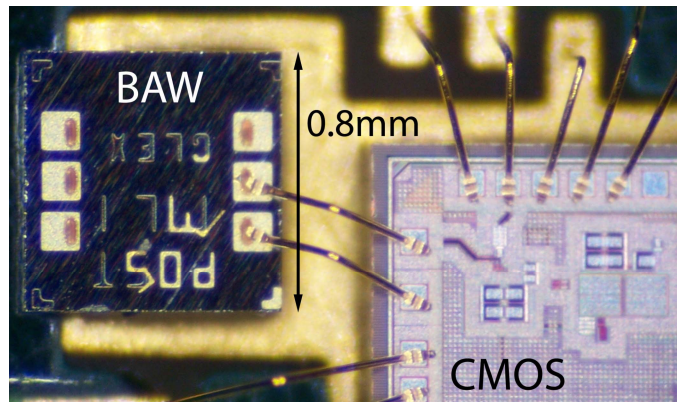


Fig. 5. Prototype micrograph with CMOS and BAW resonator.

by thermal noise, the reference scaling feature provides an additional 12dB of baseband gain from the ADC.

III. MEASUREMENT RESULTS

The receiver is implemented in a standard 90nm CMOS process with metal-insulator-metal (MIM) capacitors. A die micrograph is shown in Fig. 5. The CMOS die is mounted on a printed circuit board, and the BAW resonator die is bonded directly to the CMOS in the upper left corner. The lack of on-chip inductors allows the entire receiver to be implemented in a small corner of the die. Thus, the active area of the CMOS circuitry is less than 0.16mm^2 , using no external components except one BAW resonator.

Fig. 6 shows the measured $|S_{11}|$ of the receiver, which is better than -15dB at the resonant frequency. The gain of the FEA is characterized using a standalone test amplifier included on the chip. Peak $|S_{21}|$ of the FEA is +10dB, corresponding to approximately 18dB in-situ voltage gain after loss from the measurement buffer is subtracted. The effect of the high-Q resonance of the BAW filter is clearly visible in the gain response. The measured noise figure of the standalone amplifier is 9.2dB, compared with 7.5dB obtained

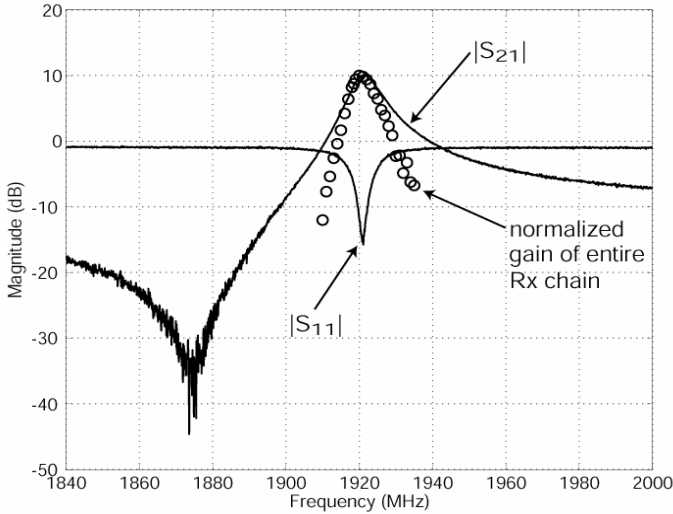


Fig. 6. Front-end amplifier S-parameters and receive chain gain.

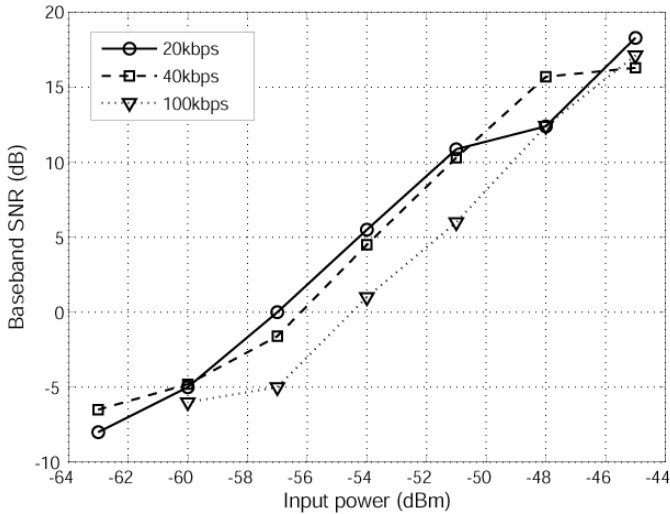


Fig. 7. Receiver output SNR for various data rates.

from simulations. The high noise figure is expected due to the active inductor and the extremely low bias current budget. However, as mentioned in Section II, the overall receiver noise figure is limited by the envelope detector, leading the designer to trade noise performance for higher gain in the FEA whenever possible.

In order to characterize the entire receiver, the baseband digital samples from the ADC output were captured using a logic analyzer system. The normalized gain of the entire receiver to baseband is overlaid with S-parameter data in Fig. 6, exhibiting an RF bandwidth of 7MHz. The RF bandwidth of the receiver is slightly less than the intrinsic bandwidth of the FEA due to the nonlinear squaring function of the envelope detector. Fig. 7 compares the receiver sensitivity for different data rates, using the metric of output signal-to-noise ratio (SNR). For a typical baseband SNR requirement of 12dB, the measured sensitivity is -50dBm for a data rate of 40kbps. The maximum data rate is 100kbps, which causes degradation in

TABLE I
WAKEUP RECEIVER PERFORMANCE SUMMARY

Supply Voltage	0.5 V
Front-end Amplifier	S21 = 10dB (18dB in-situ) S11 = -16dB Power = 48 μ W
PGA	Min / Max Gain = 18 / 50 dB 3dB-BW > 150 kHz Power = 2.5 μ W
Envelope Detector	Power = 1 μ W
ADC	Resolution = 6b Clock frequency = 750kHz Min. LSB = 1.05 mV Max. LSB = 4.2 mV Core power = 3.8 μ W Reference power = 10 μ W
Receiver	Sensitivity: -49dBm @ 20kbps -50dBm @ 40kbps -48dBm @ 100kbps Overall 3dB-BW = 7 MHz Power = 65 μ W

sensitivity by about 2dBm. The total power consumption from the 0.5V supply is 65 μ W, of which the FEA consumes approximately 75%. An overall performance summary of all implemented receiver circuit blocks is given in Table I.

As described in Section II, the reference voltage generator for the ADC was designed to be digitally scalable. This feature effectively implements gain control directly in the ADC. In Fig. 8, transient waveforms of the ADC samples are plotted for two different ADC reference voltage settings. Both traces were captured with the same RF input power, demonstrating 6dB of effective gain via reference voltage scaling.

Finally, because the intended application is a wakeup receiver, it is important to characterize the performance of the receiver while detecting a “wakeup signal.” For the purposes of this testing, the wakeup signal is represented by a binary PN sequence. Operating as a wakeup receiver, the relevant performance metric is not baseband SNR, but probability of detection and false alarm (FA) rates after appropriate baseband detection algorithms. For maximum testing flexibility, the wakeup sequence detection algorithm is performed offline in Matlab with a simple correlator bank architecture. However, simulations of the digital circuitry required to implement the algorithm indicate that the power consumption of the detection block should be less than 5 μ W. The detection threshold for all measurements was set for a fixed 90% probability of detection (P_{det}). As the RF input power decreases the detection threshold must be reduced to maintain a constant P_{det} , thereby increasing the likelihood of false alarm due to random noise. For comparison, the test was repeated using different PN code lengths of 7, 15, 31, and 63 bits. For high input power levels (high baseband SNR), the average time between false alarms increases rapidly and false

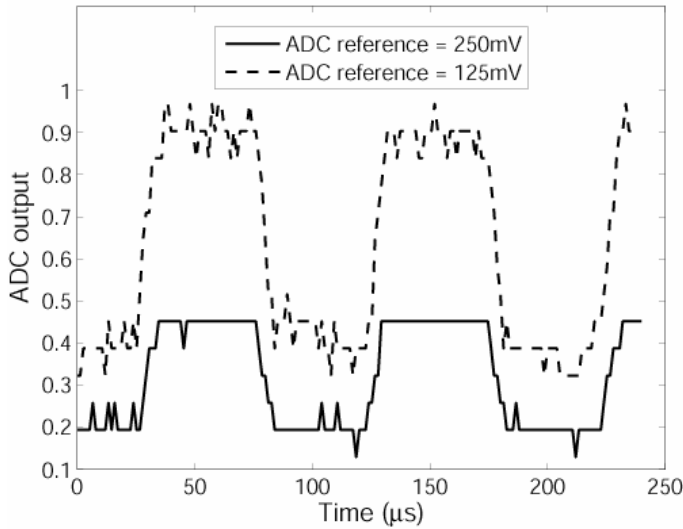


Fig. 8. Effect of ADC reference voltage scaling.

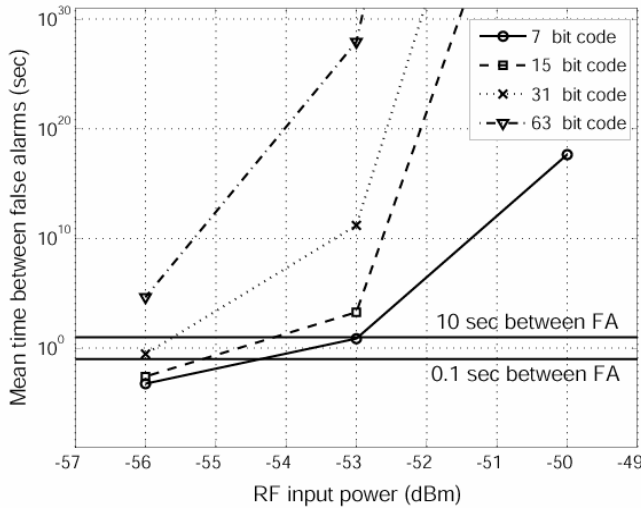


Fig. 9. Receiver sensitivity to wakeup code sequences of various lengths.

alarms become very infrequent. In typical sensor network environments with traffic rates on the order of several packets per second, the minimum time between FA should be at least 1 second. As shown in Fig. 9, the mean time between FA reaches 1 second for a minimum detectable signal of -56 dBm with a wakeup sequence length of 31 bits. This represents the practical sensitivity level of the receiver to realistic wakeup signals under typical conditions.

TABLE II
PERFORMANCE COMPARISON

Reference	Carrier Frequency (MHz)	Sensitivity (dBm)	Active power (μ W)
[2]	1900	-100.5	400
[3]	2400	-95	330
[8]	900	-37 to -65	500 to 2600
WuRx	1900	-50	65

IV. CONCLUSION

The overall performance of the WuRx is compared with other data receivers for sensor networks in Table II. Although several achieve impressive sensitivity, their power consumption is much too high to be useful as an “always on” wakeup receiver. To the authors' knowledge, this design is the only reported receiver to integrate all necessary components of a wakeup receiver, at sufficiently low power to meet the specifications.

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