

A 100KS/s 65dB DR $\Sigma - \Delta$ ADC with 0.65V supply voltage

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Abstract— We present a low-power $\Sigma - \Delta$ modulator to be used in the baseband sections of wireless sensor network receivers with 0.65V V_{dd} operation. The design is optimized for low-power consumption and low operating supply by minimizing operational amplifier open-loop gain. Simple differential pair amplifiers with ≈ 40 dB of open loop gain and low noise factor are employed as the integrator cores and guarantee a spurious-free dynamic range(SFDR) of 63dB. The prototype employs only standard V_{th} devices and dissipates $27\mu W$ to achieve 65dB dynamic range in a 50KHz bandwidth, including regulated bias. The peak SNDR of 59.5dB corresponds to a figure of merit (FOM) of 0.36pJ/Conv.Step.

I. INTRODUCTION

The reduced supply voltage available to integrated circuits in scaled technologies exacerbates dynamic range issues and limits the available per-stage gain of amplifiers, resulting in designs with reduced power efficiency. Architectures that do not rely on high-gain operational amplifiers, such as successive approximation converters and sigma-delta modulators become therefore more and more attractive.

When embedded in a receiver system, oversampling converters have a additional advantages, as they enable a simplification of the analog filtering subsystem and an increased level of receiver digitization. Furthermore, thanks to oversampling, $\Sigma - \Delta$ converters are inherently robust to charge leakage, which is an increasing concern in sub-MHz rate converters implemented in fineline CMOS [1].

For example, in the super-regenerative receiver described in [2], a continuous-time filter is used to separate the quench tone from the pulse width modulated signal in the baseband. This filter consumes a significant amount of power ($32\mu W$), while its complexity limits the achievable data-rate of the radio. Using an oversampling converter, the quench tone could instead be sampled together with the data, and removed in the digital domain by the decimation filter. This would lead to increased end-to-end data-rate, higher programmability, and easier portability to future processes.

This paper presents a switched-capacitor sigma-delta modulator for wireless sensor receivers that employs a low-gain differential pair amplifier as the integrator building block. Thanks to the simple amplifier structure, a small noise factor and a low flicker corner frequency are obtained, resulting in low power consumption. This prototype modulator consumes $27\mu W$ from a 0.65V supply, showing that that the increased

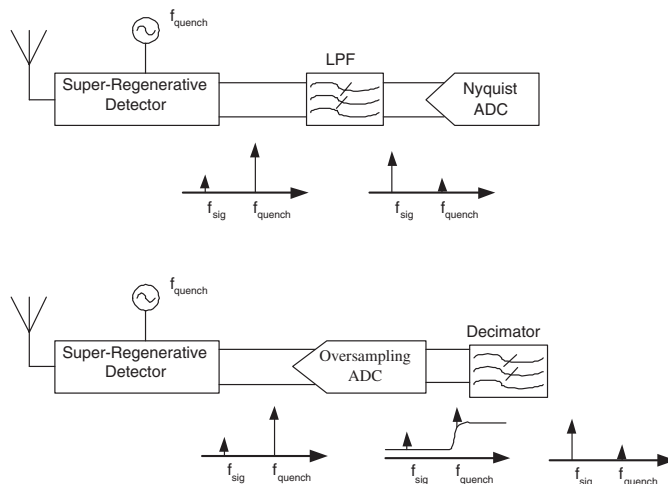


Fig. 1. Radio receiver baseband architectures: analog filtering+Nyquist conversion (top); oversampling conversion+ digital decimation(bottom)

receiver digitization allowed by its use does not introduce a power penalty when compared to traditional solutions.

II. ARCHITECTURE DESIGN

The major sources of power efficiency loss in low voltage mixed-signal designs are reduced signal swing and reduced per-stage gain of amplifiers. Minimizing operational amplifier gain specifications and maximizing swing are therefore the key goals pursued at the architecture level.

Fig. 2 displays the converter architecture adopted. A single-bit, single-loop architecture is preferred to a MASH cascade to relax amplifier amplifier gain requirements and minimize hardware complexity by obviating the need for dynamic element matching, while a third order loop filter is preferred to a second order one as it requires a lower amplifier gain to suppress limit cycles with low input amplitudes [3]. The

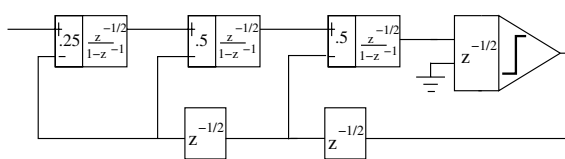


Fig. 2. Modulator Architecture

oversampling ratio is set to 64, leading to a nominal clock frequency of 6.5MHz and ensuring a signal to quantization noise ratio higher than 82dB even in the presence of leaky integrators. As half-delay integrators are used in the forward path, delay cells, implemented with standard cell flip-flops, need to be inserted in the feedback path. The coefficients of the loop filter have been chosen to minimize integrator swing to be [0.25, 5.5] as suggested in [4]. System level simulations show that the integrator swings are kept within $\pm V_{ref}$ for input signals as high as -6dBFS.

III. CIRCUIT DESIGN

Ensuring sampling linearity and achieving power-efficient and low-noise voltage gain are key issues when designing under a reduced supply. In this work, a bootstrapping technique [5] linearizes switch on resistance, while a bottom-plate sampling scheme suppresses residual signal dependent charge injection due to body effect. This scheme guarantees better than 80dB linear sampling for frequencies up to 20 MHz. An operational amplifier topology able to deliver sufficient gain and bandwidth at low power levels is also required. Since at the low 0.65V supply cascoding is not practical, obtaining gain in the order of $(g_m r_o)^2$ typically requires two-stage amplifiers to be employed, leading to an approximately four-fold power penalty. In order to avoid costly overdesign, a MATLAB-based simulation tool ([3]) was developed and used to evaluate the effect of nonlinear operational amplifier gain on converter performance. The analysis showed that for the chosen architecture, and assuming a peak SNDR specification of the order of 60dB, an amplifier open loop gain of 36dB, which can be obtained in one stage, is sufficient. Such modest gain value could be achieved by using of a current mirror OTA, obtaining rail-to-rail operation ([6], [4]). This topology is avoided here because it presents a tradeoff between the position of the non-dominant pole associated with the current mirror, its noise contribution and its current gain M . In order for a current mirror OTA to be power efficient, a large value of M should be used. However, a large M reflects into poor stability and high integrated output referred noise. To avoid this tradeoff, a simple differential pair amplifier is used (Fig. 4). In this case, the only non-dominant pole is determined by the non-quasi static behavior of the input transistors ([7]), while the load devices do not enter the frequency response and can hence be made long and wide, decreasing their flicker corner frequency and increasing the output resistance. With this choice, thermal noise factor is traded for signal swing, which has to be maximized through careful design. The first integrator uses of 24u/1.75u n-channel input devices and 32u/4u p-channel load devices to achieve a DC gain of 39dB in conjunction with a 10KHz corner frequency at a bias current of 19uA. All the devices are biased in moderate inversion to keep parasitic loading at a reasonable value. The input and output common mode are set at 400mV, resulting in a signal swing of 300mV zero-peak differential. The second and third stage amplifiers have sampling capacitor values, device width and bias currents scaled by a factor of 4 w.r.t. the first stage.

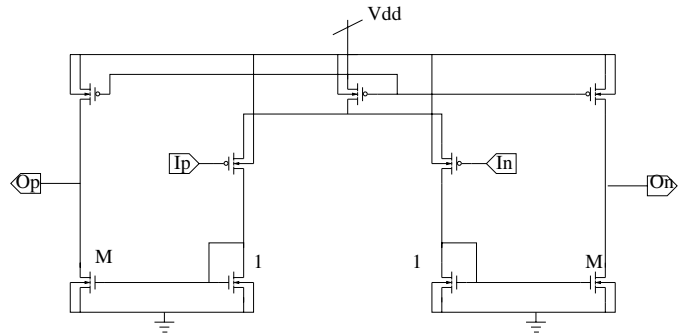


Fig. 3. Current-Mirror Based OTA

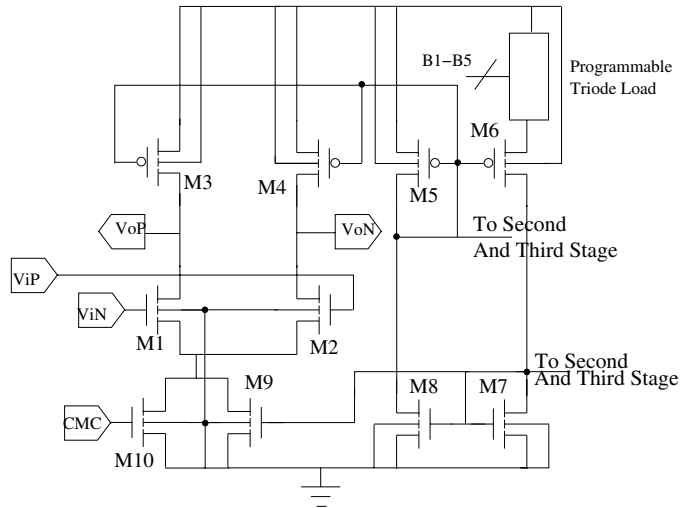


Fig. 4. Circuit Schematic of First OTA and integrated PTAT bias

The speed of the operational amplifiers can be programmed by changing their bias current, determined by a self-referenced current mirror with digitally trimmed triode MOS degeneration that provides a 31:1 ratio of maximum to minimum output current (Fig.4); bias voltages are distributed directly in the voltage domain, so that all integrators share the same speed setting.

The one-bit quantizer is implemented with a comparator composed of an NMOS differential pair preamplifier and a CMOS cross-coupled latch, followed by an S-R flip-flop that prevents metastability effects (See Fig.5). A replica bias circuit with 4 bits of digital control enables the comparator to operate for clock frequencies up to 100MHz.

IV. EXPERIMENTAL RESULTS

A prototype was fabricated in a 90nm 7M2P digital CMOS process with MIM process options from ST Microelectronics using only standard- V_{th} devices. Fig.6 reports a die microphotograph. The active circuitry area is $.11mm^2$, dominated by sampling and integrating MIM capacitors. Chip-On-Board assembly was used for testing purposes.

Fig.7 shows a 65536 points FFT plot of the output of the ADC when the input is short-circuited. No idle tone is

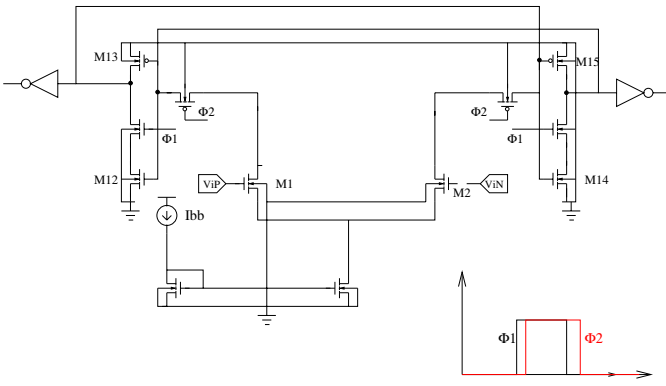


Fig. 5. 1-Bit quantizer simplified schematic and timing

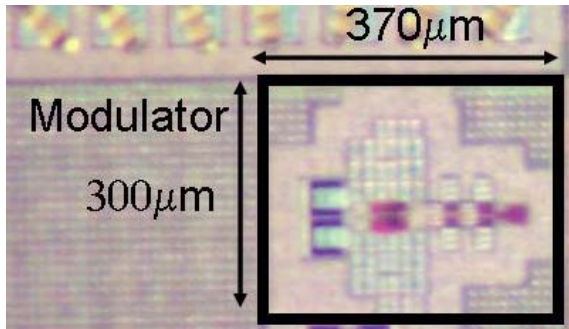


Fig. 6. Die photograph

present. The measured input referred noise corresponds to a 100uV minimum detectable signal (-70dBFS).

In Fig. 8, the output spectrum for an input 6 dB below full scale is shown. The Spurious Free Dynamic range is 63dB, limited by integrator gain nonlinearity; the peak SNDR is 59.5dB (9.75 ENOB).

Fig. 9 displays the SNDR versus input level characteristic. The measured data closely matches system-level simulations, showing the validity of our design methodology. The modulator achieves a dynamic range (DR) higher than 65dB over the 50KHz signal bandwidth. Figure 10, finally, shows the change in converter dynamic range when an out of band tone is applied to the input, against the amplitude of the applied tone. For an out-of-band tone amplitude of 50mV, corresponding to the measured quench residual in [2], the converter always remains stable, and a maximum desensitization of 3dB is obtained in correspondence of a 300KHz input. For higher input frequencies, the converter stable input range and dynamic range degradation are respectively increased and decreased as a consequence of the low-pass characteristic of the signal transfer function. The measured performance is sufficient to support digital demodulation of baseband signals from the receiver in [2]. Increased robustness can be obtained in more demanding applications using the techniques in [8].

The modulator, including bias and digital circuits, draws $42\mu A$ from the 0.65V supply when operating at 100KS/s output rate (6.5MHz clock), consuming $27\mu W$ of power dissipation. Operational amplifiers consume $27.5\mu A$, 65% of the total.

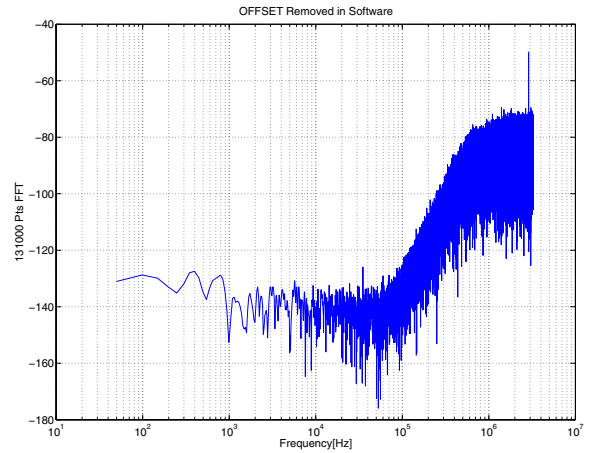


Fig. 7. Modulator noise floor with shorted inputs. The flicker noise corner is approximately 10KHz; no spurious tones are present.

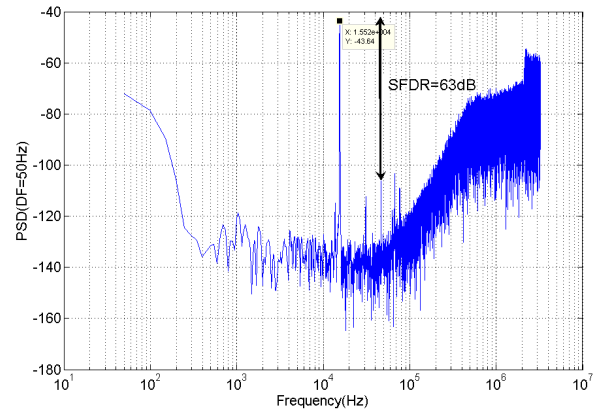


Fig. 8. Output spectrum for -7dBFS input. The tones at 52KHz and 75KHz are caused by instrumentation noise pickup.

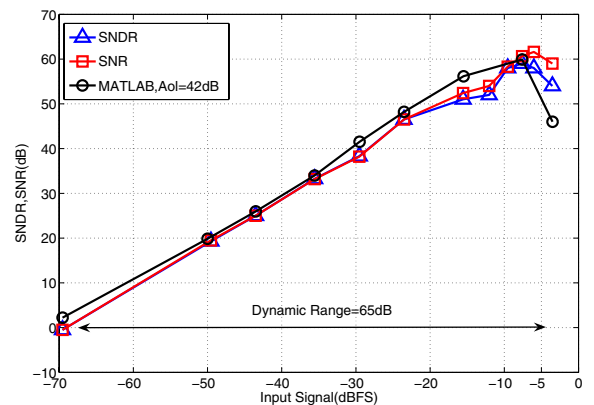


Fig. 9. Signal to noise and distortion ratio versus input level

Ref.	DR[dB]	SNDR[dB]	BW[Khz]	V_{dd} [V]	FOM [pJ/Conv]	FOM_{noise}	Power [μ W]	Process
[9]	74	74	24	0.5	1.63	35e-6	300	0.18 μ
[4]	77	62	16	0.9	1.2	330e-6	40	1.2 μ
[10]	75	67	8	0.7	2.8	52-6	80	0.18 μ
[11]	83	80	10	0.9	1.22	166e-6	200	0.18 μ
[12]	78	78	20	0.6	2.36	25e-6	1000	0.18 μ
[6]	88	83	20	1	.31	1.66e-3	130	0.09 μ
[13]	70	65	300	0.6	8	7.137e-6	7200	0.09 μ
This work	65	59.5	50	0.65	.36	122e-6	27	0.09 μ

TABLE I

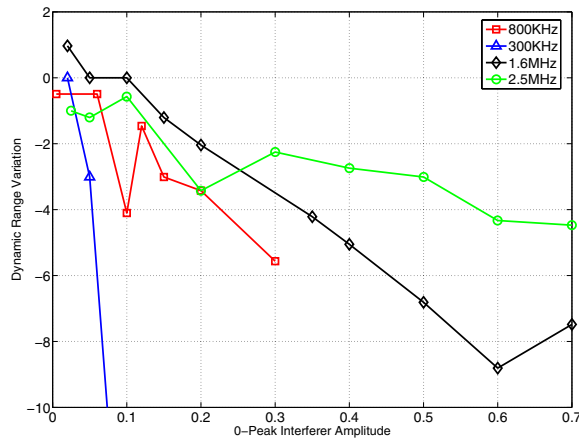
COMPARISON WITH OTHER LOW-VOLTAGE $\Sigma - \Delta$ CONVERTERS

Fig. 10. Measured converter desensitization versus out-of band tone amplitude. The converter full-scale is 0.3V differential.

Bias circuits contribute $5\mu A$, while clock distribution and comparator account for roughly $9.5\mu A$.

V. CONCLUSIONS

We presented a low-power, low-voltage $\Sigma - \Delta$ modulator. The measured results show that $\Sigma - \Delta$ modulators can be used to perform moderate or high-resolution digitization at microwatt power levels with power efficiency comparable to that of successive-approximations counterparts ([1]), while naturally enabling higher receiver digitization and better performance.

In Tab.I, this work is compared to other recently published low-voltage, low-power oversampled converters with $\geq 60dB$ Dynamic Range using the widely accepted metrics of ISSCC figure of merit $FOM = \frac{P_d}{BW^2 ENOB}$ and the normalized noise-limited figure of merit $FOM_{noise} = \frac{4KT10^{DR/10} BW}{P_d}$. This design attains an FOM of 0.36pJ/Conv.Step. which to the author's knowledge is the lowest reported to date for designs operating strictly below 1V. This high level of power efficiency is obtained by choosing the simplest possible circuit implementation compatible with the target specifications for the modulator critical building blocks.

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