

A 1 V 250 KPPS 90 NM CMOS PULSE BASED TRANSCEIVER FOR CM-RANGE WIRELESS COMMUNICATION

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ABSTRACT

We present a baseband pulse based transceiver for centimeter range wireless communication. It is implemented in 90nm CMOS technology and uses a $0.5cm^2$ on board inductor as antenna to reduce cost and minimize size. All the timing information is extracted from the incoming pulse sequence by means of an on-chip Phase Locked Loop whose output is used to duty cycle the receiver and drive the transmitter, obviating the need for an on board quartz reference. The complete system integrates front end, antenna and clock-recovery in a single module with cm^2 size. At 250Kpps, the transceiver consumes $257\mu W$ ($6\mu W$ TX, $181\mu W$ RX, $70\mu W$ PLL), corresponding to an energy consumption of 1nJ/Pulse.

I. INTRODUCTION

Advanced packaging/assembly technologies and implantable systems drive the demand for very low-power communication systems with range limited to a few centimeters. In this scenario, radiative field propagation is unavailable and links operate in the near field regime unless carrier frequencies in the multi-GHz range are used. In this work we adopt a baseband pulse-based approach, similar to the one presented in [1] for chip to chip communication. Data transfer is realized through on board inductors much smaller than the free space quarter-wavelength at the pulse center frequency, resulting in electrically small loops [2].

II. TRANSCEIVER OVERVIEW AND DESIGN CONSTRAINTS

In a pulse based communication system with low data rate the information is concentrated in narrow time slots with respect to the pulse repetition period and the average power consumption of the receiver is reduced by means of duty cycling ([3], [4]). The total power dissipation reads

$$P_{av} = P_{on} \frac{\alpha T_{pulse}}{T_{bit}} + P_{synch} \quad (1)$$

where P_{on} is the peak active power, $\alpha > 1$ is the ratio of the system on time to pulse duration, and P_{synch} is the synchronization overhead, i.e. the power required to

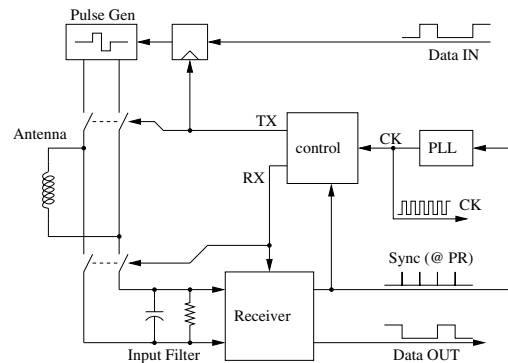


Fig. 1. Transceiver block diagram

generate the the low jitter clock of the node, that has to be constantly active to generate the duty cycling signals. Conventionally, P_{synch} is minimized at the expense of integration, size and cost by using an on-board crystal-stabilized oscillator. In this work, to achieve the maximum level of integration and avoid the use of a precise local oscillator on each node, we employ a Phase Locked Loop (PLL) that locks the local time base to the incoming signal. After a $\approx 100ms$ -long training phase, in a strongly connected network global synchronization is obtained by locking all the nodes to a small set of master nodes provided with a reduced set of crystal oscillators. A block diagram of the transceiver is shown in Fig. 1.

II-A. Transceiver operation and architecture selection

The transmitter operates by forcing a signed square pulse $V(t)$ limited by the supply on the loop (See Fig. 2 for the time domain voltage and current waveforms and the voltage spectrum). Bi-phase modulation is used to simplify clock recovery. The 85% power bandwidth bandwidth of the signal is given by 2 divided by the pulse duration τ , while the peak current flowing into the inductor is given by $I_{MAX} = V\tau/(2L)$.

Being k the coupling factor between the transmitter and the receiver antenna, the amplitude of the received voltage

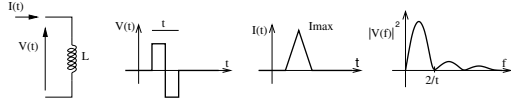


Fig. 2. Transmitter signal waveforms

pulse is given by $kV(t)$. Since the transmitted pulse shape is bandpass (as shown in 2), a low-Q passive LC filter with inductance fixed by the receive loop limits the receiver bandwidth to $2/\tau$, and fixes the received peak voltage over effective noise ratio to the value given in Eq. 2.

$$SNR = \frac{V_r}{N_r} \approx \frac{k\alpha V}{KT/C} \quad (2)$$

Here KT is the Boltzman constant multiplied by the absolute temperature and C the receiver filter capacitance. For a fixed peak current in the transmitter, a larger inductor results in both a larger coupling factor [1], and a narrower bandwidth, quadratically improving SNR. In this design, the stringent size constraint led to the selection of an on-board 3-turns 8.1 mm-diameter circular inductor. An inductance of 76 nH, and a self resonance around 800 MHz were measured. The estimated coupling factor is $k = 10^{-4}$ (-80 dB) for 2 inductors in free space laid out on the same plane at 5 cm distance. Obtaining a 13 dB SNR at the receiver requires a pulse duration of 3 ns, giving a peak current of 20 mA in the transmitter. Assuming a 1 V supply in the transmitter, the received peak signal at 5 cm distance is therefore as small as $100 \mu\text{V}$ (-80 dBV).

III. TRANSCEIVER IMPLEMENTATION

The designed energy-detection transceiver architecture was shown in Fig. 1.

III-A. Transmitter

The transmitter, shown in Fig. 3 is realized with a MOS bridge that directly drives the inductor.

The duration of the pulse is adjusted by means of digitally controlled delay lines. To save power the delay lines are biased only 1 Clock period prior to the pulse and kept active for 2 Clock periods. Because of the impulsive nature of the current with a 20 mA peak, the transmitter supply is filtered by an RC filter; the 600 pF on-chip capacitor is realized by means of metal-insulator-metal and MOS capacitors to maximize density.

III-B. Receiver

The receiver, whose block diagram is shown in Fig. 4, should detect the $100 \mu\text{V}$ pulse across the LC filter. In order to avoid the power overhead contributed by the generation of a Nyquist-rate sampling clock, and the complexity of multiple parallel paths, a sampling architecture [4] is avoided and an energy-detection scheme

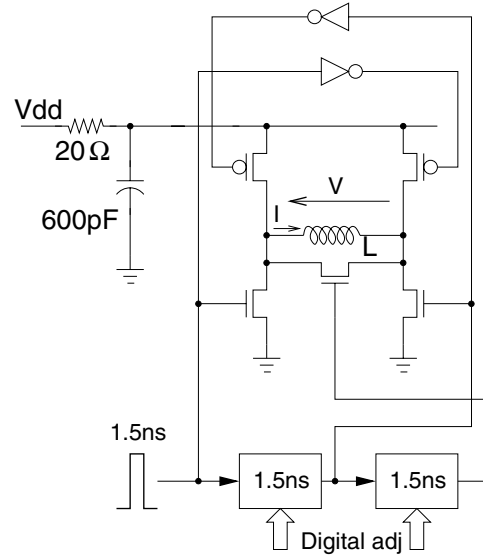


Fig. 3. Transmitter schematic

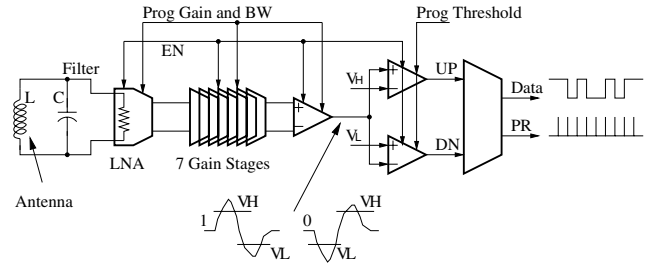


Fig. 4. Receiver Schematic

is implemented [5]. To minimize the accuracy and jitter requirements of the duty cycling signal, an activation time substantially longer than the pulse duration is chosen. The received signal is filtered by a wide band LC parallel resonator ($f_0 = 205 \text{ MHz}$, $Q = 0.8$) designed to maximize the peak voltage over the effective noise. This results in a 13 dB SNR on the tank with 10^{-4} coupling factor. A hybrid common gate shunt feedback LNA [6] simultaneously synthesizes a shunt conductance that damps the LC antenna filter response and provides a first stage of wideband gain. Seven more stages of fully-differential wideband gain further regenerate the signal to the rails, before it is converted to single-ended format and thresholded by two continuous-time comparators. The LNA is biased at $400 \mu\text{A}$ to get the desired input resistance of 78Ω , with a simulated gain of 21 dB on a 20-950 MHz band. The gain stages are realized as differential pairs with resistive loads, and have been optimized to maximize the ratio of gain(dB) to bias current over the signal bandwidth. The nominal bias current is $300 \mu\text{A}$ for a gain of 8.8 dB and a 3 dB cut-off frequency of 3 GHz. AC-coupling and

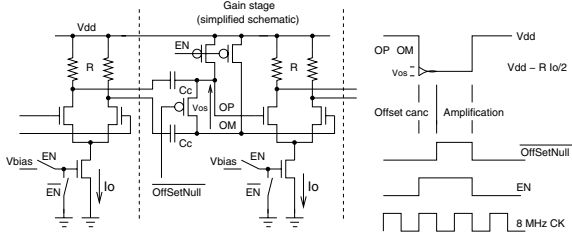


Fig. 5. Differential Gain Stage; duty cycling and offset cancellation

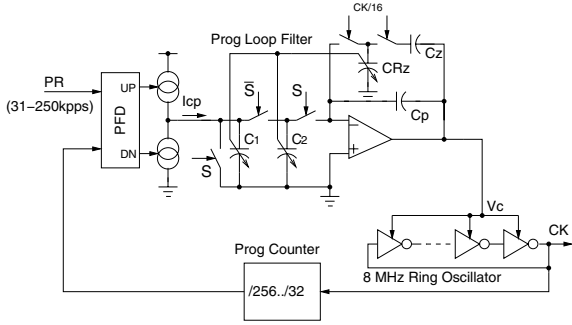


Fig. 6. Phase Locked Loop

offset cancellation are used throughout the gain chain to maximize dynamic range. The differential stage schematic and the offset cancellation technique, together with the duty cycle timing are shown in Fig. 5.

In the duty cycled mode each stage is activated by then EN signal for 1 and half CK period every pulse period, giving an average current consumption of $98 \mu\text{A}$ at 250 kpps with an 8 MHz clock for the 7 stages. Because of its longer set up time, the LNA is activated half clock period in advance, increasing its average power consumption to $50 \mu\text{A}$.

III-C. Synchronization

The received signal is used to synchronize the 8 MHz PLL sketched in Fig. 6. The PLL is the only time base available on the node and provides the clock to the transmitter and the receiver. To achieve a fully integrated implementation with small filter capacitances C_p and C_z , the effective charge pump current ($I_{cp} = 1 \mu\text{A}$) is scaled by C_1 and C_2 and only a fraction of the charge injected into the loop filter. This results in an minimum effective current of 62.5 nA and a total PLL capacitance of only 250 pF . The filter resistance is realized with the switched capacitor C_{Rz} driven by two non overlapping phases at $1/16$ of the 9-stage ring VCO frequency. In order to minimize the static phase error, the OPAMP input referred offset is canceled.

The PLL is programmable to lock on pulse rates from 31.25 to 250 kpps and produces a time resolution for duty

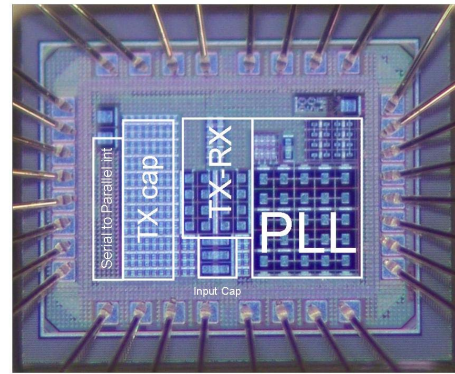


Fig. 7. Chip photograph

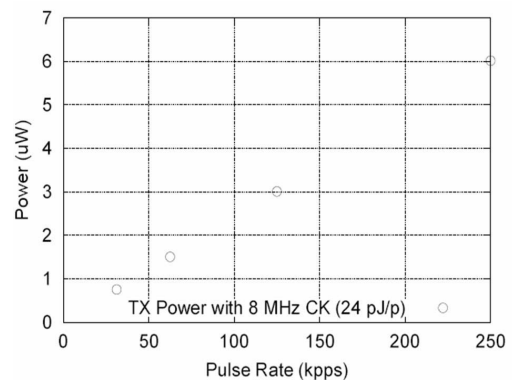


Fig. 8. Transmitter power consumption at low pulse rates with 8 MHz clock and 2 periods of duty cycling

cycling equal to a clock period (125 ns), as shown in Fig. 5.

IV. EXPERIMENTAL RESULTS

The transceiver has been implemented in 1P7M 90 nm STMicroelectronics CMOS process with $V_{dd} = 1\text{V}$. The die size is 0.9 by 1.1 mm and its annotated photo is shown in Fig. 7.

IV-A. Transmitter characterization

Due to the simple operation and the very low duty cycle, the energy consumed by the transmitter is minimal. A $52.4 \mu\text{A}$ bias current is required by the adjustable delay line, while 10.86 pJ are required by the bridge for the pulse generation (including the bridge drivers). The transmitter power consumption at different pulse rate is shown in Fig. 8. At 250Kbps, the average energy consumption is 24 pJ/Pulse .

The transmitter can support even higher pulse rates, showing improved energy efficiency. At 50 Mpps for

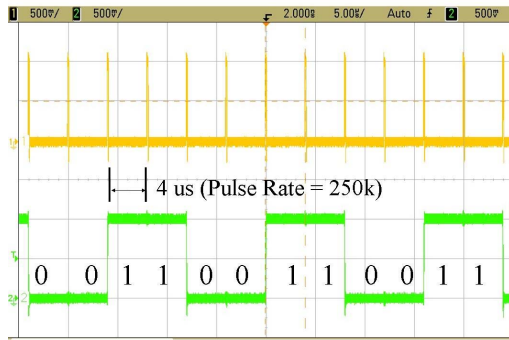


Fig. 9. Receiver Synchronization Pulse and Received Data at 250 kpps (Transmitted sequence = 00110011)

example a power consumption of 596 μW , corresponding to an average energy dissipation lower than 12pJ/Pulse, has been measured.

IV-B. Receiver Characterization in loopback

The transceiver characterization was limited by two different problems. First, the lines necessary to interface with the transceiver and to read the data cause a change in the magnetic field distribution, reducing the inductors coupling factor. Due to this effect, the longest-range wireless channel achieved was established by placing the inductors facing each other and at reduced distance of 1cm.

Second, the current charging instrumentation capacitance produces a magnetic field that concatenates with the receiver antenna causing an increase in BER. This self-interference could be attenuated by separating in time the receiver operation and the output pad switching, but still was an issue for testing of this first implementation.

A complete transceiver characterization was then performed for loopback mode. In this mode, the transmitter directly feeds the receiver by means of an attenuator. To achieve the maximum attenuation the on-board inductor has been shorted and its terminal and the transmitter directly feeds the receiver on the same chip. In these conditions, both detection and synchronization were successful. Figure 9 shows the data received when the transmitted sequence is “0011”, together with the duty cycle signal of 125 ns that activates the receiver.

Measured data on the transceiver are summarized in Table I. Without duty cycling a maximum pulse rate of 50 Mpps, partially limited by the test equipment, has been found.

V. CONCLUSION

We reported a CMOS baseband pulse-based transceiver for centimeter-range wireless communications. Loopback

Pulse Rate	50 M	250 k	125 k	62.5 k
Duty Cycle	1	1/32	1/64	1/128
Power (μW)				
PLL	70	70	70	70
TX	565	6	3	1.5
RX	3600	181	103	61.1
Total	4153	257	176	133
Epulse TX (pJ/p)				
Epulse TX (pJ/p)	11.3	24	24	24
Epulse RX (pJ/p)				
Epulse RX (pJ/p)	72	720	820	980

Table I. Transceiver power consumption (and Energy per pulse) for different pulse rate

test shows that a communication at 250 kpps can be established with 7 μW (24 pJ/bit) in the transmitter, 181 μW (720 pJ/pulse) in the receiver plus 70 μW for the PLL provides the transceiver synchronization on the incoming pulse sequence. The transceiver does not rely on a precision crystal oscillator, and is therefore suited to ultra-low cost, ultra-low power applications. The achieved energy dissipation of 1nJ/Pulse, while including the synchronization overhead, is comparable or better than that of other state-of-the-art UWB implementations ([4],[3]) operating at higher pulse rates.

VI. ACKNOWLEDGEMENTS

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