CMOS Power Amplifier Linearization for Wireless Communications

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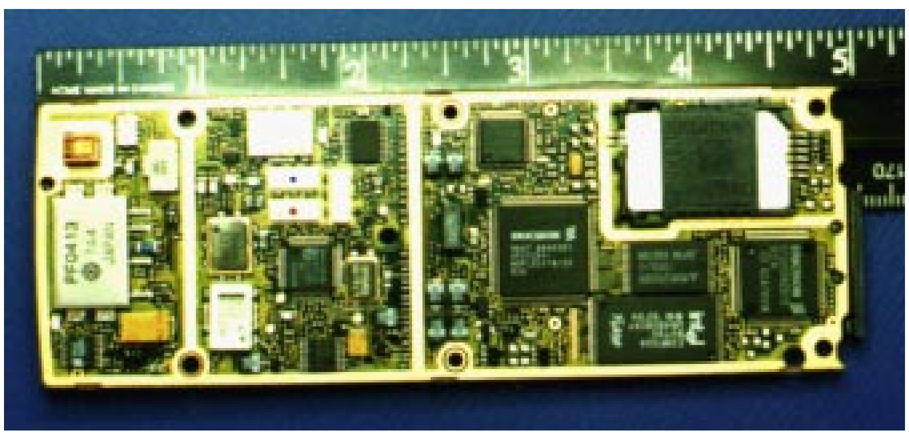
BWRC Summer Retreat
June 3, 2002

Why CMOS RF?

- **Because we can**
  - progress in device performance enables high-frequency operation - 0.18μm CMOS F_t=60GHz
- **Low Cost**
  - economy of scale for digital ICs - ~90% of ICs shipped are CMOS
- **High Integration**
  - sharing technology with digital circuitry
  - System on a Chip



Potential CMOS Implementation

CMOS Power Amplifier Challenges

Most transceiver blocks have been demonstrated, but Power Amplifier remains a problem

- **Low breakdown voltages**
- **Low current drive**
- **Lack of High-Q passives**

Power efficient CMOS PAs have been demonstrated but have poor linearity

Summary of Wireless Standards

Radio Standard	Year Launched	Data Rate (raw)	Channel Spacing	bps/Hz	Modulation
AMPS	1983		30kHz		FM
GSM	1991	270.8kbps	200kHz	1.354	GMSK
DECT	1992	1.152Mbps	1.728MHz	0.66	GFSK
IS-95	1996	1.2288Mbps	1.25Mhz	0.983040	QPSK
IS-54/136	1997	48.6kbps	30kHz	1.62	π/4 DQPSK
802.11a	2002	72Mbps	20Mhz	3.6	64QAM OFDM
GSM/EDGE	2002?	812.5kbps	200kHz	4.06	8-psk

- **New applications demand linear amplification for spectral efficiency**

The Problem:

How to meet High-Linearity Requirements in a Power Efficient CMOS RF Power Amplifier

Proposed Solution:

Linearization

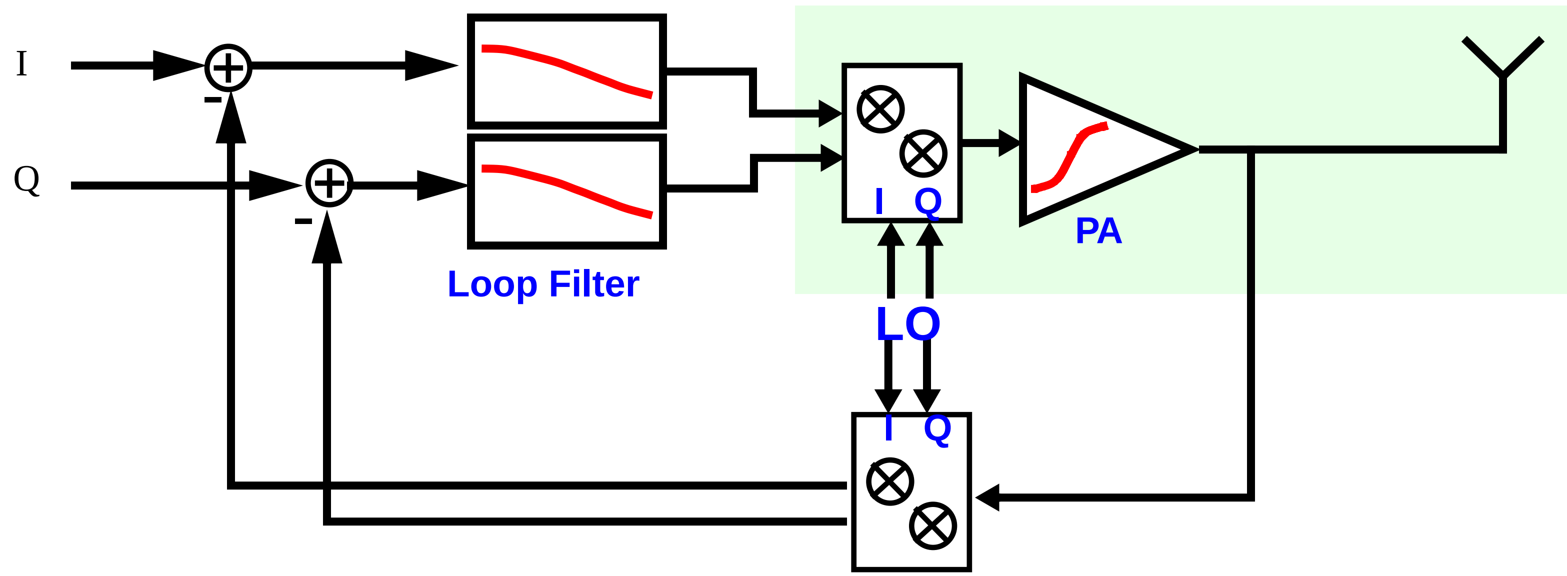
- **Understand system-level considerations and identify design guidelines**
- **Examine implementation issues for integration in CMOS**

Linearization Techniques

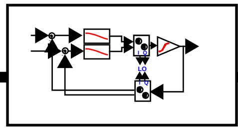
- Linear class A amplifier
- Predistortion
- LInear amplification with Nonlinear Components (LINC)
- Feedforward
- Envelope Elimination and Restoration (EER)
- Feedback

- poor power efficiency
- need to track shifts in amplifier linearity
- need to synthesize baseband signals with bandwidths wider than channel bandwidth
- need to efficiently sum different PA outputs
- need to match different signal paths
- need wide bandwidth DC/DC converter
- stability is an issue

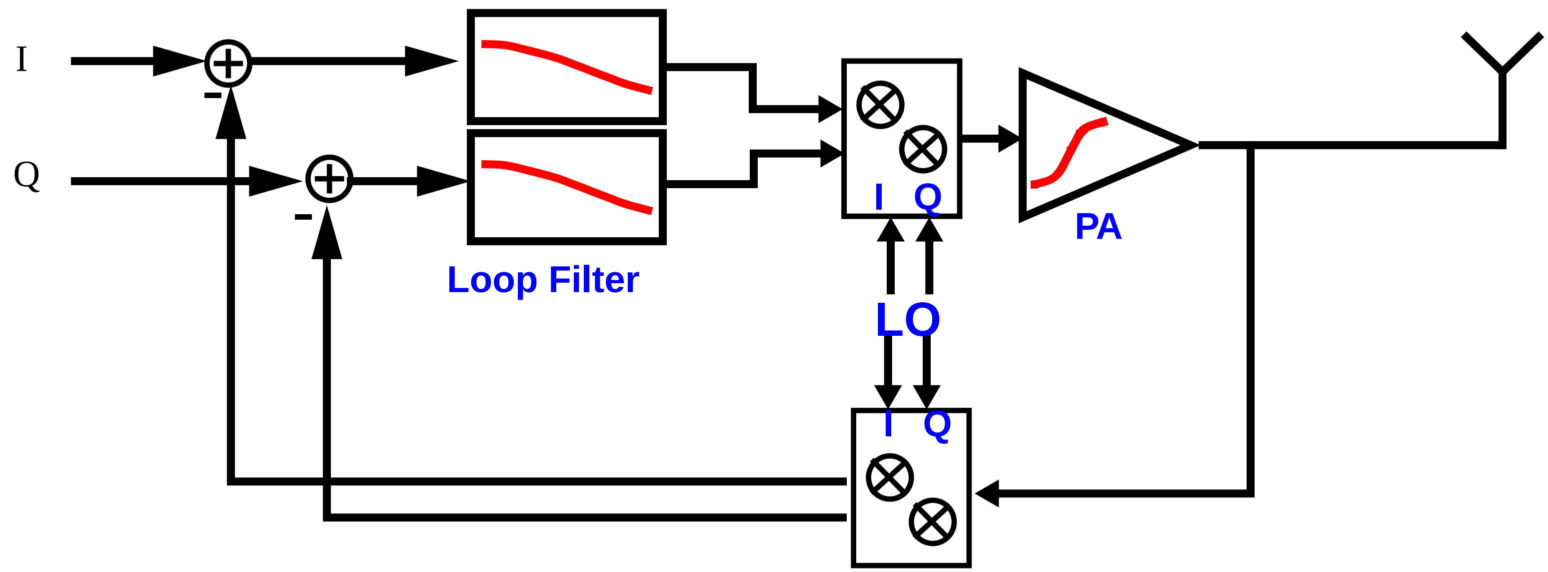
Cartesian Feedback Architecture



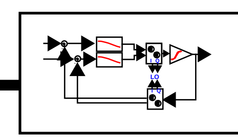
- Feedback forces output to track input
- Linearity performance relies on feedback mixer rather than PA
- Mixer linearity easier to achieve due to lower power levels



Feedback Issues

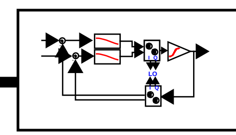


- Loop Filter design must trade stability and error suppression
- Excessive distortion from PA can cause loop instability
- Stability with highly nonlinear amplifier has not been well understood

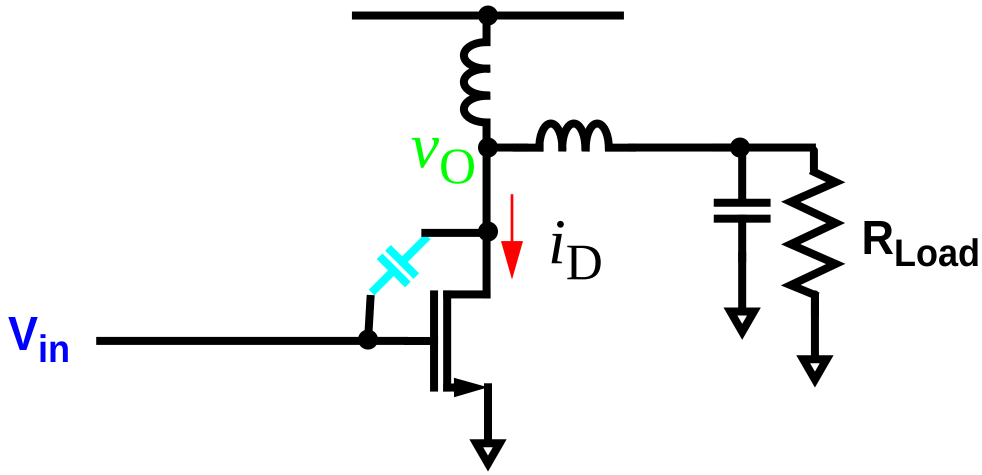


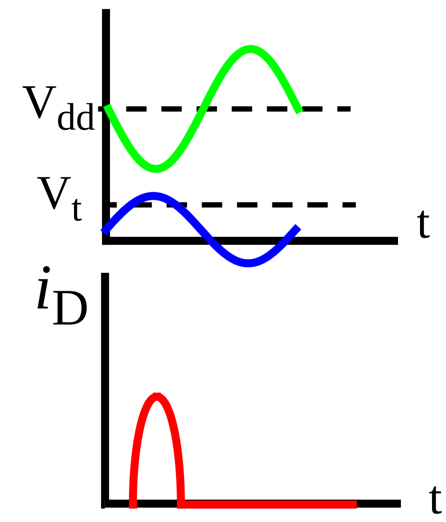
Circuit Challenges

Problem		Approach
• **Class C AM/PM distortion**	→	• **Class C+AB amplifier**
• device stacking limited by supply	→	• baseband current folding
• downconversion linearity and 1/f noise	→	• hybrid active/passive downconversion mixer
• loop filter gain/stability tradeoff and device tolerance sensitivity	→	• passive lead/lag compensation topology

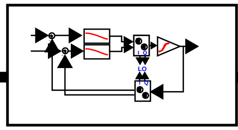


Class C Power Amplifier

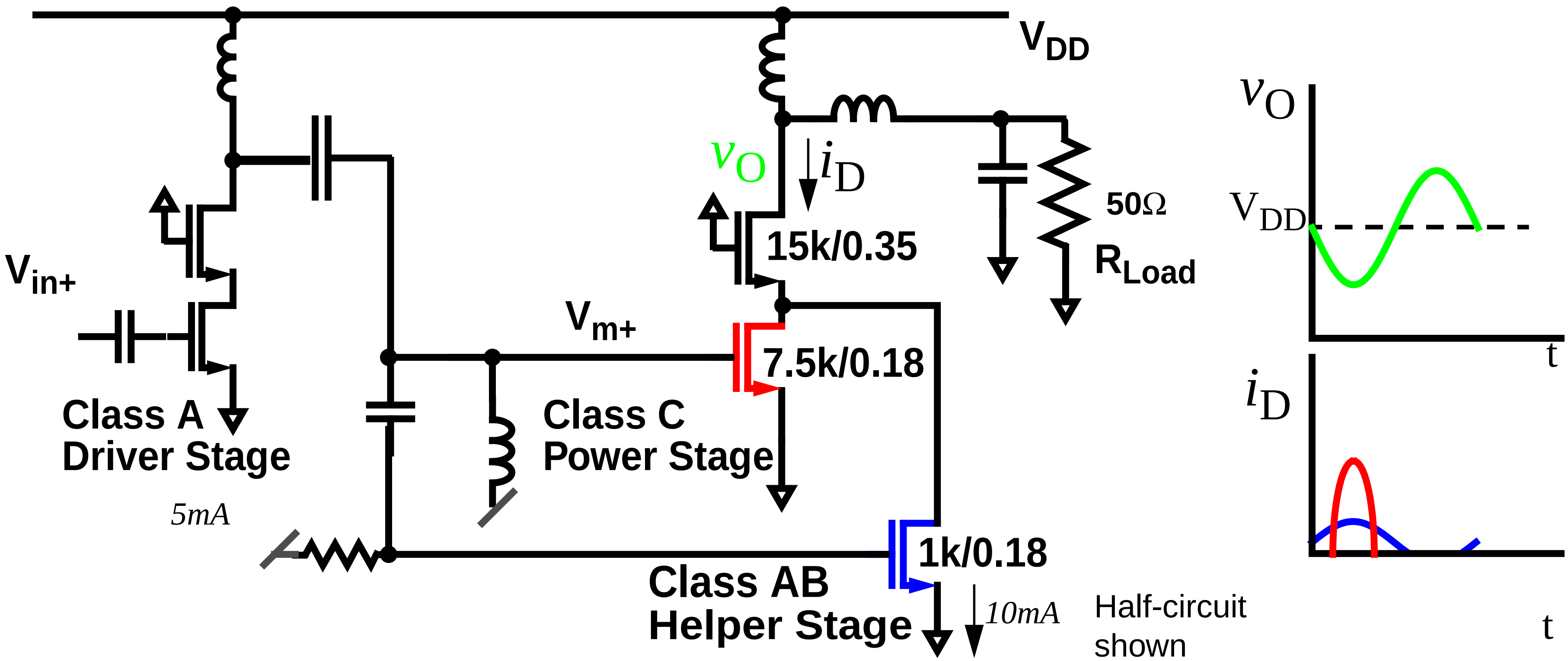




- **Class C amplifier allows envelope modulation and offers good power efficiency**
- ***Problem for feedback*****: at low amplitudes transistor does not turn on, but capacitive feedthrough is noninverting**



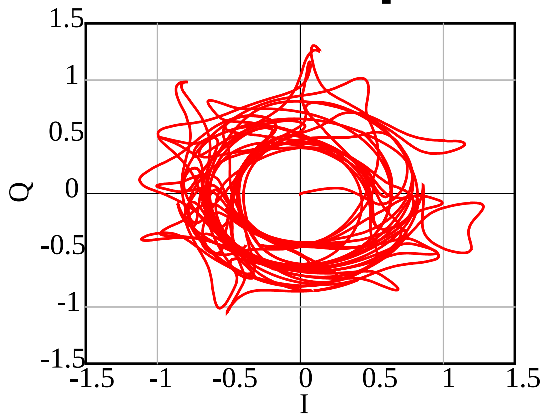
Class C+AB Power Amplifier



- Cascode device protects transconductor from wide output swing
- Class AB stage offers gain for small input signals to prevent overall phase shift
- Peak efficiency ~55% for 1W (two-sides)

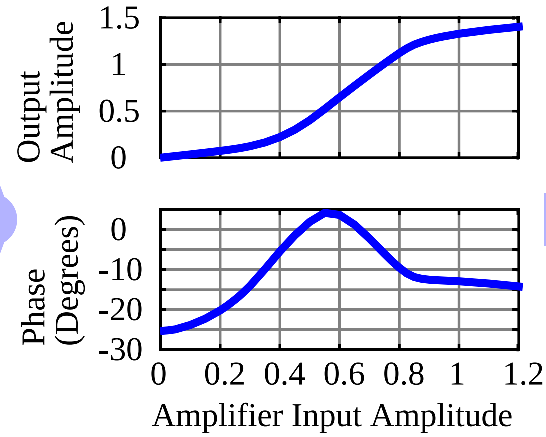
Closed-Loop Simulation Results

Upconversion Mixer Input

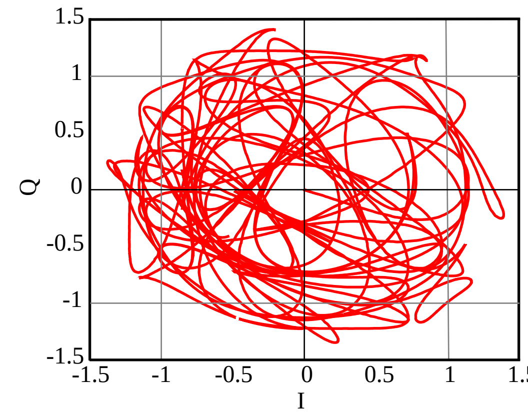


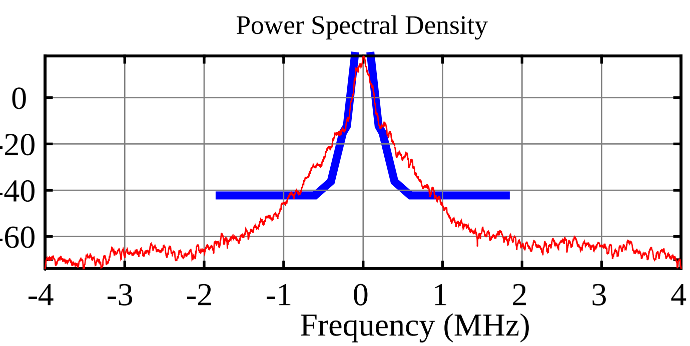
Amplifier

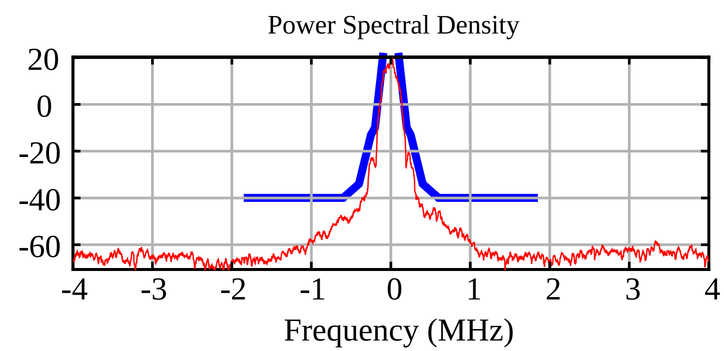
AM/AM & AM/PM



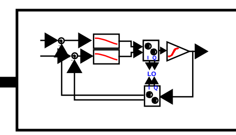
Output







- Behavioural simulation of loop with PA model extracted from Spectre simulations
- Overall power efficiency ~38% for 500mW (mean) output

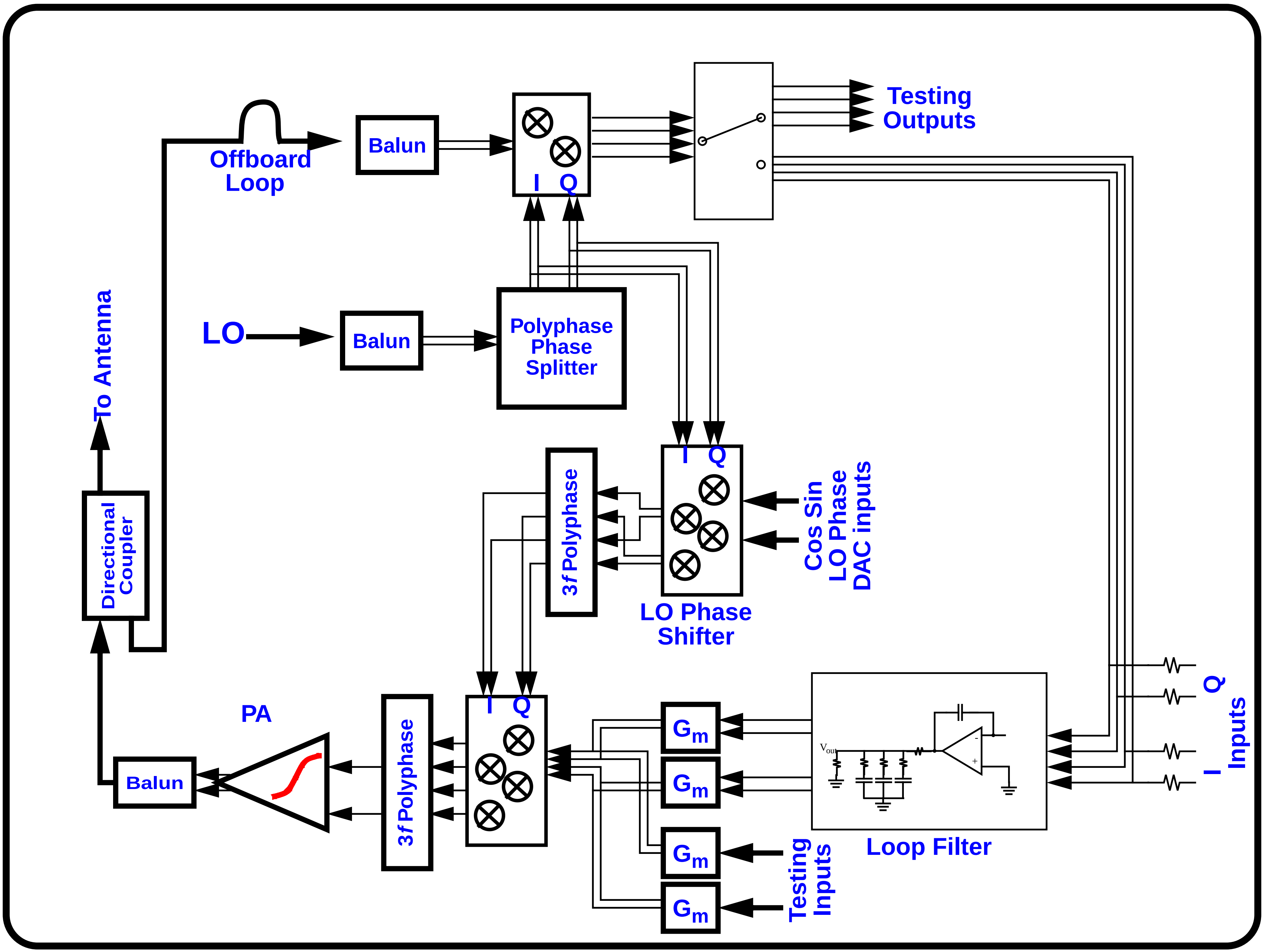


Expected Research Contributions

Demonstrate that High Transmitter Linearity can be achieved with an integrated non-linear power-efficient CMOS PA

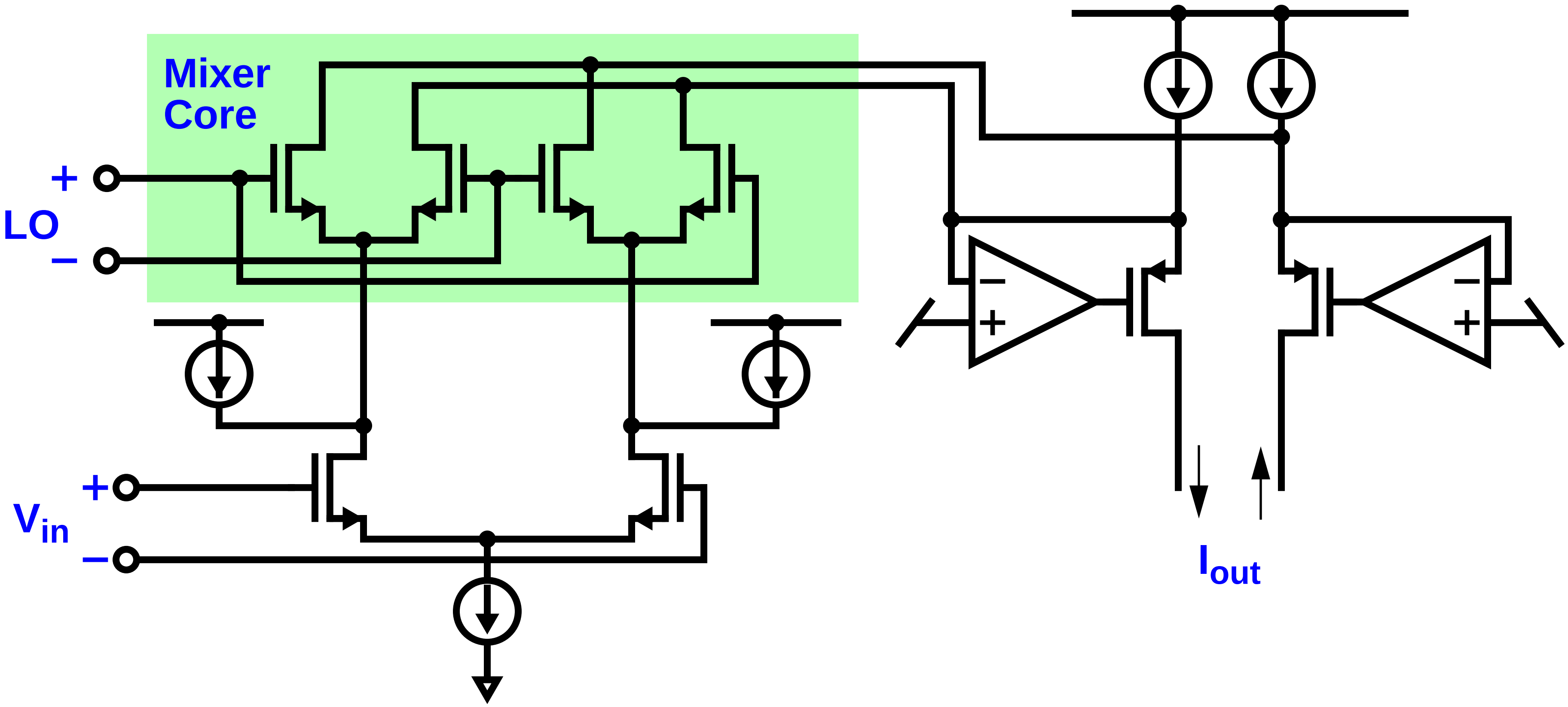
Prototype allows CMOS PA to meet DCS 1800 EDGE specifications with good power efficiency

Just in case... (Q+A)



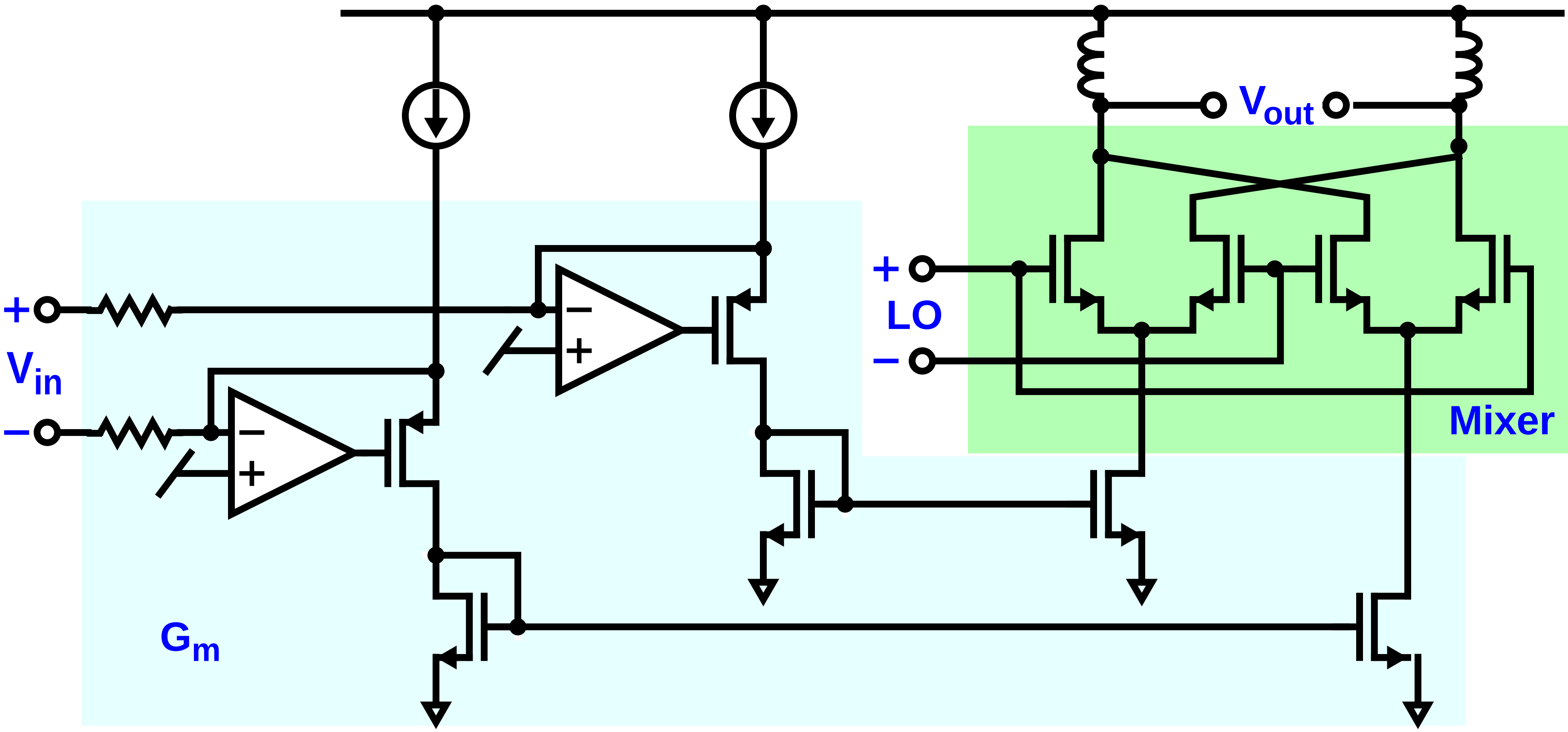
Offboard Loop
Balun
I Q
Testing Outputs
LO
Balun
Polyphase Phase Splitter
To Antenna
I Q
Directional Coupler
3f Polyphase
Cos Sin LO Phase DAC inputs
LO Phase Shifter
PA
Balun
3f Polyphase
I Q
Gm
Gm
Gm
Gm
Testing Inputs
Loop Filter
Q
I
Inputs

Hybrid Active/Passive Downconversion Mixer

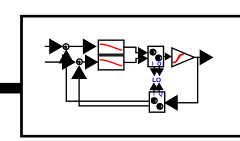


- Current bleeds eliminate DC bias current in switch transistors, reducing 1/*f* noise
- Active cascode ensures low load impedance for switch devices, enhancing linearity

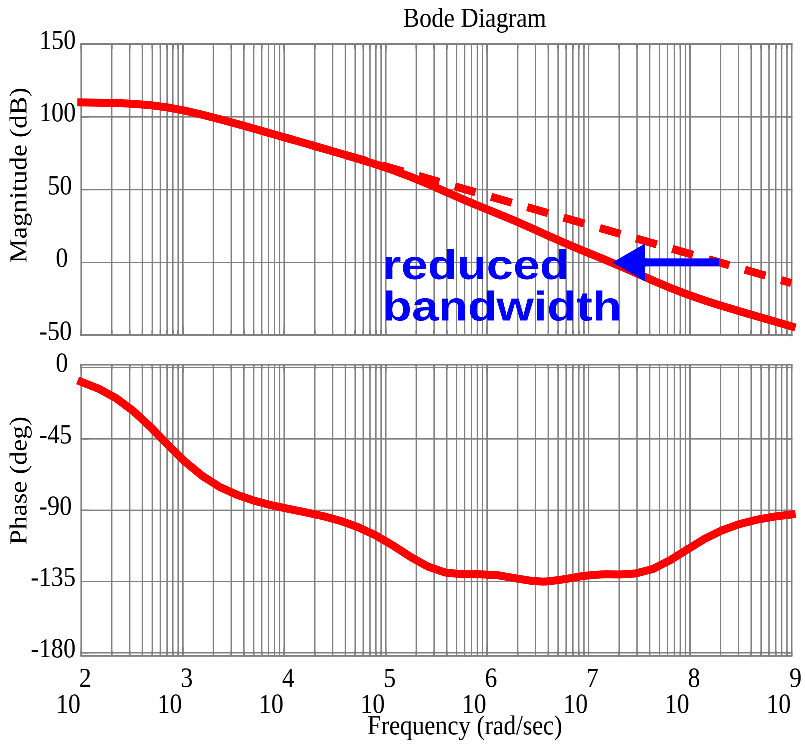
G_m/Current Commutating Upconverter

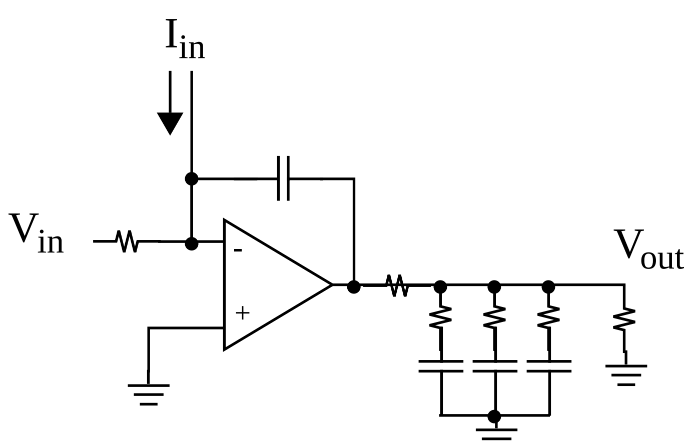


- Improve linearity by taking advantage of baseband techniques for input



Loop Filter Design

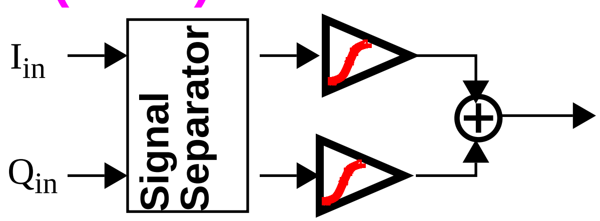




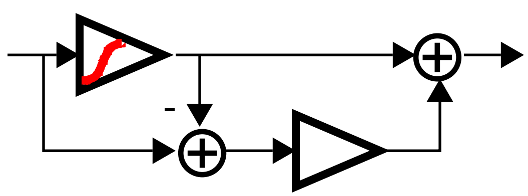
- Extra pole/zero pairs (lead/lag compensation) trade phase margin for faster gain rolloff and better gain insensitivity
- Active integrator presents low impedance to down-conversion mixer for good linearity
- Passive lead/lag network insensitive to bottom plate capacitance and resistor tolerance

Other Linearization techniques

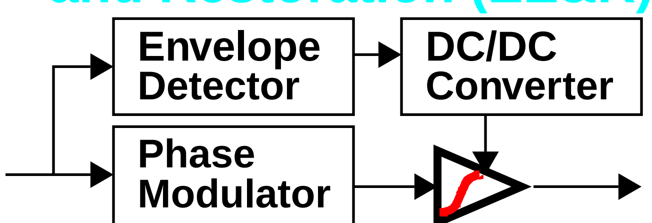
- Predistortion
- LInear amplification with Nonlinear Components (LINC)



- Feedforward



- Envelope Elimination and Restoration (EE&R)



- need to track shifts in amplifier linearity
- need to synthesize baseband signals with bandwidths wider than channel bandwidth
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- need to match different signal paths
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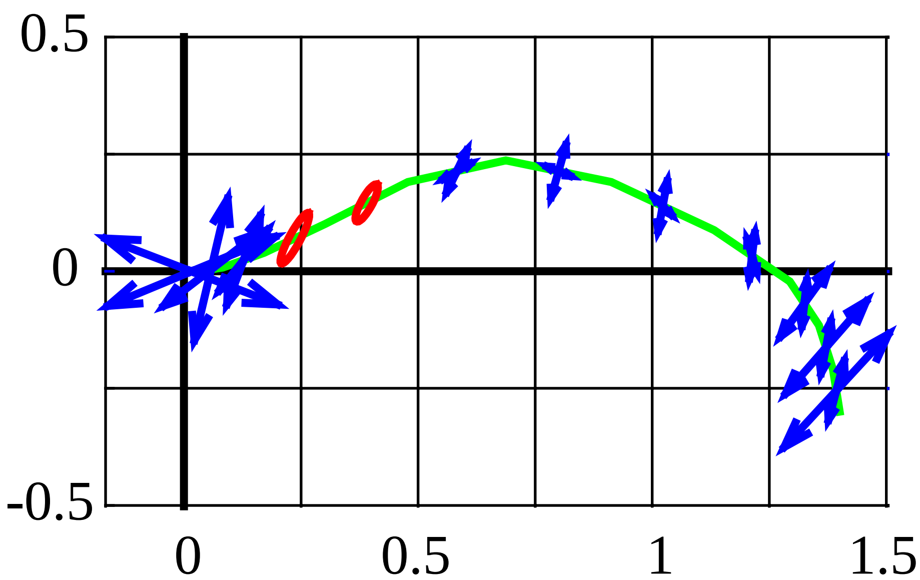
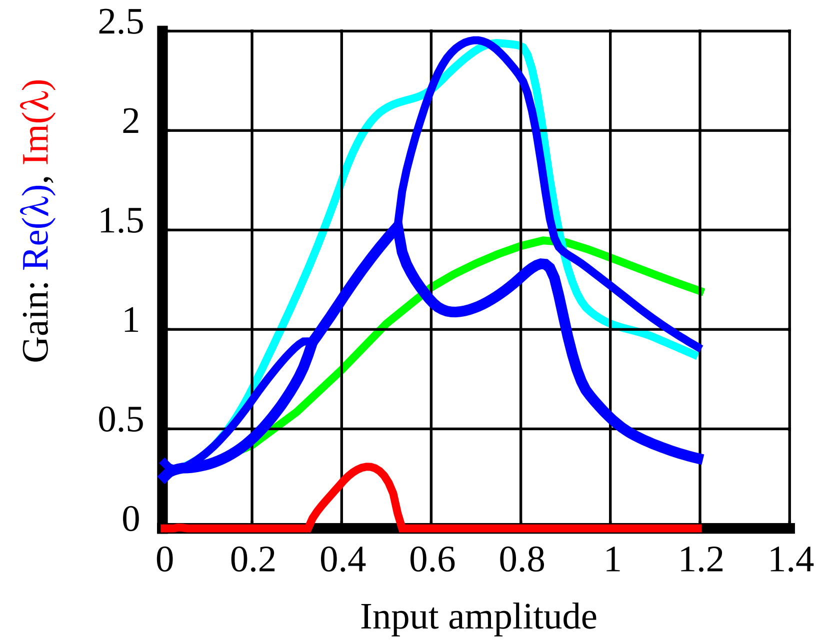
Eigenvectors/eigenvalues for PA





- **small signal gain can be as much as 2.5x nominal large signal gain**
- **with single pole loop filter, bandwidth could be as much as 90MHz at RF - narrowband assumptions may be questionable**