

A 52 μW Wake-Up Receiver With -72 dBm Sensitivity Using an Uncertain-IF Architecture

Nathan M. Pletcher, *Member, IEEE*, Simone Gambini, *Student Member, IEEE*, and Jan Rabaey, *Fellow, IEEE*

Abstract—A dedicated wake-up receiver may be used in wireless sensor nodes to control duty cycle and reduce network latency. However, its power dissipation must be extremely low to minimize the power consumption of the overall link. This paper describes the design of a 2 GHz receiver using a novel “uncertain-IF” architecture, which combines MEMS-based high-Q filtering and a free-running CMOS ring oscillator as the RF LO. The receiver prototype, implemented in 90 nm CMOS technology, achieves a sensitivity of -72 dBm at 100 kbps (10^{-3} bit error rate) while consuming just 52 μW from the 0.5 V supply.

Index Terms—BAW resonator, sensor networks, ultra-low power, wake-up receiver.

I. INTRODUCTION

WIRELESS SENSOR NETWORK (WSN) applications, such as building monitoring, ambient intelligence (AmI), and personal area networks (PAN), require highly integrated electronics for reduced size and cost, combined with low power consumption for extended battery life. In order to reduce power consumption, sensor nodes are typically heavily duty-cycled, spending most of the time in a low power sleep mode. In order to communicate, two neighboring nodes must have a method for activating their wireless communication simultaneously, introducing a challenge for synchronization. There are several ways of solving this problem. A synchronous protocol can be implemented by maintaining a global clock across all nodes in the network and assigning timeslots to individual nodes. Alternatively, asynchronous methods avoid the need for global synchronization by using a request-based protocol to control duty-cycle and set up communication between nodes. With protocol-based duty-cycle control, the receiver uses a timer to periodically listen to the channel for communication requests. When the transmitter wants to communicate, it repeatedly sends requests until the two happen to coincide in time (Fig. 1(a)). Both synchronous and asynchronous methods exhibit a clear trade-off between power consumption and latency.

In order to break this trade-off, a fully asynchronous protocol can be implemented using a dedicated auxiliary receiver called a wake-up receiver (Fig. 1(b)). The wake-up receiver (WuRx) continuously monitors the channel for requests and activates

the receiver [1]. Because the WuRx is listening continuously, latency is reduced substantially. The WuRx is not duty-cycled, however, so its active power consumption must be very low to avoid dominating the overall average power of the link. Minimizing the active power consumption differs from typical duty-cycled receiver design for WSN, where energy efficiency (energy per received bit) should be optimized. The power specification for the WuRx depends on many factors, such as the main receiver characteristics and the level of packet traffic in the network. For typical WSN conditions, power modeling indicates that the active power consumption of the WuRx should be less than 100 μW [2]. The challenging power specification represents around an order-of-magnitude reduction over previously published receivers for sensor networks [3]–[5]. In this paper, we present a receiver designed specifically for the wake-up application, which employs a novel architecture to achieve significant power reduction.

First, an overview of potential receiver architectures is summarized in Section II, along with a discussion of the factors limiting performance and power reduction. Section III then describes the “uncertain-IF” architecture and outlines the design considerations and trade-offs particular to this architecture. The implementation details and circuit design of each block in the receiver are presented in Section IV, followed by measurement results from a prototype implementation (Section V). Finally, Section VI summarizes the work and places it in context with other research on low power wireless receivers.

II. RECEIVER ARCHITECTURES FOR LOW POWER

A. Frequency Conversion Architectures

Most wireless receivers utilize a frequency conversion architecture in which selectivity is achieved through careful frequency planning, combining narrowband low frequency responses with frequency-converting mixers and high purity oscillators. For example, the super-heterodyne architecture (Fig. 2(a)) utilizes two separate downconversion operations. The RF signal is converted to intermediate frequency (IF) with a high-accuracy, tunable LO. The IF signal is amplified and filtered with a fixed frequency filter to remove the image and interferers. A second mixer converts the signal to DC using a fixed frequency oscillator at the IF frequency. The advantage of frequency conversion is that gain and selectivity can be realized at lower frequencies, resulting in lower power consumption and improved performance.

For frequency conversion architectures, power consumption is often limited by the RF oscillator. The stringent frequency accuracy and phase noise requirements almost invariably require a resonant LC oscillator embedded in a phase-locked loop. For an LC oscillator, the limited quality factor (Q) of integrated

Manuscript received April 16, 2008; revised July 24, 2008. Current version published December 24, 2008. The authors wish to acknowledge the support of the Berkeley Wireless Research Center students, faculty, and sponsors, NSF Infrastructure Grant 0403427, the Gigascale Systems Research Center, and the California Energy Commission

N. Pletcher is with Qualcomm Inc., San Diego, CA 92121 USA (e-mail: nathanp@qualcomm.com).

S. Gambini and J. Rabaey are with the Department of Electrical Engineering and Computer Sciences, University of California, Berkeley, CA 94704 USA.

Digital Object Identifier 10.1109/JSSC.2008.2007438

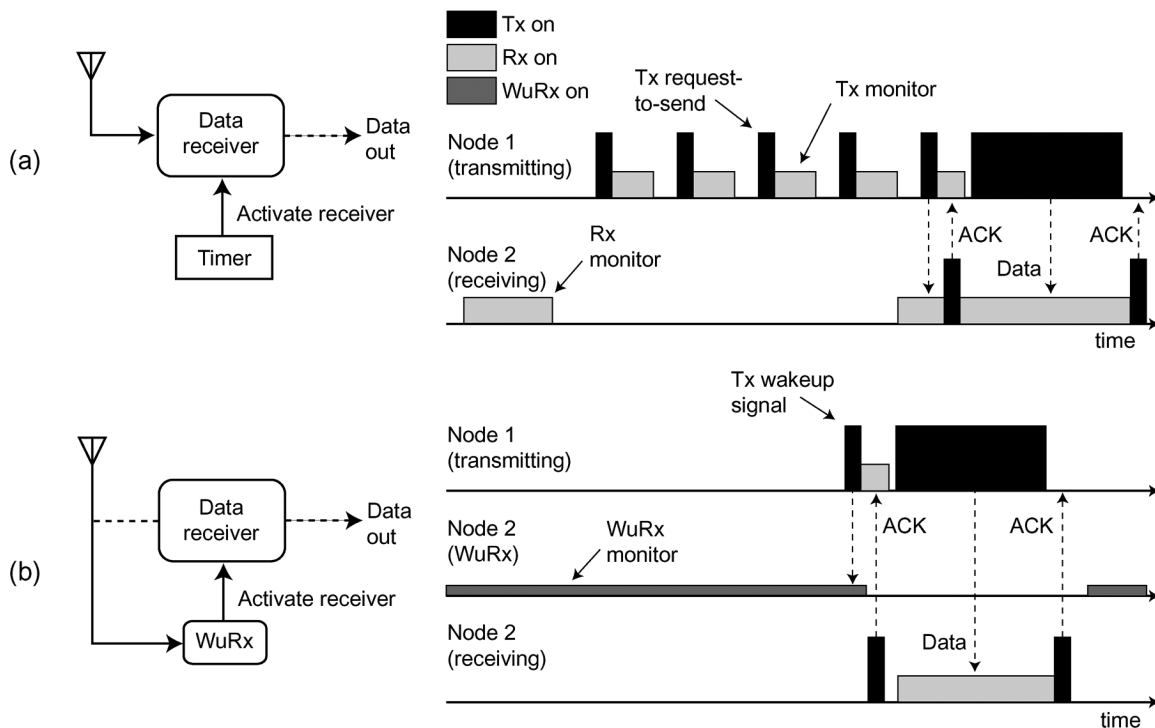


Fig. 1. Comparison of (a) protocol-based duty-cycling and (b) wake-up duty-cycling.

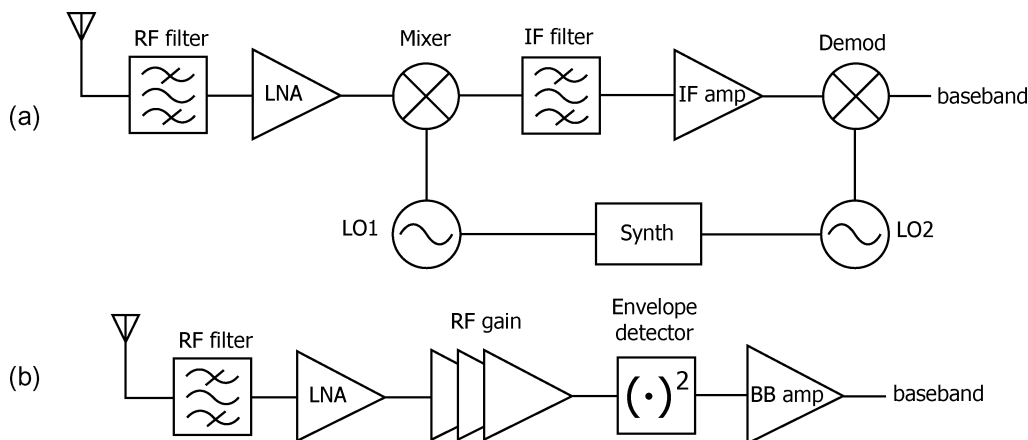


Fig. 2. Block-level comparison of receiver architectures: (a) frequency onversion and (b) RF envelope detection.

passives leads to a power floor of a few hundred microwatts. Zero-IF and low-IF receivers are special cases of the super-heterodyne architecture and are therefore subject to the same limitations. In fact, for one recent low-IF receiver implementation, the bulk of the power consumption is dedicated to the LO [4].

B. RF Envelope Detection

The simplest receiver architecture can be implemented with just RF amplification and an envelope detector, similar to the first AM receivers. This architecture, also called “tuned RF” (TRF), eliminates the power-hungry LO altogether (Fig. 2(b)). There are two main drawbacks with the TRF architecture. First, since the self-mixing operation is insensitive to phase and frequency, selectivity must be provided through narrowband filtering directly at RF. Second, high RF gain is required to overcome the sensitivity limitations of the envelope detector, usu-

ally implemented with a nonlinear element like a diode.¹ In [7], the TRF architecture is chosen to implement a wake-up receiver with very low power consumption. However, although the RF amplifier consumes most of the receiver’s total power, the available RF gain is limited and ultimately results in poor receiver sensitivity. In the next section, we analyze the relationship between gain and sensitivity in detail by considering a hypothetical envelope detection receiver.

C. TRF Receiver Sensitivity Analysis

A purely linear noise figure (NF) analysis cannot be used to determine the performance of a TRF receiver. The reason

¹In TRF receiver implementations, the gain stages preceding the detector have relaxed linearity specifications, because the detector nonlinearity dominates the total receiver distortion. This can be seen by considering the equation for distortion in a cascade of receiver stages [6].

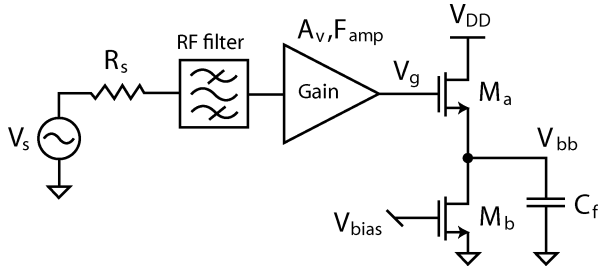


Fig. 3. Simplified TRF receiver schematic.

is that, due to the nonlinear nature of the envelope detection process, signal gain through the receive chain is reduced with decreasing input signal amplitude [8], [9]. In addition, typical envelope detector circuit implementations exhibit finite linear gain at low frequency, resulting in increased noise. Existing analyses of squaring-detector receivers in literature [10], [11] focus on calculating the probability distribution of the output noise after the squaring operation but ignore the extra noise added by the detector as well as its low frequency transmission. These analyses have proven useful in calculating the quantum limit of an optical receiver based on direct detection [11], but they resort to a rather sophisticated mathematical treatment and provide little design insight. Furthermore, in many cases the noise added by the detector through direct generation, as well as low-frequency transmission, dominates the total receiver budget. For this receiver, we adopt a simpler (although not as general), more design-oriented analysis to highlight the main trade-offs in TRF receiver design and prove that for moderate sensitivity designs, front-end noise figure should be traded for gain whenever possible. Essentially, the ultimate sensitivity is determined by analyzing the various noise contributions and gain factors to the detector output and calculating an effective NF that depends on the input signal power. The simplified receiver schematic for this analysis is shown in Fig. 3, consisting of a front-end amplifier with a specified voltage gain (A_v) and noise factor (F_{amp}) followed by an envelope detector (M_a, M_b).

The first step is to determine the nonlinear response of the detector. The detector shown in Fig. 3 is a standard topology [12] where the nonlinearity of M_a contributes a DC term at the output in response to an AC signal at V_g . Device M_a is biased in deep subthreshold where its drain current is an exponential function of gate-source voltage. The bandwidth of the detector is set by the pole $f_{p,det}$, determined by C_f and the output impedance of M_a

$$f_{p,det} = \frac{g_{m,a}}{2\pi C_f}. \quad (1)$$

The output capacitor C_f is chosen to be large enough to filter out any signal at the fundamental and higher harmonics. For small input AC voltages, it can be shown [9] that the effective conversion gain to baseband V_{bb} is given by

$$k = \frac{V_{bb}}{V_g} = \frac{V_g}{4nV_t} \quad (2)$$

where V_g is the amplitude of the AC input signal, n is the sub-threshold slope factor (about 1.5 in this CMOS technology),

and V_t is the thermal voltage (kT/q). Any input signals, including noise, at frequencies below the detector output bandwidth (BW_{det}) will experience the linear transfer function instead, with approximately unity gain ($k_{DC} \approx 1$). The total noise factor F_{tot} of the entire receiver can then be written as [8], [9]

$$F_{tot} = 2F_{amp} + \frac{N_{LF}k_{DC}^2}{N_{src}A_v^2k^2} + \frac{N_{o,ED}}{N_{src}A_v^2k^2} \quad (3)$$

where N_{src} represents the noise from the source resistance ($4kTR_s$), $N_{o,ED}$ is the output noise power of the envelope detector, and N_{LF} is the low frequency noise at the output of the front-end amplifier.² The gain of the front-end amplifier is given by A_v , while k is the envelope detector gain from (2). As anticipated, because of the dependence of k on signal level, the second and third terms on the right hand side of (3) have a V_{in}^{-2} dependence. Therefore, the total effective noise figure F_{tot} increases as input power decreases. Using F_{tot} , we can calculate an input-referred noise for the receiver in dBm

$$P_{n,in} = -174 + 10 \log(BW_{det}) + NF_{tot}. \quad (4)$$

If the minimum signal-to-noise ratio (SNR) for reliable detection is SNR_{min} , the minimum detectable signal ($P_{m ds}$) is the input power P_{in} for which

$$P_{m ds} = P_{n,in} + SNR_{min} \quad (5)$$

where the quantities in (4) and (5) are expressed in dB. This relationship can be visualized by plotting the noise power $P_{n,in}$ and $(P_{in} - SNR_{min})$ versus P_{in} and finding the intersection. In order to illustrate the calculation, consider the following example for the receiver shown in Fig. 3. The curves described by (4) and (5) are simulated first for a front-end amplifier with $A_v = 20$ dB and $NF = 10$ dB, and then repeated with 40 dB gain and 20 dB NF, using a typical value of 12 dB for SNR_{min} . For this example, only the amplifier gain and NF vary, while the rest of the receiver remains unchanged. The results are plotted in Fig. 4 for both sets of amplifier parameters. In both cases, the sensitivity limit is reached when the input voltage to the detector becomes so small that the receiver conversion gain drops towards zero. In this circumstance the noise generated both by the detector itself, as well as by subsequent stages, is increasingly magnified when referred to the input. For TRF receivers, it is this noise magnification, and not the RF front-end noise, that limits the achievable sensitivity as the input signal power falls. When the gain preceding the envelope detector is increased, the input power level corresponding to this drop in conversion gain is decreased, resulting in better sensitivity. For this reason, the receiver with higher gain has almost 20 dBm better sensitivity, despite 10 dB higher NF in the front-end.

The example illustrates the benefit of increasing gain in the front-end of an envelope detection receiver, even if the increase in gain results in poorer front-end noise performance. Unfortunately, adding high frequency gain requires too much power for the WuRx. Heterodyne architectures, on the other hand, are promising because they utilize frequency conversion to allow

²The expressions for $N_{o,ED}$ and N_{LF} are derived in [9]. In practice, simulations are used to verify hand analysis and account for other effects, like flicker noise.

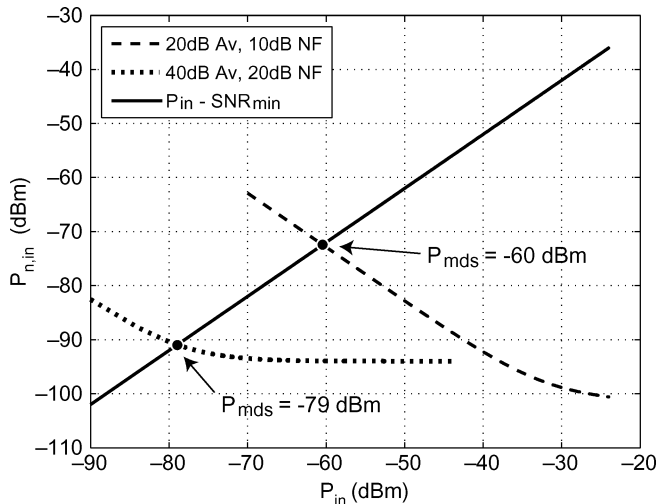


Fig. 4. Comparison of two TRF receiver examples operating with different front-end amplifier gain and noise characteristics.

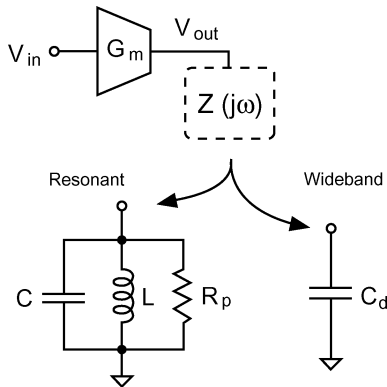


Fig. 5. Diagram of gain stage using resonant or wideband load network.

amplification at lower frequencies. If the power contribution of the LO can be reduced, frequency conversion offers a possible way to improve the performance of the envelope detection receiver.

III. WURX ARCHITECTURE CHOICE

A. Oscillator Power Limitations

In order to address the problem of oscillator power consumption, it is useful to review the fundamental power limitations for oscillation. The basic building block of any oscillator is a gain stage, simply modeled as a transconductance stage driving a load impedance (Fig. 5). In severely power-constrained designs, the bias current and device transconductance are limited to small fixed quantities. Therefore, in order to maximize gain, the load should be optimized for high impedance. For RF circuits, the load itself is usually implemented with a resonant LC network, where the impedance at the resonant frequency ω_0 is given by

$$R_p = \omega_0 L Q_L. \quad (6)$$

Equation (6) assumes that the network Q is limited by the inductor Q_L . For on-chip inductors in the low GHz regime, R_p is practically limited to a few kilohms by the size and quality of integrated passives. Microelectromechanical systems (MEMS) possess high Q factor and deliver low phase noise, but are nevertheless subject to similar limits in R_p [13] and therefore power consumption [14]. Unfortunately, technology scaling has little impact on the limitations of passive components, and R_p is unlikely to improve significantly in future technologies.

As an alternative to resonant networks, the load impedance can also be implemented as a wideband resistive load. In this case the bandwidth is determined by the load capacitance, which is normally the input device capacitance C_d of the subsequent stage. In contrast to resonant networks, scaled CMOS technologies excel at reducing device size and capacitance. The result is that, for fixed frequencies, the impedance magnitude attainable from a wideband network is increasing rapidly with technology scaling, far surpassing resonant networks in 90 nm CMOS. Fig. 6 illustrates this trend, comparing the impedance magnitude of an LC tank with that of transistor input capacitance at 2 GHz. For the LC tank, a very high quality inductor ($L = 20$ nH, $Q = 15$) is assumed to represent a best-case scenario, and as mentioned above, the impedance stays roughly constant as technology scales. In the wideband case, devices in each technology are sized and biased around moderate inversion to provide a transconductance equal to 1 mS, intended to model a realistic capacitive load C_d for a wideband amplifier. Clearly, the impedance magnitude due to device capacitance in modern technologies has greatly exceeded that of even a very high quality resonant tank. This observation leads us to expect a simple ring oscillator, which consists of wideband inverting gain stages, to achieve lower power oscillation than an LC oscillator.

To verify this expectation, the power consumption of a 3-stage CMOS ring oscillator is compared with a simple LC oscillator as technology scales (Fig. 7). The ring oscillator V_{DD} is reduced with technology to maintain the frequency constant at 2 GHz. For the LC oscillator, the power consumption required for startup diminishes slightly due to the reduced device threshold voltage in scaled technologies, enabling lower supply voltages with the same bias current. However, since the power of a CMOS ring oscillator scales with the total switched capacitance and the square of supply voltage, its power consumption drops much more rapidly. For modern 90 nm and 65 nm technologies, the 2 GHz ring oscillator yields a factor of 20 power savings over an LC oscillator. This finding is consistent with the analysis presented in [15], where the power efficiency of a resistively-loaded RF amplifier at 900 MHz was shown to be superior to a tuned amplifier in 0.18 μm CMOS.

B. Uncertain-IF Architecture

The preceding analysis addressed only the minimum power required to achieve oscillation at RF frequencies, without considering phase noise or frequency accuracy. Of course, these are important considerations for frequency conversion architectures, and the ring oscillator is known to have inferior frequency

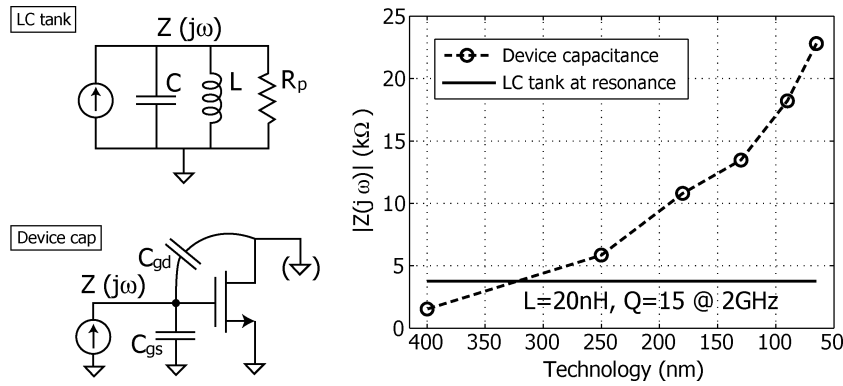


Fig. 6. Comparison of simulated impedance magnitude for resonant and nonresonant load networks as technology scales.

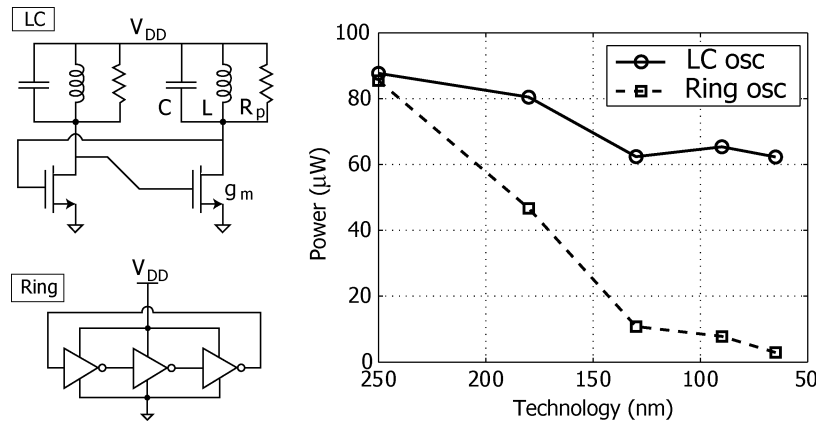


Fig. 7. Simulated power consumption of an LC oscillator and CMOS inverter-based ring oscillator as technology scales.

stability compared with an *LC* oscillator [16]. However, the receiver presented here overcomes these problems at the architecture level, by employing an “uncertain-IF” to relax the phase noise and frequency accuracy specifications, allowing the use of a free-running ring oscillator for LO generation.

The frequency plan and method of operation for the uncertain-IF architecture are shown in Fig. 8. The desired signal is first filtered at the front-end to remove image and interferers. It is then mixed with an LO whose frequency is not well-defined. In fact, the LO only needs to be guaranteed to lie within some pre-determined frequency band $\pm BW_{if}$ (± 100 MHz in this implementation) around the RF channel frequency. Due to the uncertainty of the LO frequency, the exact IF frequency will vary, but the downconverted signal will lie somewhere around DC within BW_{if} . The signal is then amplified at this IF frequency, which is much more power efficient than achieving the equivalent gain at RF. Finally, envelope detection performs the final downconversion to DC. Note that the use of envelope detection limits the receiver to detection of amplitude-modulated signals, most commonly on-off keying (OOK), because the envelope detector removes all phase and frequency content in the IF signal.

For an ultra-low power receiver like the WuRx, the uncertain-IF architecture holds several advantages over the architectures described in Section II. First, LO phase noise and frequency accuracy requirements are significantly relaxed. LO frequency variation simply appears as IF frequency variation, to

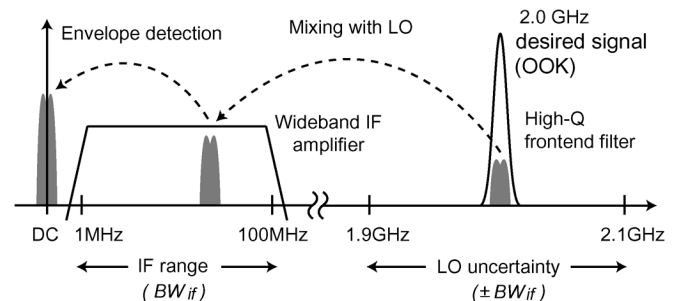


Fig. 8. Uncertain-IF receiver frequency plan and method of operation.

which the envelope detector is insensitive.³ An initial calibration step is required to account for process variation and tune the LO within the desired range. Thereafter, re-calibration is only required to counteract frequency drift due to temperature or supply variation. The LO is implemented with a digitally-controlled oscillator (DCO) to allow for convenient calibration and tuning without the need for a complete PLL. Furthermore, as in the heterodyne architecture, signal amplification can be performed at IF instead of RF. This is a benefit because non-resonant loads have even higher impedance than resonant loads at the lower IF frequency, yielding a substantial savings in power consumption. The result is essentially performance similar to a

³Any degradation in selectivity due to reciprocal mixing is negligible compared with the nonlinearity introduced by the envelope detector.

TRF receiver with large effective gain before envelope detection, improving performance compared to receivers using only RF gain.

A variety of well-known techniques can be used to calibrate the DCO, which is similar to a coarse tuning algorithm in standard digital PLLs [17]. Re-calibration of the LO frequency is only required to adjust for process variations and changes in temperature and voltage that occur over time. Additional care should be taken to ensure that the frequencies of the DCO and the incoming signal never overlap. The input signal would then be directly converted to DC, bypassing the nonlinear function of the envelope detector and corrupting the baseband output. This condition, where the natural frequency of the DCO happens to precisely align with that of the RF matching network, never occurred with any of the prototypes tested. However, the probability of this event occurring is on the order of a few percent and therefore not small enough to neglect entirely. As long as the IF bandwidth is kept about 10% larger than the frequency calibration step size, there will always be at least two tuning words such that the downconverted signal lies within the IF band. Therefore, the receiver could periodically alternate between neighboring tuning codes to guarantee faithful reception with high probability.

At the architecture level, an additional design consideration is the trade-off between LO tuning accuracy and IF bandwidth. If the LO can be tuned very close to the channel frequency, the required bandwidth of the IF amplifier can be narrowed and its power reduced proportionately. On the other hand, the LO must now be kept within a smaller frequency range, increasing vulnerability to oscillator frequency drift. If the IF bandwidth is made large enough, the receiver will be relatively immune to frequency drift and the LO will be able to run for long periods without calibration. For the first prototype using this architecture, a conservative value of 100 MHz is selected for the IF bandwidth. The relatively wide bandwidth is chosen to maximize tolerance of LO jitter and frequency drift, without requiring excessive power in the IF amplifier.

Like any TRF receiver, however, a disadvantage of the uncertain-IF architecture is its susceptibility to interferers. Any undesired signal within $\pm BW_{if}$ of the LO frequency that passes through the front-end filter will be mixed down and detected by the envelope detector. Therefore, a narrow and accurate RF bandpass filter is required to improve robustness to interferers. In effect, the burden of selectivity has been shifted from the LO to the front-end filter. In this design, filtering is performed by a bulk acoustic wave (BAW) resonator, a piezoelectric structure fabricated using standard thin-film IC processing techniques with Q factors between 500 and several thousand at low GHz frequencies [18]. The combination of small size, low-cost manufacturing, and high Q lead to compact circuit implementations. Accordingly, the use of BAW resonators for low power RF circuits has been popularized recently, using the resonator both in high quality oscillators and as a filtering element [3], [13], [19].

IV. CIRCUIT DESIGN

A block diagram of the complete receiver is shown in Fig. 9. The OOK input signal is first filtered by the matching network

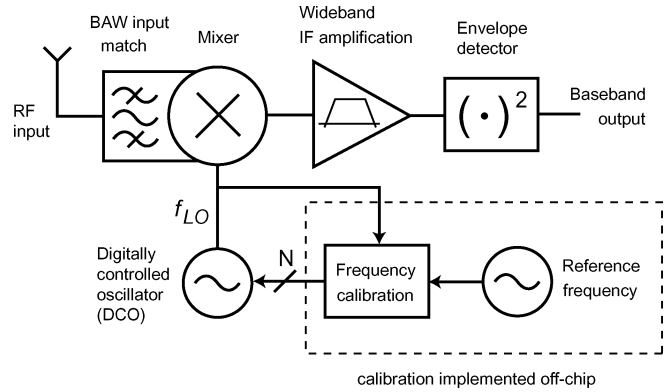


Fig. 9. Block diagram of proposed wake-up receiver using an uncertain-IF architecture.

containing the BAW resonator, followed directly by the mixer. The resulting IF signal is amplified with a gain block covering the entire IF range and finally converted to DC by the envelope detector. On the LO side, a free-running digitally-controlled oscillator (DCO) drives the mixer. Digital frequency control is used to calibrate the LO within the desired frequency range only when necessary, instead of maintaining an analog control voltage during normal operation. This section describes the design of each component in detail. In implementing each receiver block, the primary goal of reducing power consumption motivates simplicity in the circuit design. To further reduce power, the entire receiver is optimized to operate from a single 0.5 V supply.

A. Input Matching Network

The matching network serves two purposes. First, it must supply a stable impedance match to the 50 Ω input source. In addition, the network should provide the narrow RF filter required by the architecture. To satisfy both of these requirements, the matching network embeds a BAW resonator with an on-chip capacitive transformer (Fig. 10). Since the BAW impedance is high in the parallel resonance mode, metal-insulator-metal (MIM) capacitors C_1 and C_2 transform the low antenna impedance up to match the resonator impedance. The mixer input capacitance can then be absorbed with the resonator capacitance, eliminating the need for a real input impedance at the mixer input. The mixer input transistor is sensitive to voltage, so an additional benefit of the impedance transformation is approximately 12 dB of passive voltage gain [4].

B. Dual-Gate Mixer

The mixer design is driven by two goals: maximizing conversion gain and minimizing LO drive requirements. A single-ended dual-gate topology is chosen because the LO port is conveniently driven from a single-ended ring oscillator. A differential ring oscillator would require at least twice the power of the single-ended implementation. RF and LO feedthrough inherent to the single-balanced design are filtered by the load network and the IF amplifier stages before arriving at the envelope detector (Fig. 10). Devices M_1 and M_2 are sized $(10/0.1) \mu\text{m}/\mu\text{m}$, with M_2 presenting only about 10 fF of capacitive load to the LO. Although the cascode device M_2 generally modulates the

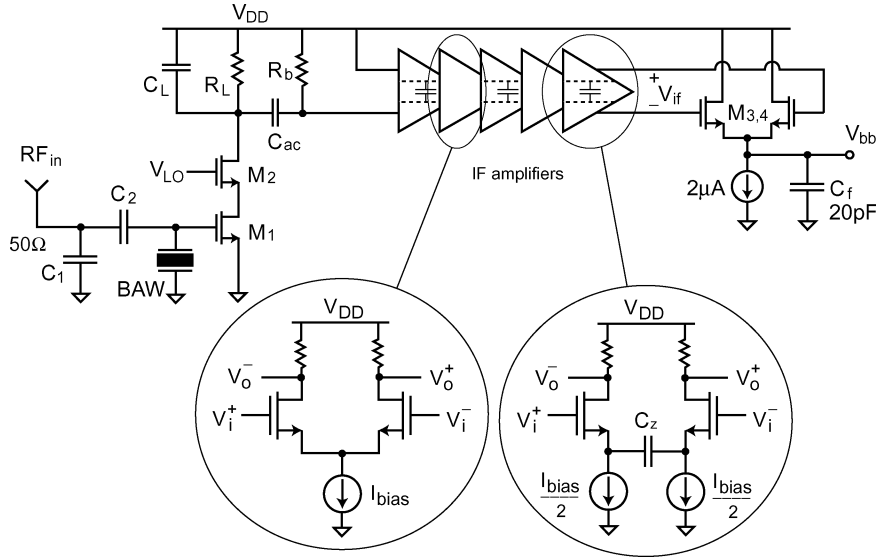


Fig. 10. Schematic of frequency conversion front-end and envelope detection circuit.

transconductance of M_1 , the CMOS buffers drive the LO port with a rail-to-rail signal, effectively switching the RF transconductor M_1 on and off. Therefore, the voltage conversion gain G_{conv} can be calculated using the Fourier series representation of the time-varying transconductance switching between g_{m0} and zero [9]:

$$G_{conv} = \frac{1}{\pi} g_{m0} (R_L || R_b || R_{o,mix}) \quad (7)$$

where $R_{o,mix}$ is the output resistance looking into the drain of M_2 when the LO voltage is at V_{DD} . The mixer load resistor R_L is made as large as possible to maximize the conversion gain within the available voltage headroom. Including the voltage gain in the matching network and using (7), the calculated voltage conversion gain of the mixer is 13.9 dB, which closely matches the simulated value of 14.5 dB.

C. IF Amplifier

As specified in the architecture design, the IF amplifier must provide gain across the bandwidth of 100 MHz. In scaled CMOS technology, this frequency performance is easily met using a wideband differential pair with resistive loads. In order to operate under the low supply voltage a multi-stage architecture is chosen, using five differential pair gain stages optimized for maximum gain-bandwidth product for a given power consumption (about 8 dB/stage). The input pair devices are sized $(6/0.2) \mu\text{m}/\mu\text{m}$ and biased in the subthreshold regime for high transconductance efficiency (g_m/I_d). The gain stages together produce more than 40 dB of total gain, with each stage consuming 8 μA of current. The use of resistive loads simplifies biasing and allows DC coupling between stages (Fig. 10). In the first, third, and fifth stages, the tail current source is split into two halves with a coupling capacitor C_z [20], introducing a zero at DC in the differential transfer function. Combined with AC coupling between the mixer and the first IF stage, this technique rolls off the IF gain close to DC, where the IF signal would be too close to the baseband bandwidth. The lack of gain at DC also prevents large accumulated offsets through the IF

amplifier chain [15]. The simulated voltage conversion gain of the combined mixer/IF amplifier front-end is about 50 dB to the IF output, with a corresponding NF of 23 dB.

D. Envelope Detector

The envelope detection circuit is implemented with a differential pair [15] biased with 2 μA of current (weak inversion) for maximum nonlinearity (Fig. 10). When a differential IF signal drives the gates of M_3 and M_4 , the nonlinear bias point shift appears at the drain of the tail current source, converting the IF energy to a DC baseband signal. A 20 pF capacitor at the output filters out any feedthrough from the IF signal or higher harmonics, with a baseband bandwidth of about 600 kHz.

E. Digitally-Controlled Oscillator

The DCO is implemented with the simplest type of ring oscillator, a 3-stage CMOS ring using standard library inverters. Frequency tuning is accomplished through the use of two resistive DACs that modify the virtual supply rails (V_H , V_L) of the ring (Fig. 11). Two DACs are used in order to keep the voltage swing near the middle of the range, so that the output levels can be restored to full swing using an inverter chain operating with the full V_{DD} . The scaled inverter chain serves as a non-resonant buffer to drive the mixer LO port. The 5-bit resistive tuning DACs are designed using Monte Carlo simulations to guarantee that the LO frequency can always be tuned within the desired range across process and temperature. Low threshold devices are used to ensure sufficient speed with the 0.5 V supply.

F. Uncertain-IF Sensitivity Analysis

With the receiver design parameters established as described above, the overall sensitivity can now be predicted. The simple example in Section II-C included only front-end NF and low frequency noise, plus envelope detector noise. For the uncertain-IF receiver, there is an additional noise source that must be taken into account, due to the wide IF bandwidth. Since the high- Q filter is at the input of the receiver, the noise of the

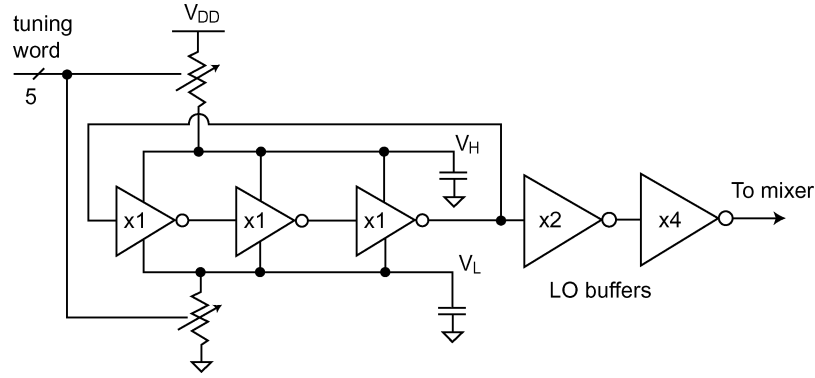


Fig. 11. Digitally-controlled oscillator schematic.

front-end entering the detector is integrated across the entire IF bandwidth of 100 MHz. This noise passes through the non-linear transfer function of the detector with the desired signal. The noise density at the detector output can be calculated as [8]

$$N_{o,IF} = \frac{2(\sigma^2)^2}{(4nV_t)^2} \frac{1}{BW_{IF}} \quad (8)$$

where σ^2 is the integrated noise power at the IF output and determined by periodic steady-state simulation. The output noise is added as an additional factor in (3) to arrive at the complete noise factor

$$F_{tot} = 2F_{linear} + \frac{N_{LF}k_{DC}^2}{N_{src}G_{conv}^2k^2} + \frac{N_{o,ED}}{N_{src}G_{conv}^2k^2} + \frac{N_{o,IF}}{N_{src}G_{conv}^2k^2} \quad (9)$$

where F_{linear} and G_{conv} are the linear noise figure and voltage conversion gain of the mixer/IF amplifier combined front-end. The relative contributions to the noise factor for each term in (9) are shown in Fig. 12, using simulations to establish final values for the noise and gain variables. Combining (9) with (4) and (5) as described in Section II-C, the predicted sensitivity is -71 dBm for 12 dB baseband SNR. The integrated IF noise ($N_{o,IF}$) dominates at the sensitivity limit due to the wide IF bandwidth, revealing a further drawback of the wideband IF. Reducing the IF bandwidth will proportionately reduce this noise component and enhance sensitivity. Of course, this improvement will result in less tolerance of LO drift and require increased tuning accuracy.

V. MEASUREMENT RESULTS

The prototype receiver is fabricated in 90 nm standard CMOS technology with MIM capacitors (Fig. 13). The active area is approximately 0.1 mm^2 , with no external components required except a single BAW resonator. For prototyping purposes, the packaged resonator is simply connected to the CMOS die using wirebonds.

A standalone test LO block is included on the prototype chip for characterization purposes. For receiver functionality, the chief metrics of interest for the LO are process compliance, temperature compliance, and transient stability. The first two factors are addressed through frequency calibration, while the

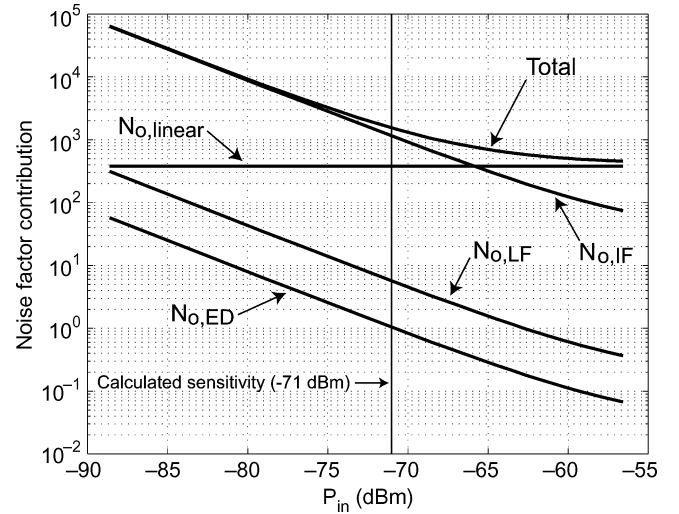


Fig. 12. Calculated noise figure contributions for the uncertain-IF receiver versus input power level.

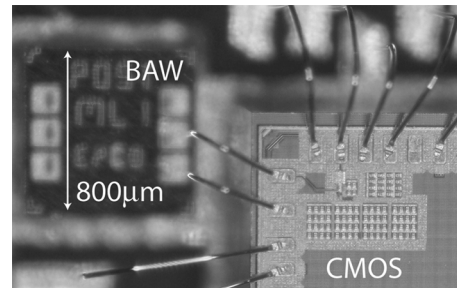


Fig. 13. Die photo of CMOS prototype. The packaged BAW resonator can be seen on the left, directly bonded to the CMOS chip.

latter determines how often calibration is required. To compensate for process variation, the measured tuning range of the LO is from approximately 1 to 3 GHz, with the tuning curves for 5 different samples plotted in Fig. 14(a). Three samples were also measured across a temperature range from 0 to 90°C , using an off-chip state machine to control the oscillator tuning. The results are shown in Fig. 14(b). The frequency of the oscillator is allowed to drift with temperature until it leaves the preset limits, which triggers an automatic calibration cycle to re-center the LO. For all three samples, the frequency remains well within the desired region around 2 GHz across the

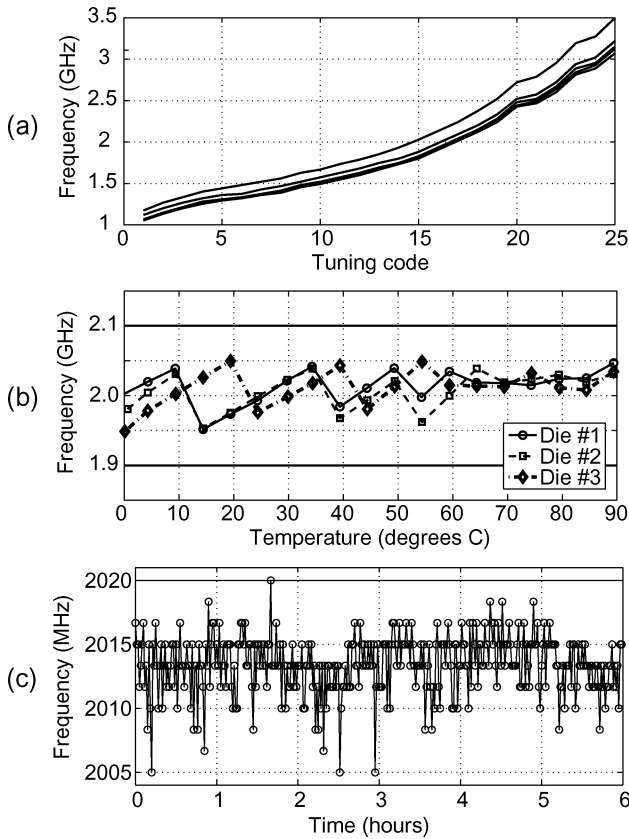


Fig. 14. DCO test block measurements: (a) tuning characteristic, (b) temperature drift calibration, and (c) free-running frequency over 6 hours (unregulated temperature environment).

entire temperature range. To quantify long-term stability, the test oscillator frequency was also measured open-loop over a 6 hour period at 1 minute intervals in an unregulated temperature (office) environment, without changing the frequency control word. Fig. 14(c) shows that the frequency ranges from 2005 MHz to 2020 MHz, verifying that LO calibration would not have been required during the entire 6 hour period. This robustness is a direct advantage of the wide 100 MHz IF bandwidth chosen for this implementation, illustrating that the receiver is able to remain functional despite long-term drift and variations in process and temperature.

The receiver's overall RF-to-baseband gain response versus frequency is plotted in Fig. 15 for four different samples. The response of the BAW resonator is evident in the plot, with the peak gain occurring at the parallel resonance of the BAW. For each sample, the LO was calibrated before measurement and the resulting frequencies are also marked on the plot, showing the natural variation in LO frequency for different samples. Although not visible in Fig. 15 due to the insufficient frequency resolution of the measurement, the response of each receiver has a narrow notch at the LO frequency. As discussed in Section III-B, this is because signals at the LO frequency are downconverted to directly DC, where the IF amplifier has a zero.

The receiver sensitivity is measured by modulating the input RF carrier with an OOK pseudorandom bit sequence and buffering the baseband analog output signal off-chip. There, the raw waveform is directly sliced by a comparator to generate

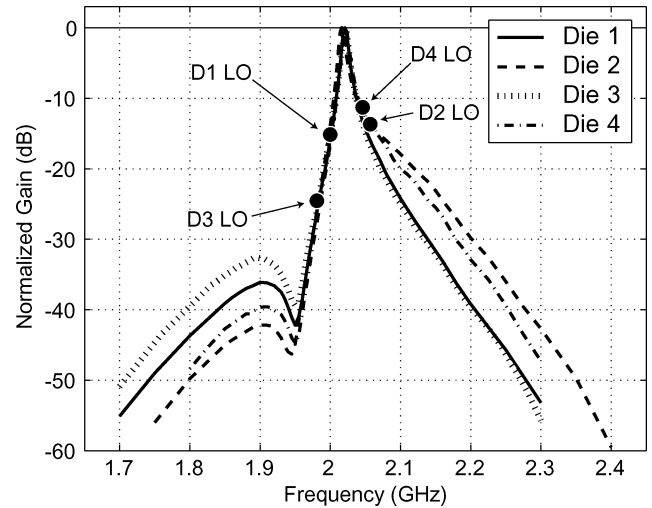


Fig. 15. Measured gain response of receiver from RF input to baseband output (normalized) for four different samples. The natural LO frequency after calibration is marked on the gain curve for each sample.

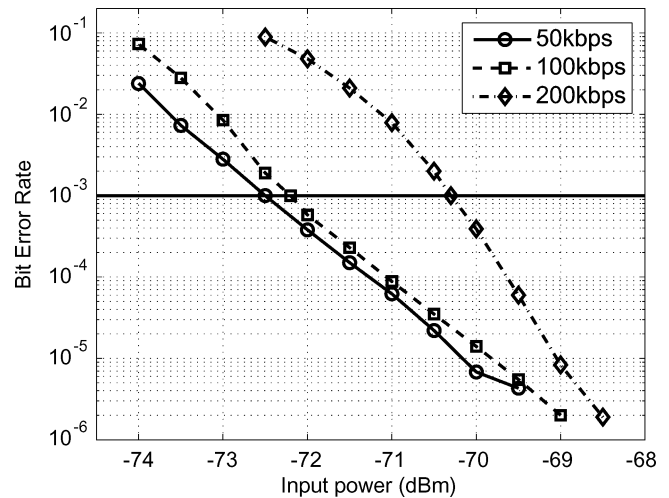


Fig. 16. Measured BER characteristic of the receiver for different data-rates.

digital bits for the bit error rate (BER) tester. For a BER of 10^{-3} and a data-rate of 100 kbps, the sensitivity is about -72 dBm (Fig. 16). For higher data-rates, the bandwidth of the envelope detector begins to limit the response, degrading sensitivity by about 2 dBm at 200 kbps. The measured sensitivity exhibits about 1 dB variation among the four different samples.

One additional area of concern with this architecture is possible LO re-radiation from the antenna, because the mixer is the first element in the receiver chain without an LNA for isolation. In practice this is not a problem, because the LO frequency is offset from the channel frequency and filtered by the BAW resonator and matching network. Re-radiation at the antenna port was measured at -81 dBm with the LO located 20 MHz above the channel frequency, falling to less than -90 dBm when the LO is offset by 70 MHz.

Receiver performance in the presence of interfering signals is a concern for the WuRx, because false alarms will needlessly activate the main receiver. The interferer performance is quantified using the following measurement setup. The desired

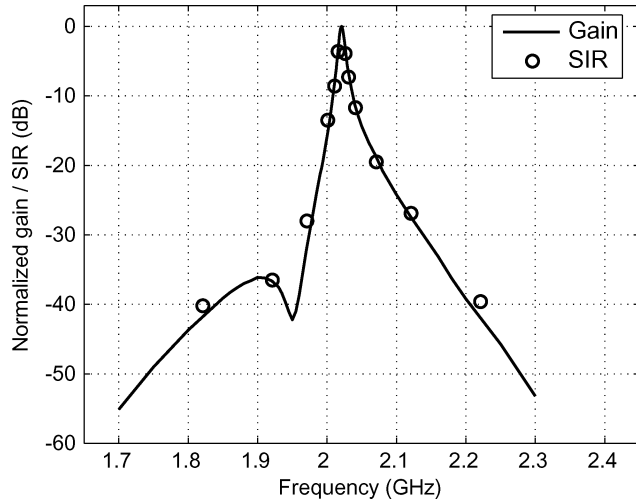


Fig. 17. Measured signal-to-interferer ratio (SIR) that can be tolerated without BER degradation for different interferer frequencies. The RF-to-baseband gain response is overlaid for comparison.

signal is injected with a power level +3 dB above the sensitivity limit, combined with a continuous wave interferer at a given frequency offset from the desired channel. The interferer power level is increased until the BER rises above 10^{-3} , yielding a signal-to-interferer ratio (SIR) at that frequency offset, which represents the maximum interferer power level that can be tolerated without blocking the receiver. The results of the measurement are plotted in Fig. 17, overlaid with the normalized gain response. Clearly, the SIR points correspond closely to the gain response, indicating that the interferer performance is dominated by the front-end filter. This is a characteristic common to all receivers based on envelope detection, because any residual undesired signal after the filter is detected with the desired signal. For example, in a two-tone blocker scenario, the blocking signals themselves will pass through the filter with finite attenuation before they experience any nonlinear effects, so the distortion products of the interferers will be negligible compared with the blockers themselves. This result is the key observation that enables the use of very low power front-end circuitry and a low supply voltage, despite poor linearity performance. Although the single resonator used in this implementation can only provide about 20 dB of out-of-band attenuation, a better filter implementation using higher Q resonators or a filter structure with multiple resonators could provide better robustness to interfering signals.

The total power consumption of the receiver is $52 \mu\text{W}$ from the 0.5 V supply. The LO generation and IF amplifiers draw about 80% of the total, with $20 \mu\text{W}$ and $22 \mu\text{W}$, respectively. The mixer consumes $8 \mu\text{W}$, while the envelope detector accounts for the remaining $2 \mu\text{W}$. The measured power of the ring oscillator alone is $6 \mu\text{W}$ at 2 GHz. Although this figure increases to $20 \mu\text{W}$ when the LO buffers are included, this total still represents an order-of-magnitude reduction compared with the integrated LC oscillator in [4] and more than a factor of 4 improvement over the BAW-based oscillator in [14]. The complete WuRx performance is summarized in Table I.

TABLE I
PERFORMANCE SUMMARY OF THE PROTOTYPE WuRx

Parameter	Value
Global supply voltage (V)	0.5
Carrier frequency/modulation	2 GHz / OOK
Power dissipation (μW)	
Mixer	8
IF amplifiers	22
LO + buffers	20
Envelope detector	2
Total	52
Data rate (kbps)	100/200 (nom/max)
Energy per received bit (nJ)	< 0.5
Raw sensitivity for 10^{-3} BER (dBm)	-72/-70 (100/200kbps)

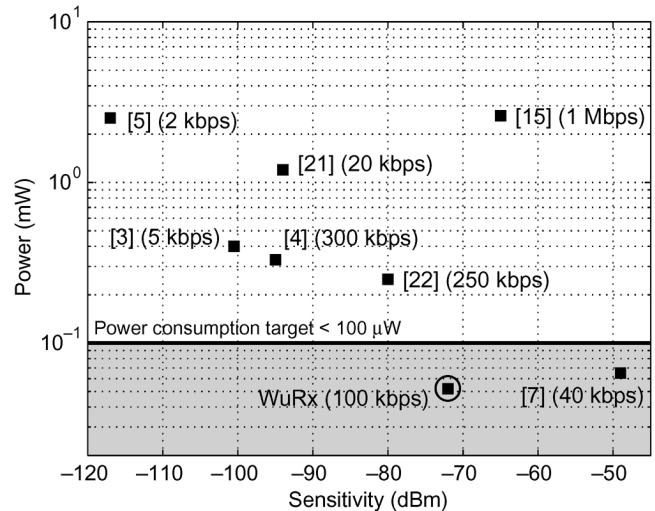


Fig. 18. Comparison of power consumption and sensitivity for the proposed receiver with previously published low power receivers for sensor networks.

VI. CONCLUSION

This paper presents a complete receiver implementation using an uncertain-IF architecture, designed specifically for the ultra-low power wake-up application. The significant power reduction is made possible through the combination of a CMOS ring LO and RF-MEMS resonator technology, breaking the power floor that arises using traditional high performance oscillators. The performance of the proposed receiver is compared with previously published low power receivers for sensor networks in Fig. 18. To the authors' knowledge, this is the first published RF wake-up receiver implementation with sensitivity better than -50 dBm. However, because the proposed receiver is not as sensitive as the higher powered data receivers shown in Fig. 18, it is most applicable when used together with a main receiver having similar sensitivity. Alternatively, the wake-up

signal could be transmitted with a higher power level than normal data to compensate for the lower sensitivity of the WuRx. In any case, the substantial improvement in sensitivity (more than 23 dB) over other published wake-up receivers [7], [23] results in a much smaller difference in sensitivity compared to other data receivers designed for sensor networks.

It is important to emphasize that while frequency calibration is still required, the uncertain-IF architecture also guarantees a high tolerance to reference frequency inaccuracy. For example, the 100 MHz IF bandwidth chosen for this implementation corresponds to approximately 5% of the 2 GHz carrier frequency. A frequency reference that guarantees 2.5% accuracy over process and temperature variations is sufficient. This requirement is over 100 times less stringent than the performance of typical communication-grade quartz crystals, and can be obtained with a fully integrated LC or CMOS oscillator [24], [25], potentially reducing cost and increasing integration when compared to more conventional solutions.

ACKNOWLEDGMENT

The authors thank STMicroelectronics and Avago Technologies for donations of CMOS fabrication and BAW resonators, respectively. The authors would also like to thank Dr. Brian Otis for measurement assistance.

REFERENCES

- [1] J. Rabaey, J. Ammer, T. Karalar, S. Li, B. Otis, M. Sheets, and T. Tuan, "PicoRadios for wireless sensor networks: The next challenge in ultra-low power design," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2001, pp. 200–201.
- [2] E.-Y. Lin, J. Rabaey, and A. Wolisz, "Power-efficient rendezvous schemes for dense wireless sensor networks," in *Proc. IEEE Int. Conf. Communications*, Jun. 2004, vol. 7, pp. 3769–3776.
- [3] B. Otis, Y. H. Chee, and J. Rabaey, "A 400 μ W RX, 1.6 mW TX, super-regenerative transceiver for wireless sensor networks," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2005, pp. 396–606.
- [4] B. Cook, A. Berny, S. Lanzisera, A. Molnar, and K. Pister, "Low-power 2.4-GHz transceiver with passive RX front-end and 400-mV supply," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2757–2766, Dec. 2006.
- [5] V. Peiris, C. Arm, S. Borjes, S. Cserveny, F. Giroud, P. Graber, S. Gyger, E. Le Roux, T. Melly, M. Moser, O. Nys, F. Pengg, P.-D. Pfister, N. Raemy, A. Ribordy, P.-F. Ruedi, D. Ruffieux, L. Sumanen, S. Todeschini, and P. Volet, "A 1 V 433/868 MHz 25 kb/s-FSK 2 kb/s-OOK RF transceiver SoC in standard digital 0.18 μ m CMOS," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2005, pp. 258–259.
- [6] B. Razavi, *RF Microelectronics*. Upper Saddle River, NJ: Prentice Hall, 1998.
- [7] N. Pletcher, S. Gambini, and J. Rabaey, "A 65 μ W, 1.9 GHz RF to digital baseband wakeup receiver for wireless sensor nodes," in *Proc. IEEE Custom Integrated Circuits Conf.*, Sep. 2007, pp. 539–542.
- [8] S. Gambini, N. Pletcher, and J. Rabaey, "Sensitivity analysis for AM detectors," EECs Dept, Univ. of California, Berkeley, Tech. Rep. UCB/EECS-2008-31, Apr. 2008 [Online]. Available: <http://www.eecs.berkeley.edu/Pubs/TechRpts/2008/EECS-2008-31.html>
- [9] N. Pletcher, "Ultra-low power wake-up receivers for wireless sensor networks," EECs Dept, Univ. of California, Berkeley, Tech. Rep. UCB/EECS-2008-59, May 2008 [Online]. Available: <http://www.eecs.berkeley.edu/Pubs/TechRpts/2008/EECS-2008-59.html>
- [10] M. Kac and A. J. F. Siegert, "On the theory of noise in radio receivers with square law detectors," *J. Appl. Phys.*, vol. 8, no. 383, 1947, doi 10.1063/1.1697662.
- [11] I. T. Monroy, "On analytical expressions for the distribution of the filtered output of square envelope receivers with signal and colored Gaussian noise input," *IEEE Trans. Commun.*, vol. 49, no. 1, pp. 19–23, Jan. 2001.
- [12] R. Meyer, "Low-power Monolithic RF peak detector analysis," *IEEE J. Solid-State Circuits*, vol. 30, no. 1, pp. 65–67, Jan. 1995.
- [13] S. Rai and B. Otis, "A 600 μ W BAW-tuned quadrature VCO using source degenerated coupling," *IEEE J. Solid-State Circuits*, vol. 43, no. 1, pp. 300–305, Jan. 2008.
- [14] Y. H. Chee, A. Niknejad, and J. Rabaey, "A sub-100 μ W 1.9-GHz CMOS oscillator using FBAR resonator," in *IEEE Radio Frequency Integrated Circuits (RFIC) Symp. Dig. Papers*, Jun. 2005, pp. 123–126.
- [15] D. Daly and A. Chandrakasan, "An energy-efficient OOK transceiver for wireless sensor networks," *IEEE J. Solid-State Circuits*, vol. 42, no. 5, pp. 1003–1011, May 2007.
- [16] A. Hajimiri, S. Limotyrakis, and T. Lee, "Jitter and phase noise in ring oscillators," *IEEE J. Solid-State Circuits*, vol. 34, no. 6, pp. 790–804, Jun. 1999.
- [17] T.-H. Lin and Y.-J. Lai, "An agile VCO frequency calibration technique for a 10-GHz CMOS PLL," *IEEE J. Solid-State Circuits*, vol. 42, no. 2, pp. 340–349, Feb. 2007.
- [18] R. Ruby, P. Bradley, J. Larson, Y. Oshmyansky, and D. Figueredo, "Ultra-miniature high-Q filters and duplexers using FBAR technology," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2001, pp. 120–121.
- [19] J. Chabloz, C. Müller, F. Pengg, A. Pezous, C. Enz, and M.-A. Dubois, "A low-power 2.4 GHz CMOS receiver front-end using BAW resonators," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2006, pp. 1244–1253.
- [20] T. Toifl, C. Menolfi, M. Ruegg, R. Reutemann, P. Buchmann, M. Kossel, T. Morf, J. Weiss, and M. Schmatz, "A 22-Gb/s PAM-4 receiver in 90-nm CMOS SOI technology," *IEEE J. Solid-State Circuits*, vol. 41, no. 4, pp. 954–965, Apr. 2006.
- [21] A. Molnar, B. Lu, S. Lanzisera, B. Cook, and K. Pister, "An ultra-low power 900 MHz RF transceiver for wireless sensor networks," in *Proc. IEEE Custom Integrated Circuits Conf.*, Sep. 2004, pp. 401–404.
- [22] D. Guermendi, S. Gambini, and J. Rabaey, "A 1 V 250 kpps 90 nm CMOS pulse based transceiver for cm-range wireless communication," in *Proc. IEEE ESSCIRC*, Sep. 2007, pp. 135–138.
- [23] S. von der Mark and G. Boeck, "Ultra low power wakeup detector for sensor networks," in *SBMO/IEEE MTT-S Int. Microwave & Optoelectronics Conf. (IMOC 2007) Dig.*, 2007, pp. 865–868.
- [24] M. McCorquodale, S. Pernia, J. O'Day, G. Carichner, E. Marsman, N. Nguyen, S. Kubba, S. Nguyen, J. Kuhn, and R. Brown, "A 0.5-to-480 MHz self-referenced CMOS clock generator with 90ppm total frequency error and spread-spectrum capability," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2008, pp. 350–351.
- [25] K. Sundaresan, P. Allen, and F. Ayazi, "Process and temperature compensation in a 7-MHz CMOS clock oscillator," *IEEE J. Solid-State Circuits*, vol. 41, no. 2, pp. 433–442, Feb. 2006.



Nathan M. Pletcher (S'01–M'08) received the B.S. degree in electrical engineering from Case Western Reserve University in 2002, and the M.S. and Ph.D. degrees from the University of California, Berkeley in 2004 and 2008, respectively.

He is currently with Qualcomm, San Diego, CA, where he is involved in the design of RFICs for wireless communication systems. His interests include the design of highly integrated, low power wireless circuits and circuit co-design with RF-MEMS. He is the co-author of several book chapters on ultra-low power design for wireless sensor networks and ambient intelligence.



Simone Gambini (S'04) was born in Piombino Italy, in 1980. He received the Dr.Ing. degree (*summa cum laude*) from the University of Pisa in 2004 and the M.S. degree from the University of California at Berkeley in 2006, where he is currently working towards the Ph.D. degree. In 2004, he also received the Diploma di Licenza from Scuola Superiore Sant'Anna, Pisa.

He has held visiting positions at Philips Research, Eindhoven, and Intel Communication Circuit Laboratory, Hillsboro, OR. His research interests are in the fields of low-power ultra-short range wireless communications, data conversion systems, and sensor interfaces.



Jan Rabaey (F'95) received the M.S.E.E. and Ph.D degrees in applied sciences from the Katholieke Universiteit Leuven, Leuven, Belgium.

From 1983 to 1985, he was a Visiting Research Engineer with the University of California, Berkeley (UC Berkeley). From 1985 to 1987, he was a Research Manager with IMEC, Belgium, and in 1987 he joined the faculty of the Electrical Engineering and Computer Sciences Department, UC Berkeley, where he now holds the Donald O. Pederson Distinguished Professorship. From 1999 until 2002, he was the As-

sociate Chair of the Electrical Engineering and Computer Sciences Department, UC Berkeley. He is currently the Scientific Co-director of the Berkeley Wireless Research Center as well as the Director of the MARCO GigaScale Systems Research Center. His current research interests include the conception and implementation of next-generation integrated wireless systems. He serves on the technical advisory board of a range of companies and research institutes focused in the areas of design automation, semiconductor intellectual property and wireless systems.