# Circuit-Level Requirements for MOSFET-Replacement Devices

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## Introduction

Power consumption has grown to be the dominant challenge for continued CMOS scaling. This issue can be traced directly to the fact that the thermal voltage $k_BT/q$ does not scale, limiting the extent to which the MOSFET threshold voltage ($V_T$) and hence the supply voltage ($V_{dd}$) can be scaled. To circumvent this limit, alternative switching device designs [1,2] which can achieve <60 mV/dec sub-threshold swing ($S$) have been proposed and demonstrated. However, many of these fail to maintain improved $I_{on}/I_{off}$ across a range of $V_{dd}$. In this paper, we apply circuit-level metrics to establish guidelines for assessing the promise of alternative switching devices for replacing the MOSFET.

## Simplified Energy-Performance Analysis

Dynamic energy can be reduced quadratically by decreasing $V_{dd}$, but to avoid increased circuit delay, $V_T$ must be decreased together with $V_{dd}$ to maintain a high on-state drive current ($I_{on}$). This results in increased off-state leakage current ($I_{off}$) and hence increased static energy. To minimize total energy, the dynamic and static energies must be properly balanced; for CMOS circuits the optimal ratio of dynamic energy to leakage energy is roughly ~30-50% for most designs. With this ratio fixed, the optimal $I_{on}/I_{off}$ ratio is proportional to the logic depth divided by the activity factor of the circuit. The value of $V_{dd}/I_{on}$ sets the performance of the system, so if a device with smaller $S$ can achieve a given $V_{dd}/I_{on}$ and $I_{on}/I_{off}$ at lower voltage, it will achieve lower total energy at the same performance.

In setting device and circuit design parameters to optimally balance leakage and dynamic energies, it is critical to consider the impact of variations. For example, since $I_{off}$ varies exponentially with $V_T$ for a MOSFET, the average $I_{off}$ is much higher than $I_{off}(V_{Taverage})$; thus, maintaining the appropriate energy ratio requires a lower nominal $I_{off}$. In contrast to energy, the performance of a synchronous digital circuit is set by the critical paths. While there is some summing of delay variations along the path, the paths are not very long, so variations remain. Thus $I_{on}$ must be increased to ensure all paths meet the performance target for the worst-case variations. The device layout area impacts capacitance (*e.g.* of interconnect wires) and thereby circuit performance, and thus is an important factor.

Applications with low performance demands or large amounts of parallelism can tolerate reduced device performance, so that $V_{dd}$ can be scaled more aggressively (with margin for variation) to reduce energy. It can be shown that for these applications, $V_{dd}/I_{on}$ is not as critical as the minimum supply voltage $V_{dd,min}$, which depends only on maintaining the optimal $I_{on}/I_{off}$ ratio and is proportional to $S$.

Before moving on, it should be noted that even if a device has low $S$ but requires a non-zero output voltage ($V_{ds}$) to conduct, it may not improve the overall energy efficiency. This is because digital gates built which such a device would either dissipate significant static power, or would be significantly constrained in terms of the number of devices that can be connected in series.

## Comparisons with CMOS: TFET and Relay Technologies

Promising sub-60mV/dec MOSFET-replacement devices generally fall into one of two categories: devices that behave very similarly to a MOSFET but which have smaller $S$, and mechanical switches based on making or breaking physical contact. To show the implications of the energy-performance analysis, we will compare two representative devices: the tunneling FET (TFET) and the electrostatically actuated relay.

A TFET has *I-V* characteristics that are similar to those of a MOSFET: $I_{ds} \propto (V_{gs} + V_T)\exp(-B/(V_{gs} + V_T))$. Note that $S$ is very small at low current levels, but that it degrades as $|V_{gs}|$ increases. For relatively slow (sub-100 MHz) applications where $V_{dd}/I_{on}$ is not critical, a TFET has a smaller average $S$ value and hence can be more energy-efficient than a MOSFET. However, for high-performance applications requiring $I_{on}$ >100μA/μm, a TFET has a larger average $S$ value and hence would consume more energy than a MOSFET. Thus, the TFET is an attractive candidate to replace the MOSFET if variability can be kept under control and the performance is not critical; see Fig. 1.

Nanoscale relays with perfectly abrupt switching appear very attractive for ultra low power electronics. If one could realize this ideal switch with an $S_{eff}$~0mV/dec and zero leakage current, our model for $V_{dd\ min}$ breaks down. For these devices, the mininum $V_{dd}$ value is that which guarantees functionality while attaining a certain level of performance. $V_{dd}$ reduction for a relay is limited by the need to overcome worst-case (over all devices on a chip) surface adhesion forces in order to break physical contact. While current devices require >1V to operate, theoretically $V_{dd,min} = \sqrt{16g\Gamma/2}$ where $g$ is the as-fabricated actuation gap thickness and Γ is the adhesion energy. For $\Gamma = 2\mu J/m^2$ [3] and $g$ = 10nm, $V_{dd,min}$ < 50 mV might be possible.

From a performance standpoint, relays exhibit an inertial switching delay on the order of ns, which is generally several orders of magnitude larger than the electrical delay (on the order of ps). Therefore, an optimized relay-based circuit design would arrange for all mechanical movement to happen simultaneously – even if this substantially increases the electrical delay. Due to their alternate circuit topologies, energy-performance comparisons of relay- *vs.* MOSFET-based designs must be made at the circuit level rather than at the device level. A recent modeling study [4] shows that relay technology offers >10× reduction in energy per operation, compared with CMOS technology, for sub-GHz throughputs. However, realizing this potential benefit from a relay technology would require both much lower voltage operation and significant reliability improvements over today's mechanical switches. In order for a relay-based circuit to operate reliably for at least 10 years at a clock frequency of 100MHz and transition probability of 0.01, the relays must be able to endure ~$3x10^{14}$ on/off cycles before failure – which is orders of magnitude higher than the endurance of the most durable MEMS switches demonstrated to date.

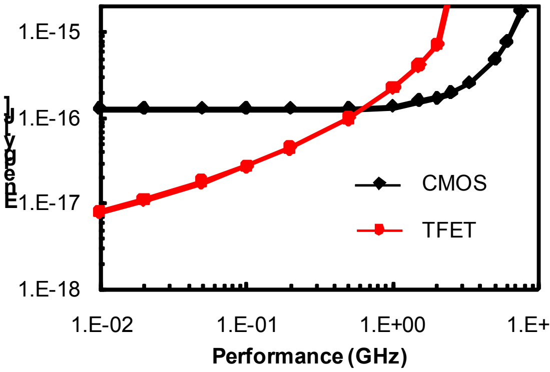

**Fig. 1:** Energy-Performance comparison of 30-stage 65nm CMOS inverter chain (transition probability=0.01, capacitance per stage=2.4fF) with a 65nm-equivalent TFET technology. Due to its alternate circuit topology, an energy-performance comparison of relay-based designs must be made at the circuit level [4] rather than at the device level.

## Conclusion

Circuit-level energy-performance analysis is necessary to assess the promise of any new device technology for potentially overcoming the energy-efficiency limitations of CMOS technology. Based on this analysis, TFET technology appears to be compelling for sub-100MHz applications. If relays can be fabricated with low surface forces and operated reliably over trillions of cycles, relay technology could potentially provide dramatic improvements in energy efficiency over a wider range of performance.

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**References:** [1]K. Gopalakrishnan *et al*. *IEDM* 2002, pp. 289–292. [2] W.Y. Choi *et al*., *IEEE-EDL* **28** 743 (2007) [3] J. A. Knapp *et al*., *JMEMS* vol. 11, no. 6, pp754-764, Dec 2002. [4] F. Chen *et al*., *IEEE/ACM ICCAD 2008.*