

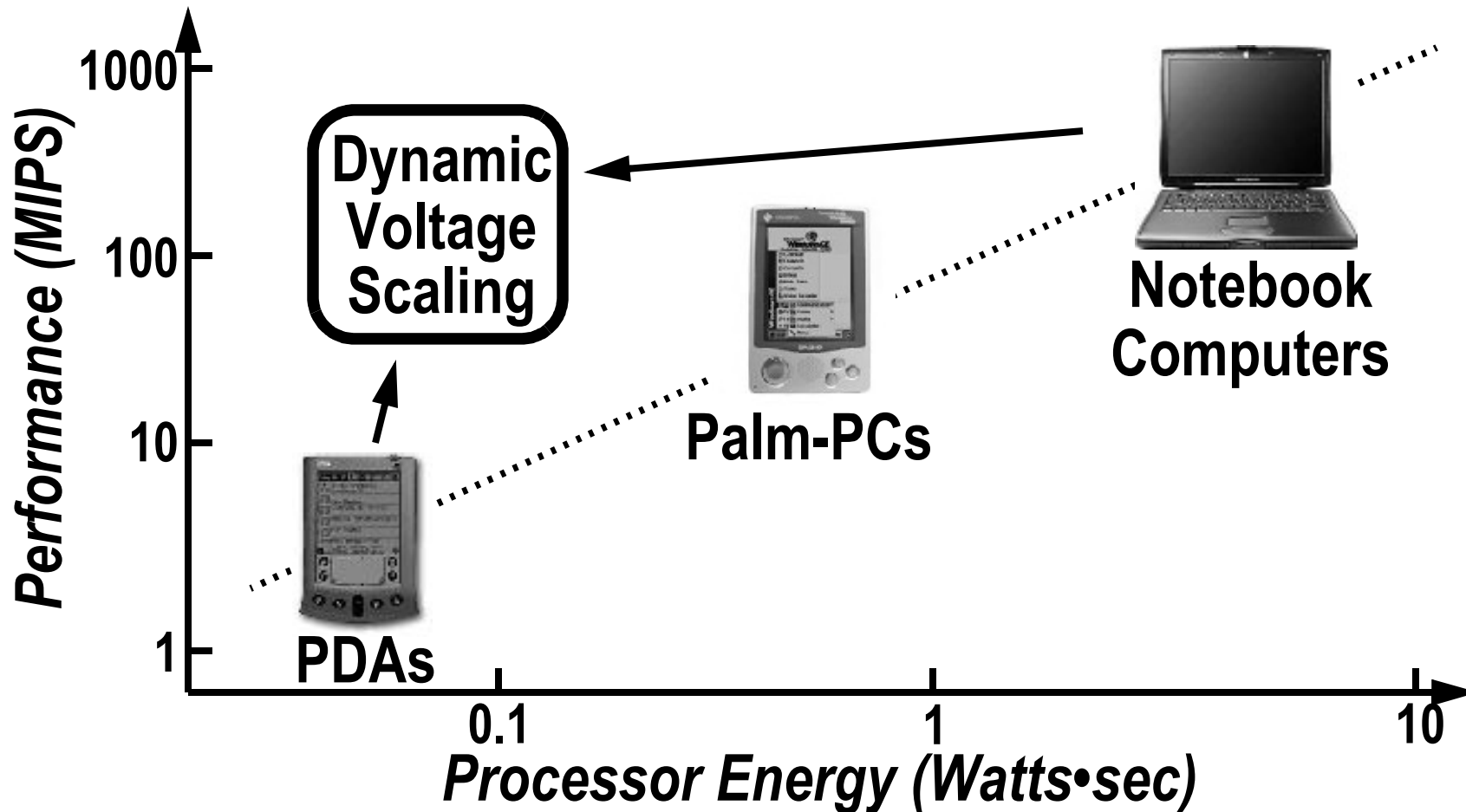
A Dynamic Voltage Scaled Microprocessor System

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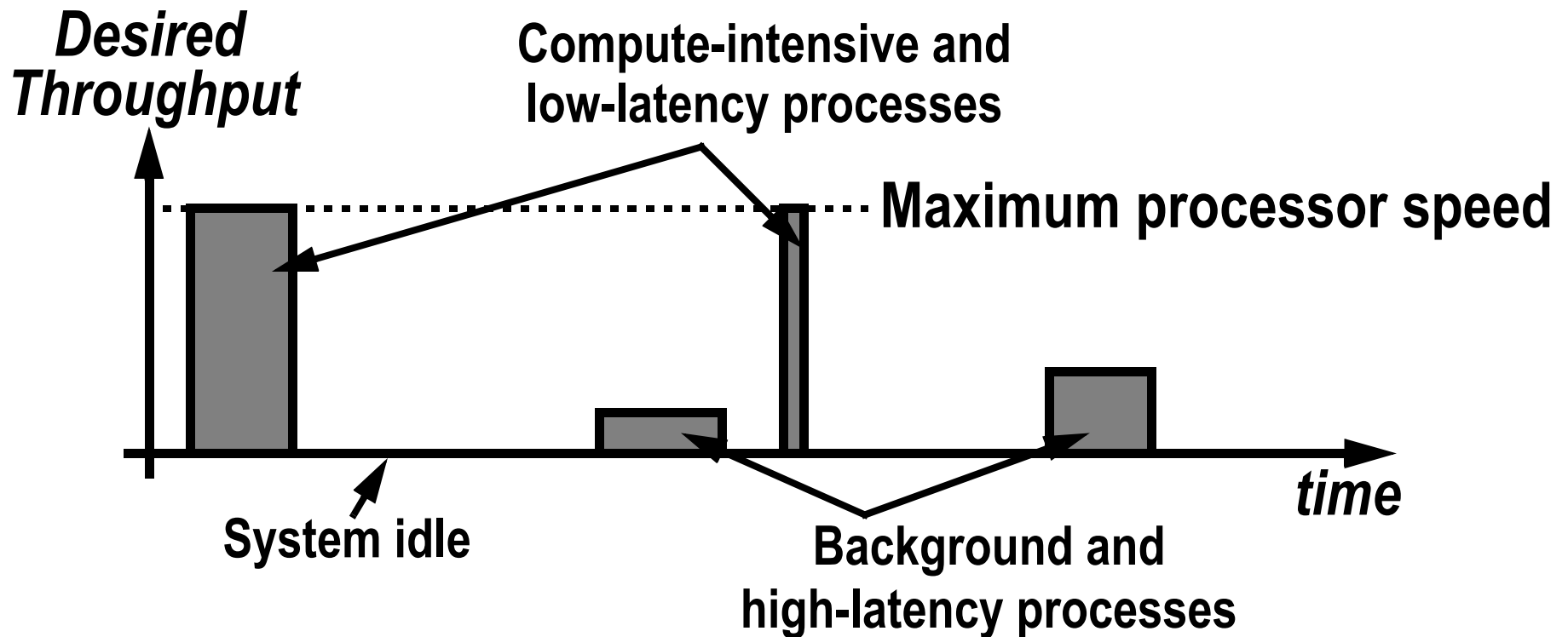
***Intel, **Volterra**

Processors for Portable Devices



- Trade-off performance for lower energy consumption

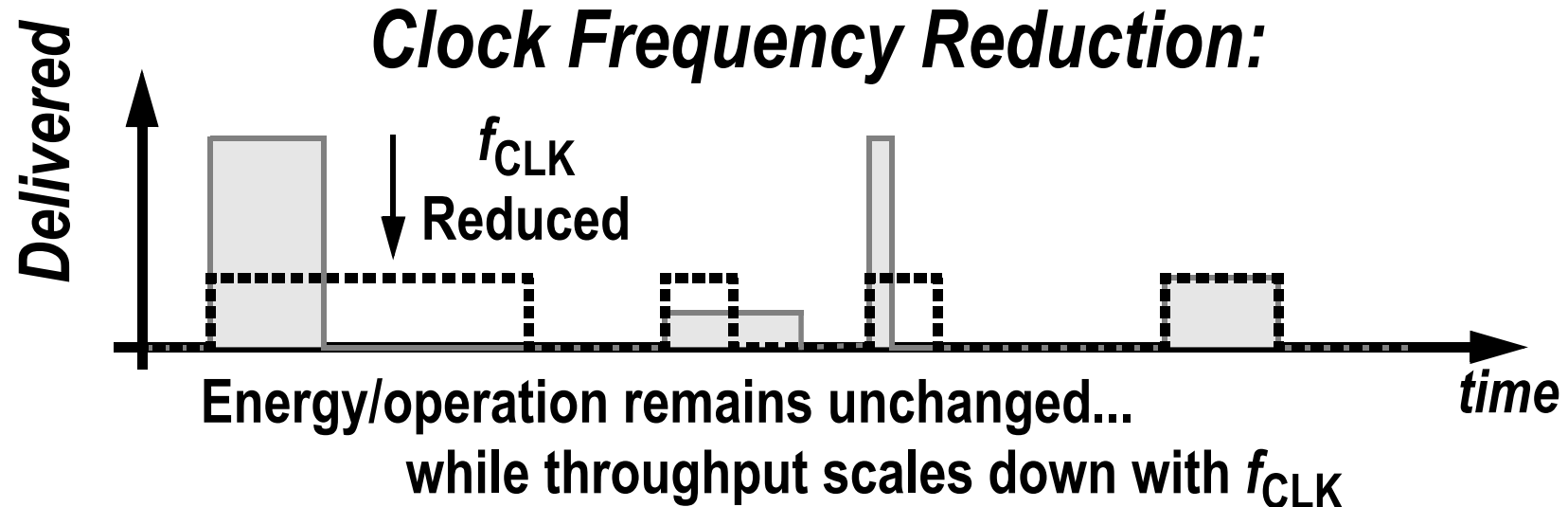
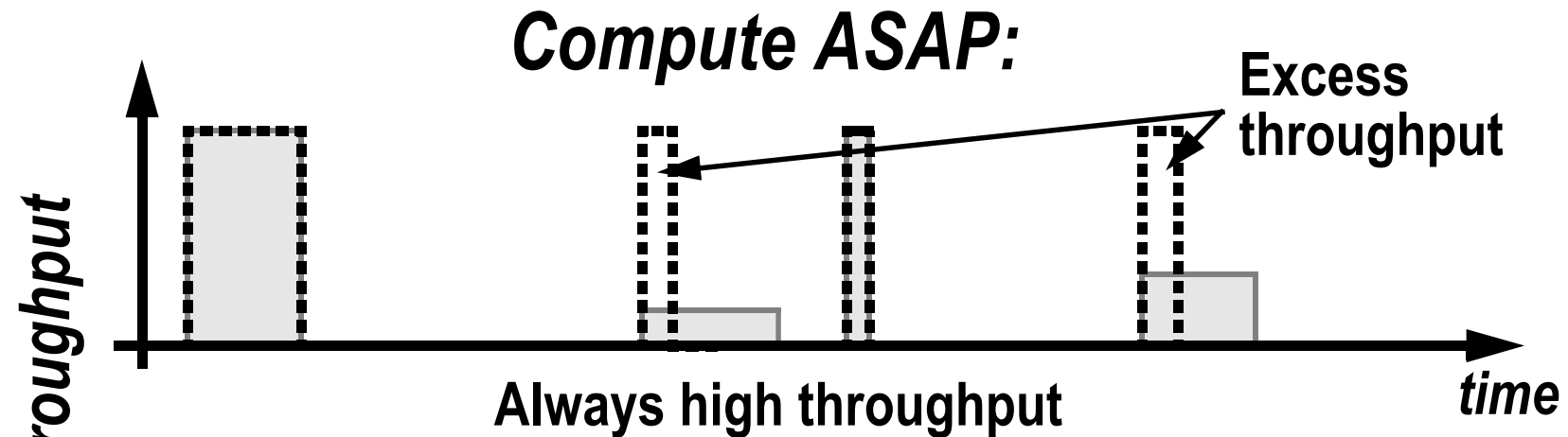
Processor Usage Model



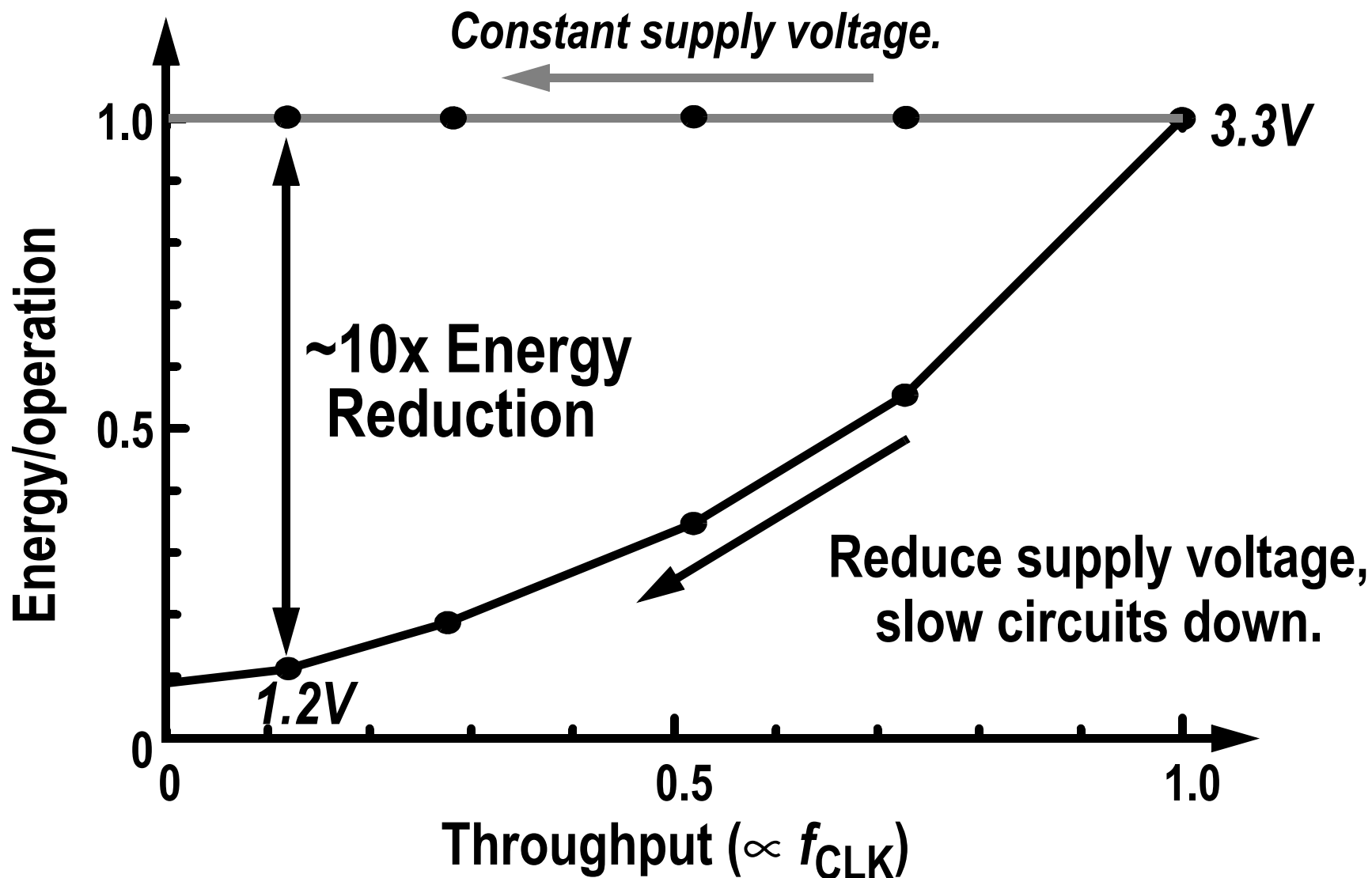
System Optimizations:

- Maximize Peak Throughput
- Minimize Average Energy/operation

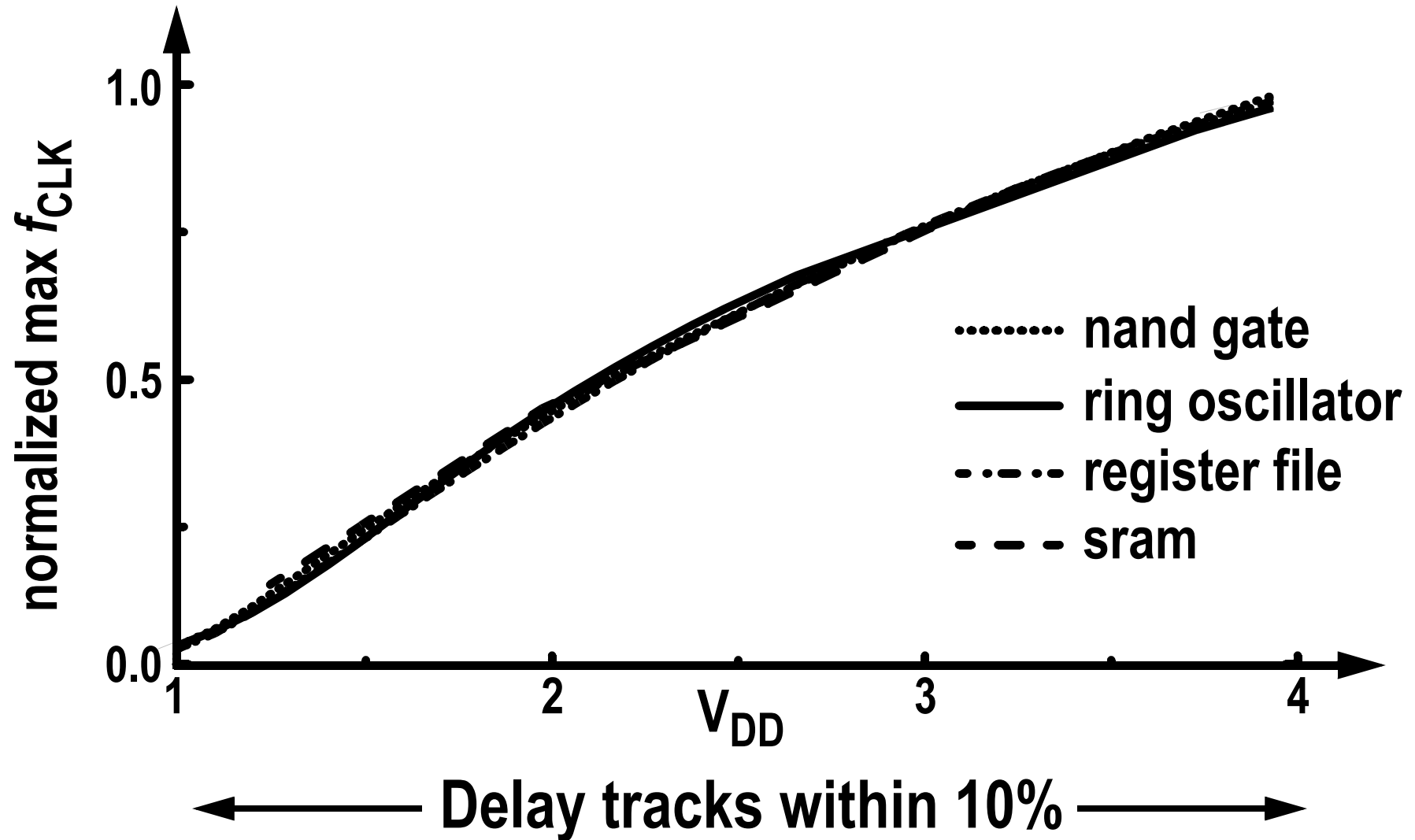
Common Design Approaches (Fixed V_{DD})



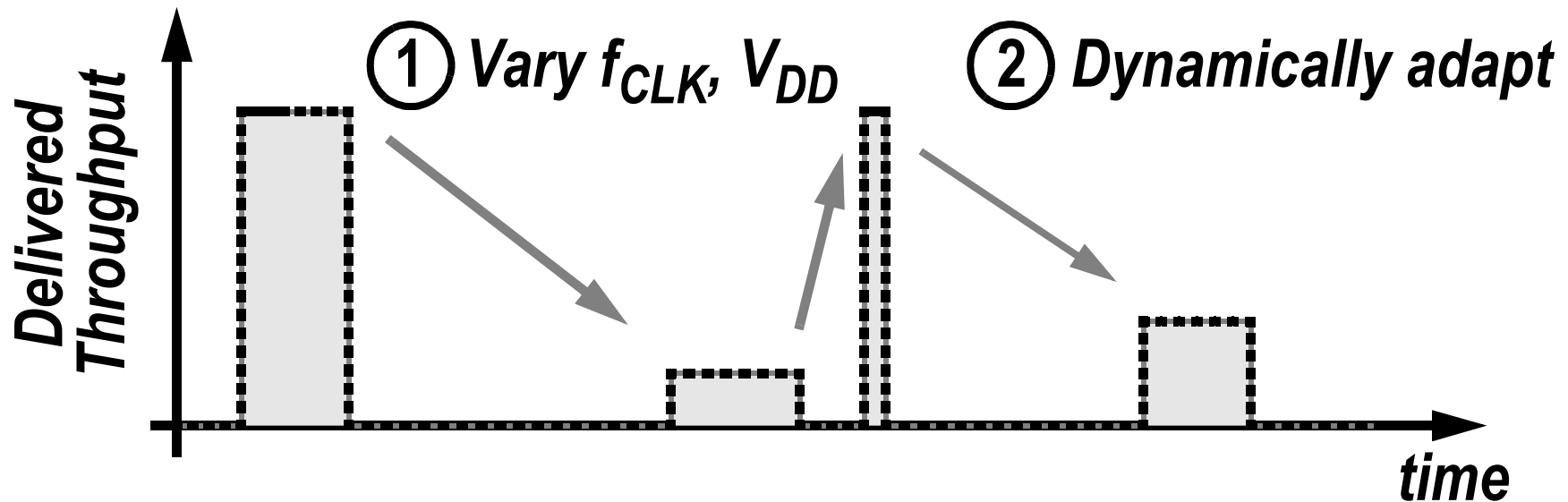
Scale V_{DD} with Clock Frequency



CMOS Circuits Track Over V_{DD}



New Approach: Dynamic Voltage Scaling (DVS)

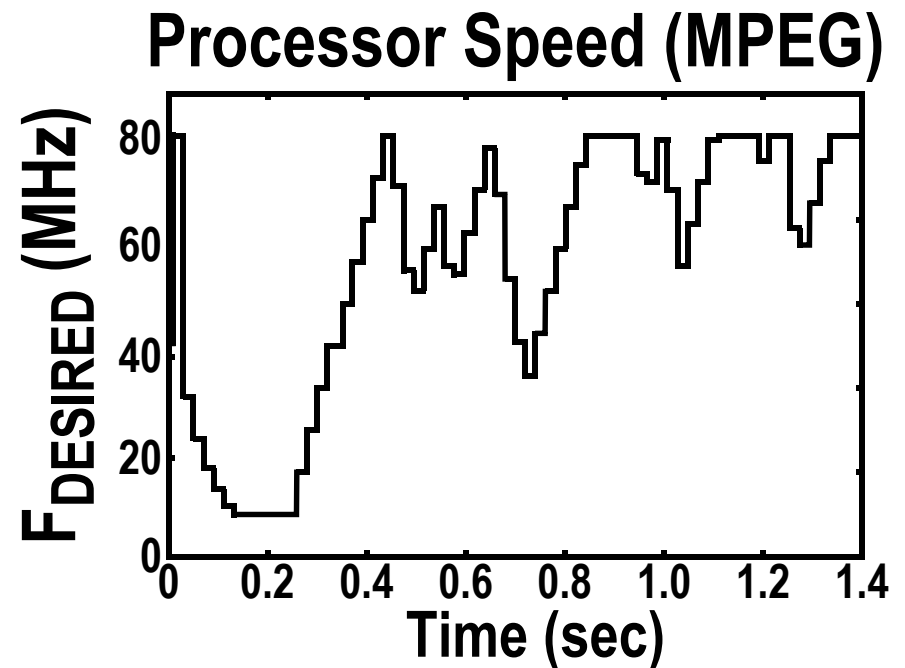


- Dynamically scale energy/operation with throughput.
- Always minimize speed \rightarrow minimize energy/operation.
- Extend battery life up to 10x with the same hardware.

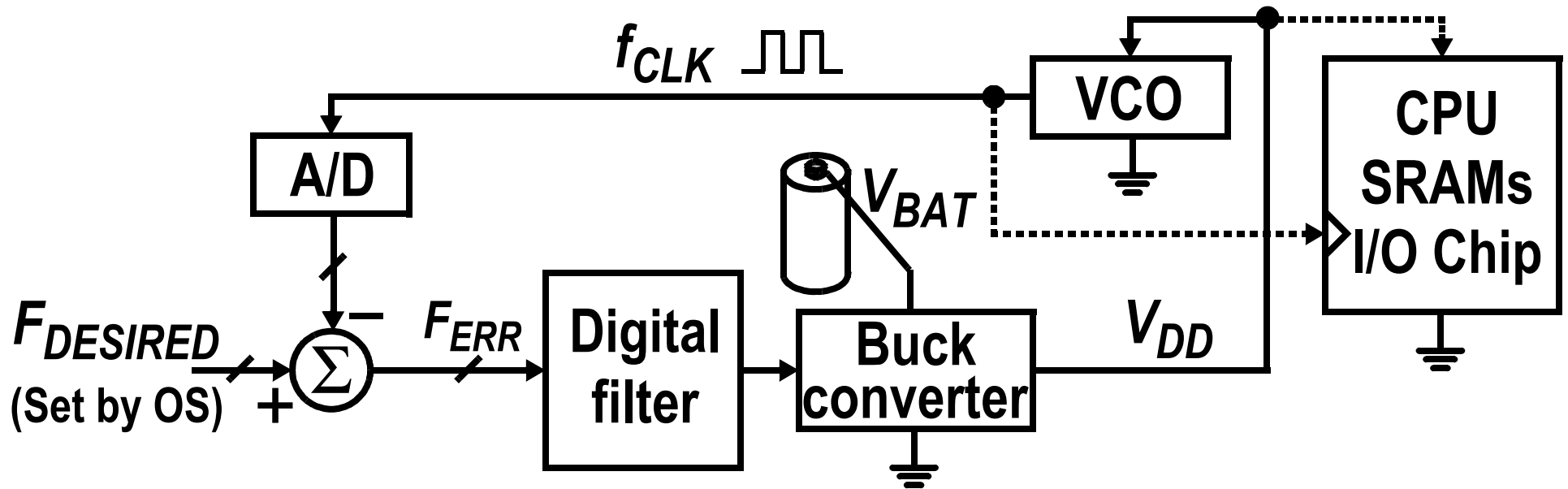
Operating System Sets Processor Speed

- DVS requires a *voltage scheduler (VS)*.
- VS predicts workload to estimate CPU cycles.
- Applications supply completion deadlines.

$$\frac{\text{CPU cycles}}{\Delta \text{ time}} = F_{\text{DESIRED}}$$

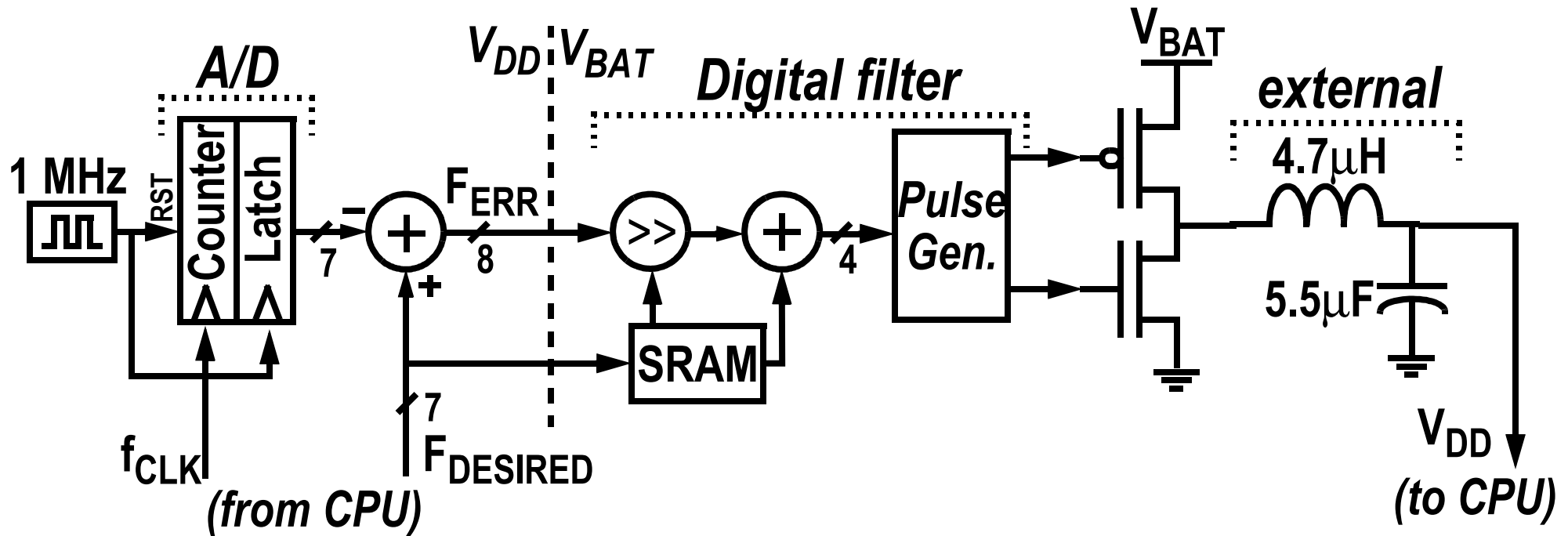


Regulation Loop Sets V_{DD} , f_{CLK}



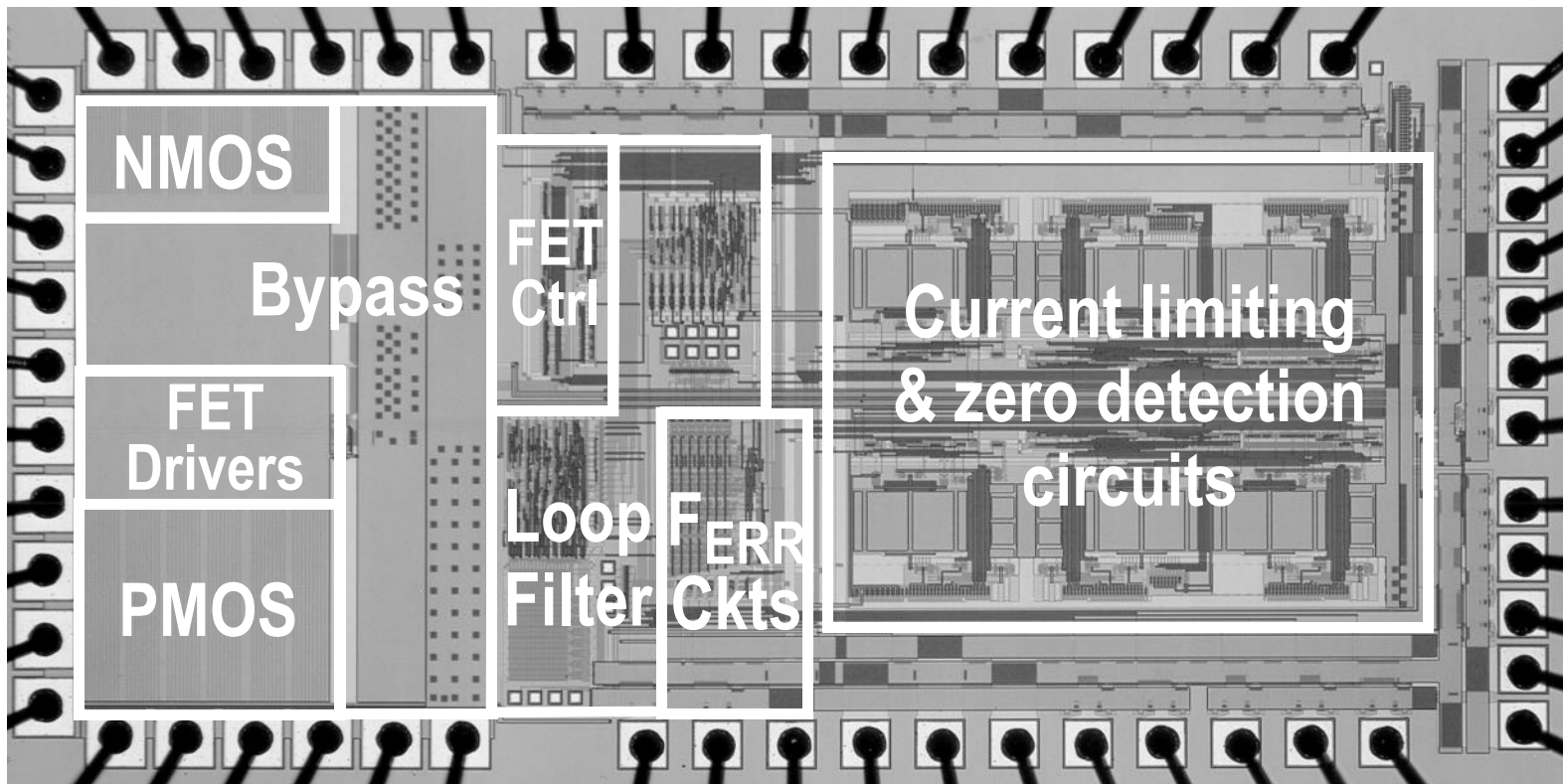
- Negative feedback loop forces f_{CLK} to lock to $F_{DESIRED}$.
- VCO: ring oscillator matched to CPU critical path.
- Loop provides voltage regulation & clock generation.

Regulator Chip Architecture



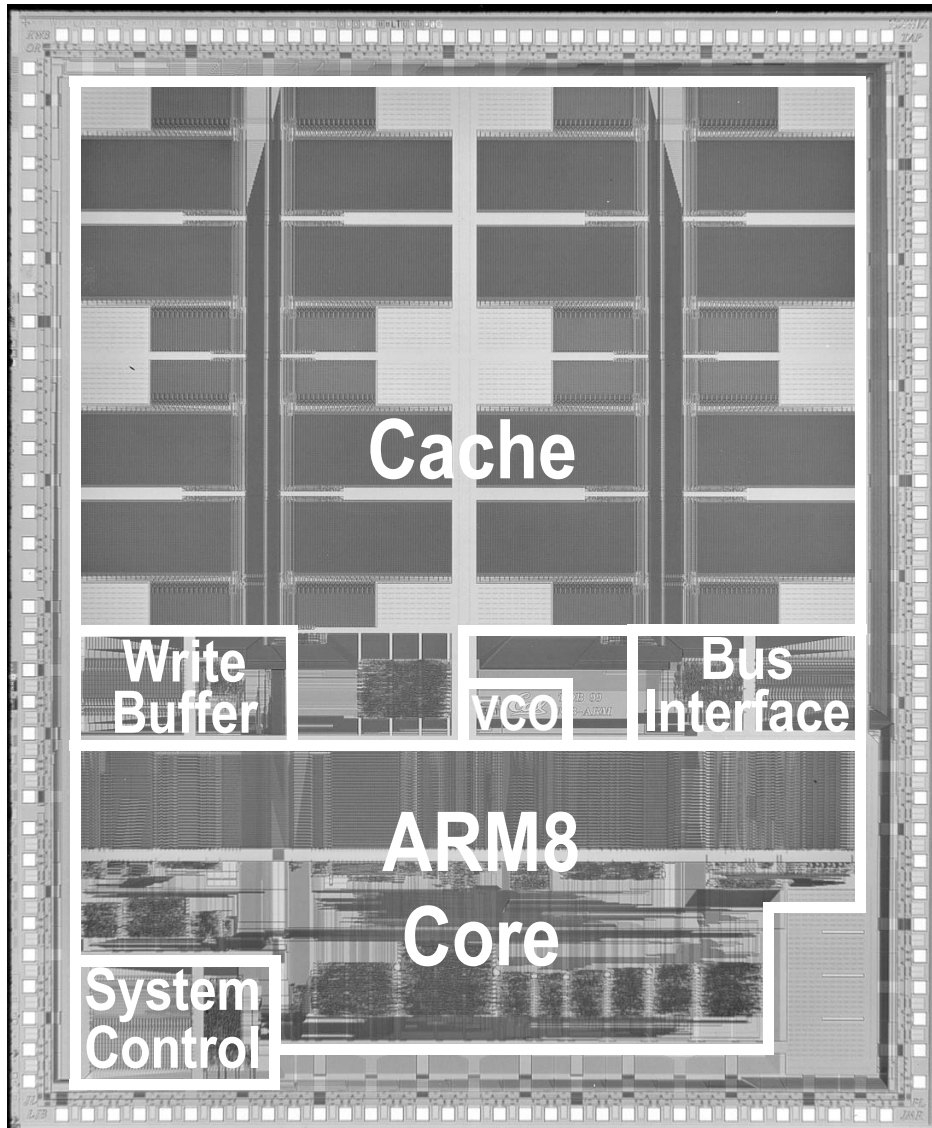
- Pulse generator uses a hybrid PWM/PFM algorithm.
- Track mode: regulator actively adapts up/down.
- Regulation mode: filter only activated for $F_{ERR} > 0$.

Regulator Chip



- **Size: 1.6 x 3.4 mm**
- **5MHz @ 1.2V, 2.7mA: 80% efficiency**
- **80MHz @ 3.8V, 125mA: 90% efficiency**

CPU Chip



- Transistors: 1.3M (Cache: 900k)
- Size: 7.5 x 9.0 mm

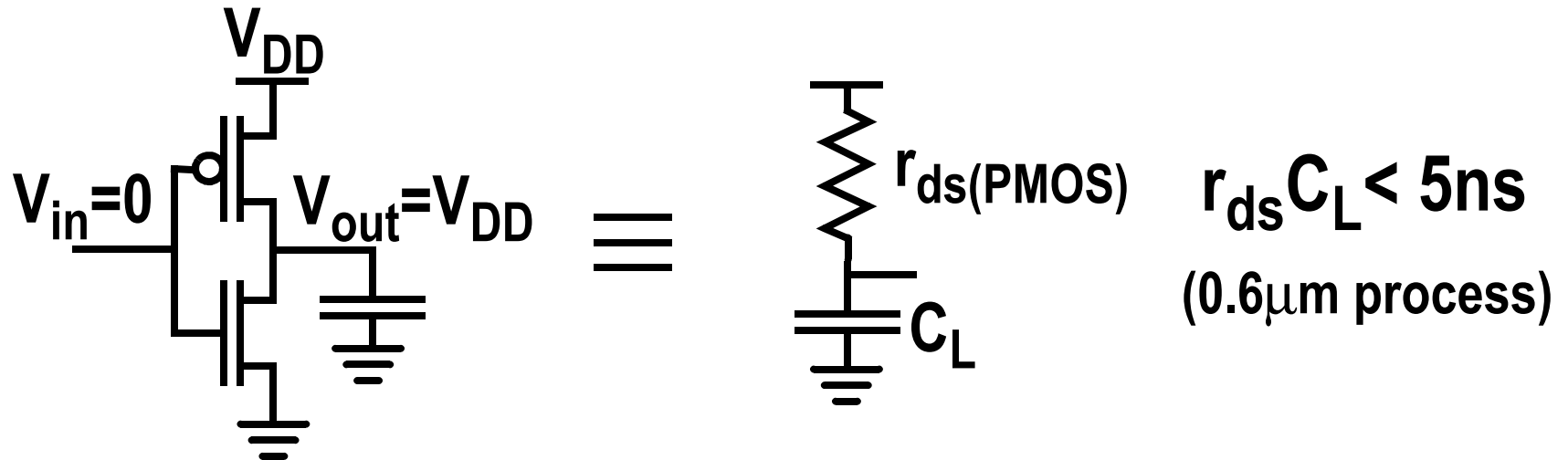
Features:

- 5-stage scalar pipeline
- Unified 16kB cache
- 12-element write buffer
- Memory & interrupt controllers, timer, and performance counters

Performance:

- 5MHz @ 1.2V: 6 MIPS, 2.8mW
- 80MHz @ 3.8V: 85 MIPS, 460mW

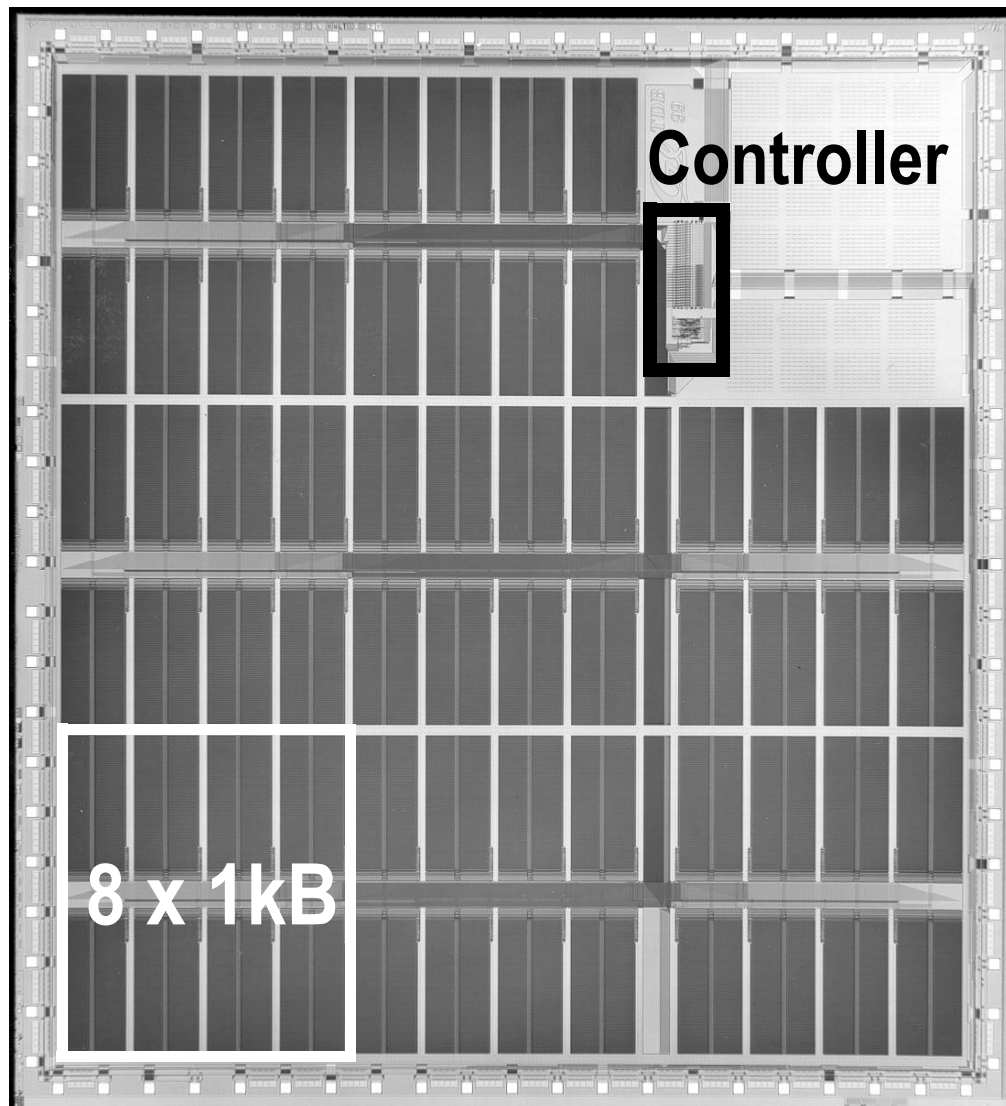
CMOS Circuits Can Tolerate High dV_{DD}/dt



but with some constraints....

- No NMOS-only pass gates.
- Requires full-rail logic.
- Capacitance can't hold state (e.g. DRAM).
- Dynamic logic should use weak feedback.

SRAM Chip



- Transistors: 3.4M
- Size: 9.6 x 10.4 mm

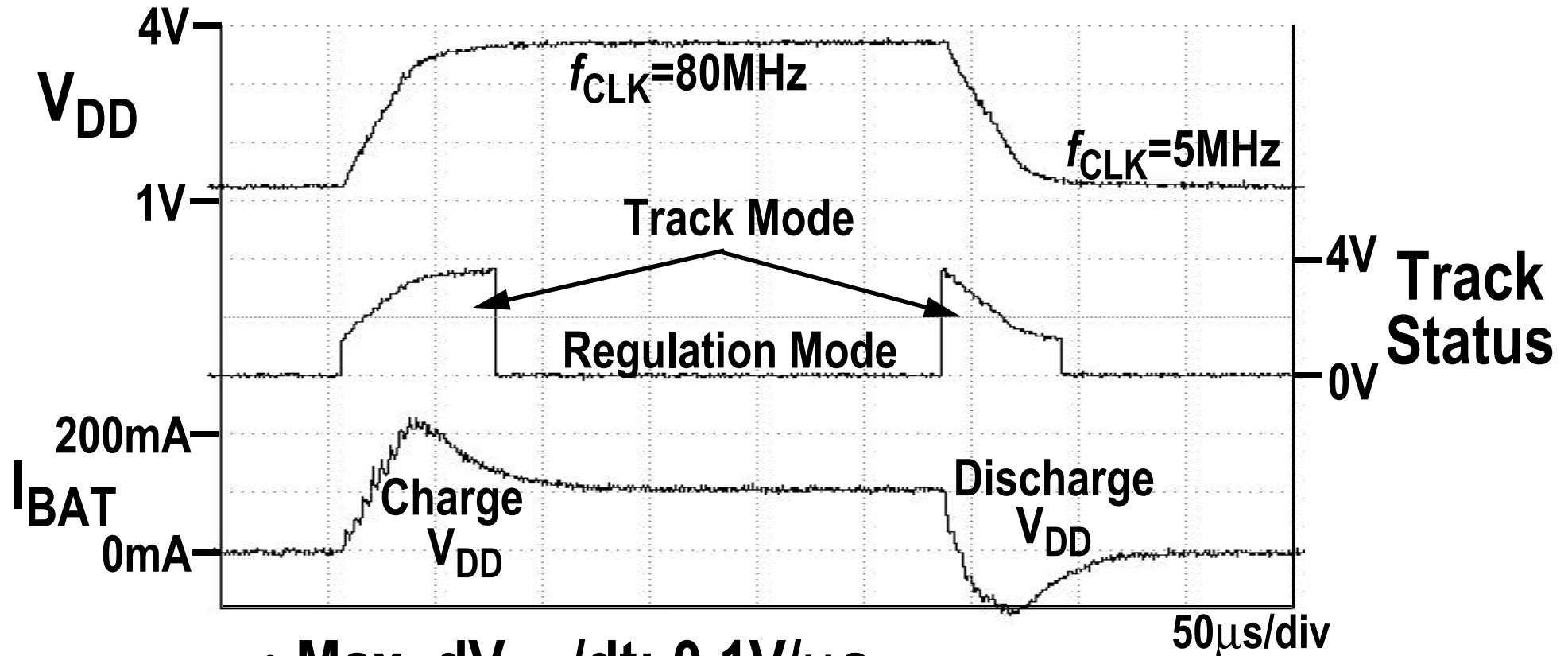
Features:

- 2-level hierarchy: 8 x 8 x 1kB
- Burst-mode accesses

Performance:

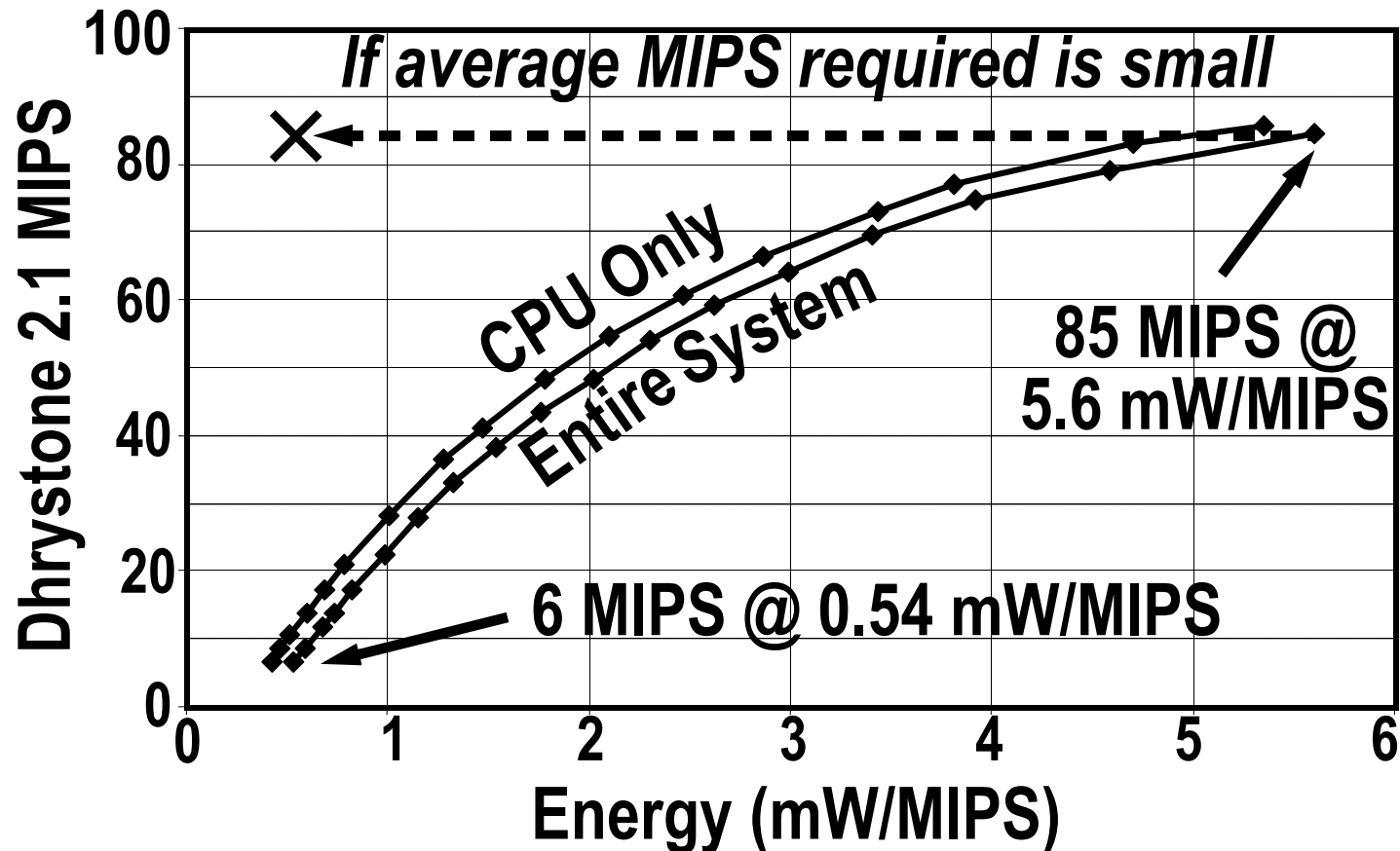
- 5 MHz @ 1.2 V: 1.3 mW
- 80 MHz @ 3.8 V: 220 mW

System Transient Response



- Max. dV_{DD}/dt : $0.1\text{V}/\mu\text{s}$
- Max. transition time: $70\mu\text{s}$ (1.2-3.8V)
- Max. transition energy: $4\mu\text{J}$ (1.2-3.8V)

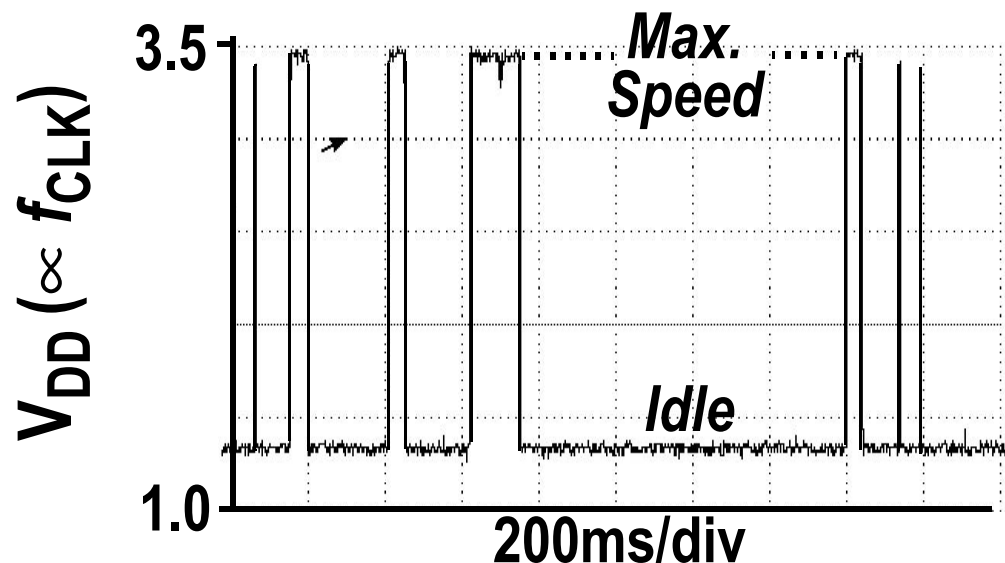
Measured Performance & Energy



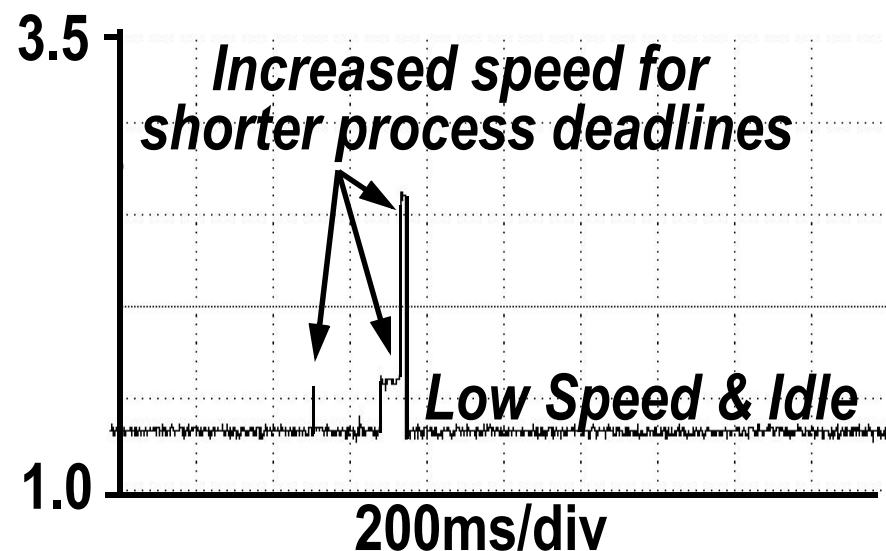
$$\frac{\text{Peak MIPS}}{\text{Average Power}} = \frac{85 \text{ MIPS}}{3.24 \text{ mW}} = 26200 \text{ MIPS/W}$$

DVS for Real Applications

Compute ASAP:



With Voltage Scheduler:



- **User-interface process: very bursty computation.**
- **High-latency computation done @ low speed/energy.**

Measured Benchmark Energy Consumption

(Normalized Energy)

Algorithm	Benchmarks		
	MPEG	UI	AUDIO
Compute ASAP	100%	100%	100%
Optimal	67%	25%	16%
<i>ZERO</i>	89%	30%	22%

- **ZERO is implemented heuristic algorithm.**
- **Difficult to optimize compute-intensive code (MPEG).**
- **Big drop in energy when less speed required (3.3-4.5x).**

Conclusions

- **DVS eliminates the energy-performance trade-off.**
- **Successfully demonstrated DVS on a full system.**
- **CMOS circuits very amenable to DVS.**
- **DVS can deliver more than 10,000 MIPS/W.**