

A 1.5V 0.7-2.5GHz CMOS Quadrature Demodulator for Multi-Band Direct-Conversion Receivers

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Abstract - This paper presents an integrated quadrature demodulator with on-chip frequency divider implemented in a 0.13 μm CMOS technology. The mixer consists of a transconductance stage, a passive current switching stage, and an operational amplifier output stage. A complementary input architecture has been used to increase the transconductance for a given bias current. From 700MHz to 2.5GHz, the demodulator achieves 10dB DSB NF with 9-33 kHz $1/f$ -noise corner and 35dB of low frequency voltage gain. The total chip draws 20mA-24mA from a single 1.5V supply.

I. INTRODUCTION

With the proliferation of wireless standards and frequency bands of operation, there is an urgent need to design a single transceiver that is compatible with multiple standards. The direct conversion (zero-IF) is attractive for the transceiver due to its high level of integration and the simplicity of the baseband circuitry. Despite the attractiveness, designing such a mixer for multi-band operations in deep-submicron CMOS technology is nontrivial. The main challenge lies in maintaining moderate gain, noise figure, and linearity at minimum current consumption across a wide frequency spectrum with the abating supply voltage.

This paper presents the design of a wideband CMOS quadrature demodulator based on the passive current switching mixer with active first order RC filtering at its output [1][2][3]. Complementary folded inputs [4][5] are employed to obtain higher transconductance efficiency. No inductor has been utilized in order to realize a wideband demodulator. The elimination of inductors also leads to significant die area reduction and reduced substrate coupling due to the sheer large dimension of inductors especially at low GHz frequencies. The circuit operates at a wide range of frequencies from 700MHz to 2.5GHz suitable for many applications such as GSM/DCS/CDMA2000 cellular standards, as will be shown in later sections.

This paper is organized as follows. In section II, the architecture of the demodulator will be discussed. The circuit design details for the mixer and the frequency divider will be presented in section III followed by the implementation and measurement results in section IV.

II. ARCHITECTURE OVERVIEW

The demodulator block diagram is shown in Fig. 1. It consists of two separate mixers and a quadrature local oscillator (LO) generation circuit. The divide-by-two circuit is implemented to generate quadrature LO signals from the external $2f_{LO}$ source. The on-chip frequency division effectively isolates the signal coupling between LO and RF ports and reduces the reciprocal mixing considerably.

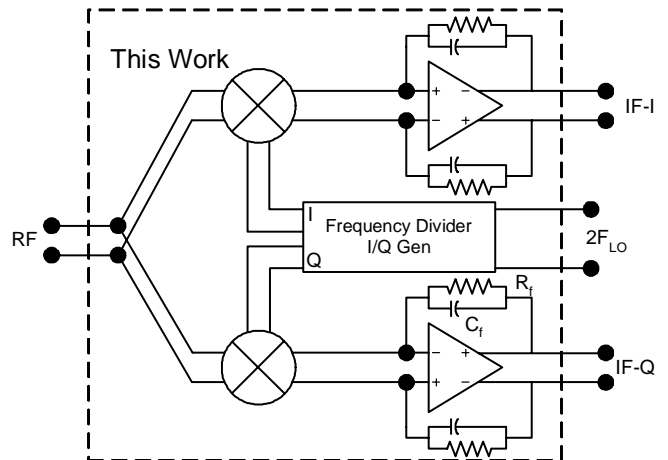


Fig. 1. Demodulator architecture overview.

The mixer core consists of an RF transconductor stage followed by a fully balanced switching quad. All the signal paths are realized in differential style in order to suppress common-mode noise and second order nonlinearity. The RF, as well as the LO signals are AC coupled into the mixer core through several linear Metal-Insulator-Metal (MIM) capacitors. The IF voltages are built at the operational amplifier output after the RF current is commutated and passes the first order RC low-pass filtering. The operational amplifiers provide virtual ground at the mixer core output and hence relieve the linearity degradation imposed by the limited voltage headroom [2][3].

The input RF voltage is converted into current by the transconductance stage and DC coupled to the switching pairs, as shown in Fig. 2. By removing capacitors between the stages (used for DC blocking), we realize minimum parasitic capacitance by compact routing. Denoting C_{PAR} as the parasitic capacitance at the output node of the transconductance stage, since the noise contribution from the op-amp itself at the mixer output is affected by C_{PAR} and is given by [3]

$$\overline{v_{n,out}^2} \approx (1 + 8R_f f_{LO} C_{PAR})^2 \overline{v_{n,opamp}^2} \quad (1)$$

Unlike narrow-band designs, C_{PAR} can not be easily tuned out for the entire frequency range. Since the op-amp design is dictated by the low voltage and low power consumption requirements, it also constitutes a nontrivial portion of the mixer noise, especially in the $1/f$ region. Minimizing C_{PAR} allows for a less stringent noise specification upon the op-amp which favorably translates into lower power consumption circuit design. On the other hand, two sets of common-mode feedback circuits, one for the transconductance stage and

another for the operational amplifier, need careful designs to ensure proper operating point, as detailed in section III.

III. CIRCUIT DESIGN

A. Transconductance

The transconductance stage of the mixer is shown in Fig. 2. It consists of a differential complementary pair with a common-mode feedback circuit. Since there is no AC coupling capacitor between this stage and the switches, low frequency intermodulation tones created by second-order nonlinearity will transfer to the next stages given any mismatch exists. Thus it is important to reduce the second order nonlinearity in this stage by using a fully differential topology. Although using the fully differential topology requires extra headroom for the pair, the RF voltage swing at this stage is low due to the virtual ground set by an operational amplifier.

The common-mode voltages at the mixer and the operational amplifier outputs are set at $V_{dd}/2$ in order to obtain the highest output swing. By setting the same common-mode voltages on both sides of the switches, their bias currents can be minimized. The I/Q mixer altogether with the common-mode and bias circuits consume 10mA.

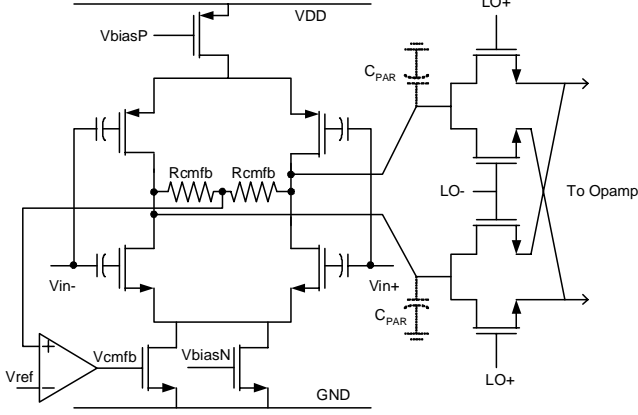


Fig. 2. Transconductance and switching stages.

B. Switches

The switches consist of four transistors forming a double-balanced structure. The LO signals are AC coupled via capacitors while the DC bias level of the switches is set at a level close to threshold of conduction in order to achieve the lowest on-resistance while preventing overlapping on-periods. The switches should be sized big enough in order to minimize the on-resistance. However, LO power consumption as well as noise contributions from the operational amplifier determine an upper limit on the size due to parasitic capacitances.

C. Op-amp and the Feedback Load

A two-stage topology was chosen for the op-amp design in order to obtain both high signal swing and low input-referred noise. The input referred noise of the operational amplifier is given by [6]

$$\overline{v_{n,in}^2} = 8kT\gamma \frac{1}{g_{m1}} \left(1 + \frac{g_{m2}}{g_{m1}} \right) + \frac{2}{fC_{ox}} \left(\frac{K_N}{(WL)_N} + \frac{K_P}{(WL)_P} \frac{g_{m2}^2}{g_{m1}^2} \right) \quad (2)$$

In order to reduce op-amp's noise contribution, the input NMOS transistors were sized to have a high (W/L) ratio with a long channel length while the PMOS have a low (W/L) ratio with a long channel length. The output stage of the amplifier is simply a common-source stage and provides almost rail-trail output swing. The op-amp is designed to be able to handle the currents swing from the transconductance stage for the linear input range. For instance, the slew rate of the op-amp must be high enough to handle the current changes of

$$\frac{di_{out}}{dt} = \frac{2}{\pi} \omega_{IF} (g_{m1} + g_{m2}) v_{RF} \quad (3)$$

The feedback resistors were chosen to be large in order to reduce the associated thermal current noise. The upper limit of the resistor value was set by linearity and voltage gain of the circuits. The feedback capacitors are large in order to attenuate the out-of band blockers [7]. Although using big feedback capacitors creates a low-frequency gain roll-off at the IF output, this can be characterized and corrected in later stages as long the noise figure is low and the gain is high enough for the IF frequency of interests. In practice, available chip area and gain of the circuit determine the upper limit of the capacitor value. The opamps draw a total of 3.5mA from the supply (both I and Q).

D. Frequency Divider and LO Buffers

The LO generation path of the mixer is as shown in Fig. 4(a). The first 2 inverters in parallel act as the input buffer to restore the high frequency waveform distorted by the packaged pin, bond wire and pad parasitics. A symmetric LO waveform is critical in ensuring the balanced switch operation so that the switching quad itself does not pose a substantial degradation to the mixer noise figure as well as the second order intermodulation product [8][9]. A divide-by-two frequency scheme is employed to produce 50% LO duty cycle so as to minimize LO asymmetries. The LO frequency ranges from 700MHz to 2.5GHz, while the divider operates at twice this frequency. This translates into higher power consumption and the need for a larger balun bandwidth. For testing purposes, multiple baluns were used to accommodate the entire frequency range.

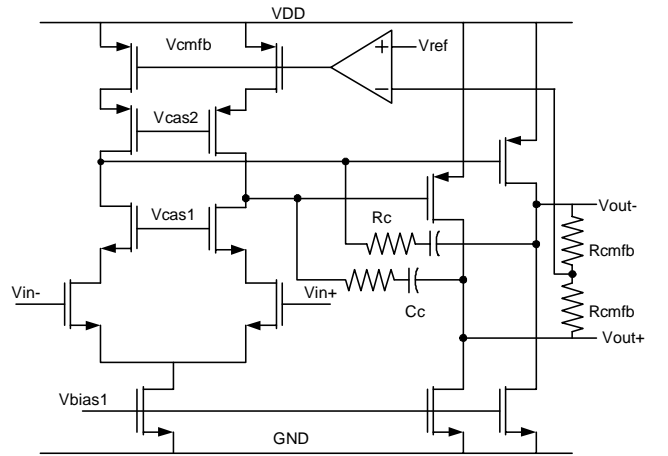


Fig. 3. Simplified operational amplifier schematic.

The divide-by-two was implemented in Current Mode Logic (CML) style. The core of the divider block consists of 2 CML flip-flops with the output cross toggled back to its input. The circuit is shown in fig. 4(b). The CML divider draws constant current and has the advantage of generating less current spikes during its dynamic operation which may propagate and appear as noise to other sensitive RF nodes. Because differential signaling is utilized in the CML divider, both I and Q LO outputs with good matching are available. A level converter between the input inverter and CML divider consisting of cascading 3 CML stages as in Fig. 4(c) without the clocked gate and the latch converts signal from the CMOS logic domain to the CML domain.

Larger LO swing expedites the switch quad transition and helps improve the mixer noise figure and second order intermodulation product [8][9]. The mixer core design requires the LO differential swing of at least $1.5V_{pk-pk}$ from a supply of 1.5V. Two scaled inverters were cascaded in each path to provide sufficient drive capability. The driving inverters consume 4.1mA and the CML circuits consume 1.43mA (both I and Q).

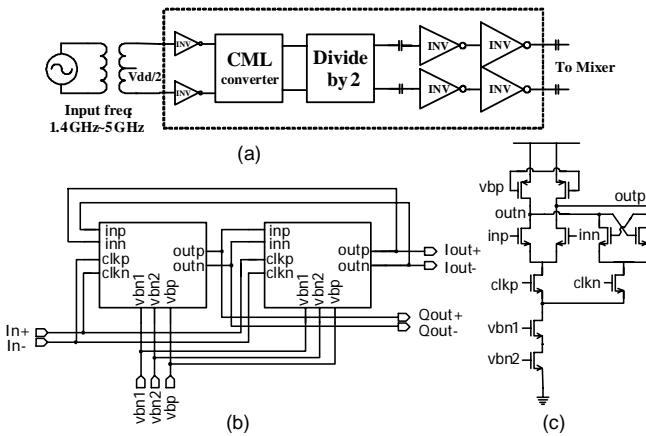


Fig. 4. LO generation circuitry.

IV. EXPERIMENTAL RESULTS

A. Measurement Setup

The prototype chip was fabricated in a $0.13\mu\text{m}$ CMOS technology and occupies an active area of $0.8\text{mm} \times 1\text{mm}$. All the pads are ESD protected. Approximately 60% of the chip area is allocated to the feedback capacitors of the operational amplifiers. The packaged chip was mounted on the PCB board for testing and on-board baluns were used to perform single-ended to differential conversion at the mixer and LO inputs. An external 100Ω resistor was placed at the mixer RF input to provide the input matching for measurement purposes. At the output of the chip, buffers were used to convert the differential outputs to a single ended output and to drive low-impedance measuring cables. Noise contributions from the buffers were significant at IF frequencies higher than 2MHz due to mixer gain roll-off and were de-embedded.

B. Measurement Results

The conversion gain plot for 900MHz and 2.1GHz is shown in Fig. 5. Conversion gain at 1kHz IF and -3dB bandwidth of the mixer from 700MHz to 2.5GHz are plotted in Fig. 6. The measured conversion power gain is close to

38.5dB and the “voltage” gain of the mixer is approximately 3dB below the measured power gain due to 3dB voltage gain of the balun.

The measured double sideband noise figure (DSB NF) at 900MHz and 2.1GHz are shown in Fig. 5. In addition, the DSB NF at 1MHz IF and $1/f$ noise corner at different LO frequencies are shown in Fig. 7. The measured noise figure floor was near 10dB and the $1/f$ noise corner was lower than 35kHz across the LO frequency range. The $1/f$ noise increases with higher LO frequencies because of more noise contribution from the operational amplifier as predicted from (1). However, the $1/f$ noise corner increases faster than expected as a function of LO frequency due to additional parasitic capacitances at the transconductance output.

Since the baluns were glued on the same PCB board with the mixer chip, leaving no probing space in between for characterizing the balun loss at different frequencies, the measured mixer gain, noise, and linearity values reported here reflects the combined effect and shows a variation of roughly 1dB.

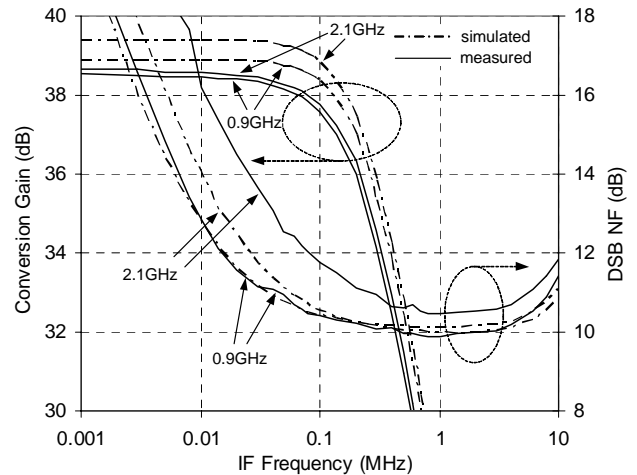


Fig. 5. Gain and NF plots at 900MHz and 2.1 GHz f_{LO} .

The two-tone linearity test results are shown in Fig. 8 for 900MHz and 2.1GHz LO frequencies. The intermodulation (IM) products were located in-band at 30kHz for all cases. All the input-referred intercept points were calculated from the input-referred powers of tones and IM products. Due to high conversion gain at low IF frequency, the output compression point of the opamp limits the input-referred linearity of the circuit and the IIP_3/IIP_2 increases as the gain decreases. Above 2MHz, the IIP_3 and IIP_2 flatten out or start to decrease due to limitations from the transconductance and the switches as well as lowered op-amp loop gain. At 1MHz offset, the achieved IIP_3 was +11dBm and IIP_2 was +64dBm. IIP_2 was measured for five samples and the minimum is higher than 60dBm at this frequency. In Fig. 8, one observes an abrupt IIP_3/IIP_2 dip at IF offset around 5MHz. This is attributed to an unintended peaking in the op-amp’s common-mode transfer function. The problem can be prevented in the future designs by carefully modifying the common-mode circuit.

The 1dB output compression point (P-1dB) of the circuit is limited by the output swing and varies with the blocking signal offset. For 900MHz f_{LO} , the measured input P-1dB at

100kHz, 1MHz, and 10MHz offsets are -25.8dBm, -13.5dBm, and -5.6dBm, respectively. The measured LO-RF leakage was -74dBm on average with the maximum value of -62dBm. The output DC offset is 19.5mV_{rms}. This translates to 0.35mV_{rms} average input referred offset assuming 35dB voltage gain. The estimated image rejection (IR), calculated from gain and phase mismatches, ranges between 20dB to 47dB depending on the LO frequency. The limitations come from the phase mismatches due to duty cycle error of the 2f_{LO} driving signal before reaching the divide-by-two circuits caused by balun and package parasitics. The total chip consumes 20mA at 700MHz and 24mA at 2.5 GHz from a 1.5V supply. The highest operating frequency is up to 2.56GHz and is limited by the divider.

IV. CONCLUSION

A low 1/f noise inductorless quadrature demodulator is presented. A fully differential complementary pair was used to increase the efficiency of the transconductance. The circuit operates over a wide range of frequencies including the 0.7-2.5GHz frequency bands. With the exceptions of some very stringent standards, the architecture is suitable as an integrated solution for multi-band receiver front-ends.

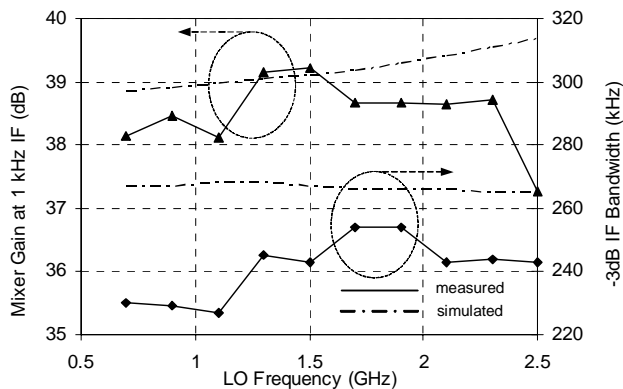


Fig. 6. Measured low frequency gain and bandwidth of the circuit.

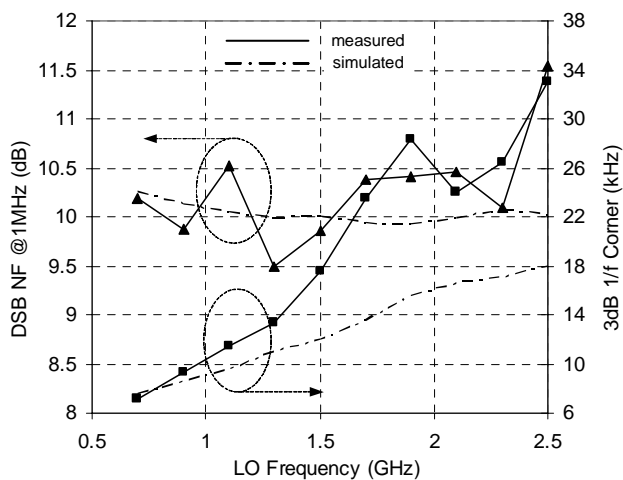


Fig. 7. Noise characteristics at different f_{LO}.

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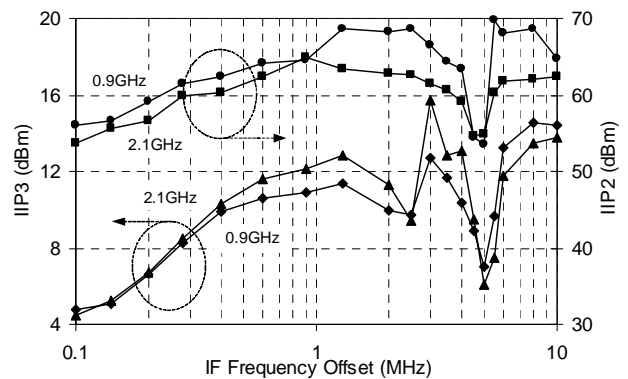


Fig. 8. Measured IIP₂ and IIP₃ at 900MHz and 2.1GHz.

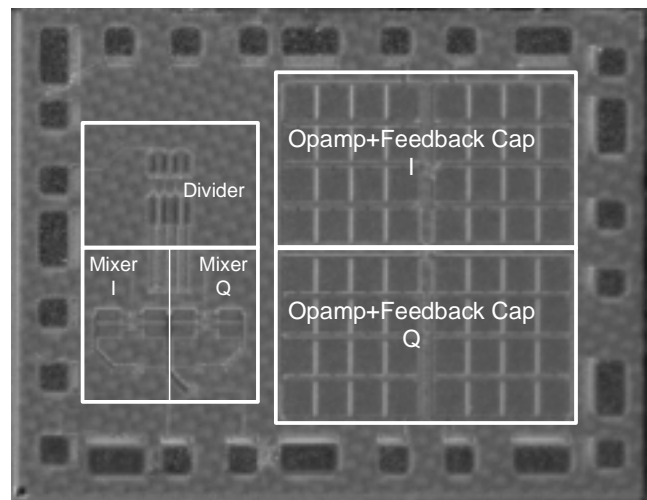


Fig. 9. Microphotograph of the chip.

REFERENCES

- [1] S. Zhou and M. F. Chang, "A CMOS Passive Mixer with Low Flicker Noise for Low-Power Direct-Conversion Receiver," *IEEE J. Solid-State Circuits*, vol. 40, No. 5, pp. 1084-1093, May 2005.
- [2] M. Valla, G. Montagna, R. Castello, R. Tonietto, and I. Bietti, "A 72-mW CMOS 802.11a Direct-Conversion Front-End With 3.5-dB NF and 200-kHz 1/f Noise Corner," *IEEE J. Solid-State Circuits*, vol. 40, No. 4, pp. 970-977, Apr. 2005.
- [3] E. Sacchi, I. Bietti, S. Erba, L. Tee, P. Vilmercati, and R. Castello, "A 15mW, 70kHz 1/f Corner Direct Conversion CMOS Receiver," in *Proc. IEEE Custom Integrated Circuits Conf.*, San Jose, CA, Sep. 2003, pp. 459-462.
- [4] V. Vidojkovic, J. Tang, A. Leeuwenburgh, and A. H. M. Roermund, "A Low Voltage Folded-Switching Mixer in 0.18-um CMOS," *IEEE J. Solid-State Circuits*, vol. 40, No. 6, pp. 1259-1264, June 2005.
- [5] D. Manstretta, R. Castello, and F. Svelto, "Low 1/f Noise CMOS Active Mixers for Direct Conversion," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 48, no. 9, pp. 846-850, Sep. 2001.
- [6] B. Razavi, *Design of Analog CMOS Integrated Circuits*, McGraw-Hill, New York, 2001.
- [7] V. Aparin *et al.*, "A Fully-Integrated Highly Linear Zero-IF CMOS Cellular CDMA Receiver," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, San Francisco, CA, Feb. 2005, pp. 324-325.
- [8] H. Darabi and A. A. Abidi, "Noise in RF-CMOS Mixers: A Simple Physical Model" *IEEE J. Solid-State Circuits*, vol. 35, no. 1, pp. 15-25, Jan. 2000.
- [9] D. Manstretta, M. Brandolini, and F. Svelto, "Second-Order Intermodulation Mechanisms in CMOS Downconverters," *IEEE J. Solid-State Circuits*, vol. 38, no. 3, pp. 394-406, Mar. 2003.