X/Ku Band CMOS LNA Design Techniques

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***Abstract*— This paper reports two 11 GHz low-noise amplifiers (LNA) in 0.18μm CMOS technology. A cascade two stage LNA achieves 12 dB of power gain, 3.5 dB of noise figure, and an input/output match of -15 dB/-27 dB at 11GHz, while consuming 28mA from 1.8V supply. The second LNA is a modified cascode amplifier and it achieves 8 dB of gain, 3.1 dB of noise figure, and an input/output match of -12 dB/-15 dB at 11GHz, consuming 18mA from the 1.8V supply. The paper also discusses design considerations such the effects of layout on frequency tuning and noise.**

I. Introduction

Rapid evolution of wireless communication has resulted in a continuous trend towards utilizing higher frequencies for wideband communication applications. CMOS technology is of major interest for its low cost and high level of integration. While much research has been done on integrating cellular and WLAN transceivers in CMOS and SiGe technology [1], very little work has been done at 10GHz (X-band, Ku-band). There are many interesting and important commercial applications in this frequency band, such as the satellite communication receivers for entertainment and high speed internet access. Current microwave receivers at this frequency are not only physically large, but are also expensive. Realization of such devices in standard CMOS will enable wider commercial adoption. On the other hand much research activity has recently focused on higher frequencies, such as the 60GHz band [2] and the 77GHz band [3]. Unfortunately microwave transmission-line based design techniques do not scale to relatively lower frequencies like 10GHz. Due to area constrains, circuits at these frequencies must employ relatively small lumped passive components, such as inductors ~ 250pH , and such small reactances must be realized on-chip. As we shall see, realization of such inductors is challenging due to parasitic inductance of the layout.

II. Design for Low Noise

A simplified small signal model for a simplified inductive degenerated cascode LNA is shown in Fig. 1. Ignoring C_{gd}, the input impedance Z_{in} is given by

$$Zin \cong \frac{1}{sC_{gs}} + s(L_s + L_g) + \frac{g_m L_s}{C_{gs}} + r_{L_g} \qquad (1)$$

By definition, the noise factor F is given by the total output noise normalized by the noise at the output arising only from the source, or

$$F \cong \frac{\overline{i^2_{o|_{R_s}}} + \overline{i^2_{o|_{r_g+r_s+r_i}}} + \overline{i^2_{o|_{Id^2_{M1}}}} + \overline{i^2_{o|_{Id^2_{M2}}}} + \overline{i^2_{o|_{R_L}}}}{\overline{i^2_{o|_{R_s}}}} \qquad (2)$$

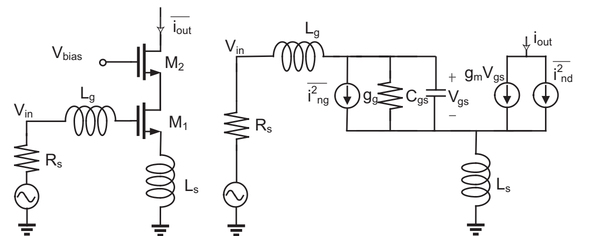

Fig. 1. (a) Simplified cascode LNA. (b) Small-signal model of (a) (M_2 is ignored for simplicity).

Which can be simplified to [4]

$$F \cong 1 + \frac{r_{Lg} + r_t}{R_s} + \Gamma\alpha g_{m_{M1}} R_s \left(1 + \frac{g_{m_{M2}}}{10 g_{m_{M1}}}\right)\left(\frac{f}{f_T}\right)^2 \qquad (3)$$

where $\Gamma = \frac{\gamma g_{d_0}}{\alpha g_m}$, $\alpha = 1 + \frac{g_{mb}}{g_m}$, $r_{Lg} = \frac{L_g \cdot \omega}{Q_{L_g}}$, R_L is the load resistance and $r_t = r_g + r_s + r_i$ accounts for total gate resistance including induced gate noise.

At a given frequency, given lossless feedback and matching networks, selection of the optimum device width and optimum bias voltage at each frequency results in an input match and an overall noise figure of F_{min}, the minimum noise figure of the circuit [5]. Unfortunately, practical inductors have finite quality factor, requiring a careful trade-off between the input match and the noise figure.

III. LNA Circuit Design

The simplified schematics of the single-stage cascode and two-stage cascade LNA's are shown in Fig. 2 and Fig. 3. Both topologies utilize inductive degeneration for input matching to 50Ω. Degeneration also improves the linearity by forming a negative series-series feedback. For the cascade two-stage design, the second stage also employs inductive degeneration to improve the linearity of the amplifier (rather than for matching). In Fig. 3, the output of first stage will resonate with the total capacitance connected to the drain of M_3. The advantage of using a single transistor for the first stage is to lower the overall noise contribution of the input stage. In single-stage LNA of Fig. 2, the impedance seen through the drain of M_1 without considering L_r and C_r could be modeled by R_p in parallel with C_p, as shown in Fig. 4. At high frequencies, the parasitic capacitance at the drain node of M_1 significantly reduces the overall impedance to ground and thus raises the noise contribution from cascode transistor

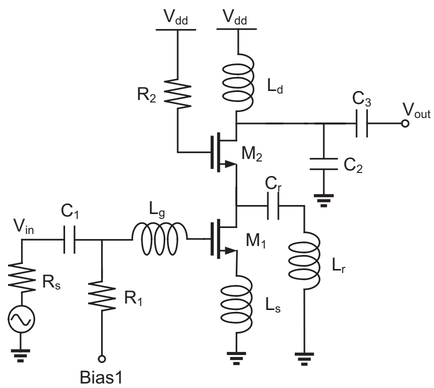

Fig. 2. Single-stage cascode LNA schematic.

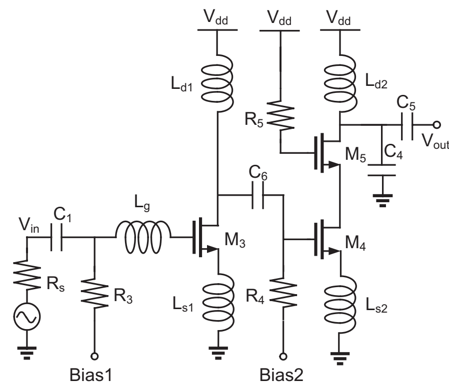

Fig. 3. Two-stage cascade LNA schematic.

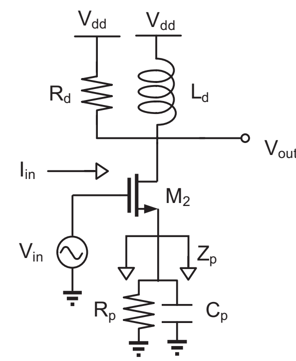

Fig. 4. Input impedance seen at the gate of the cascode transistor.

$$\overline{i^2_{o|M2}} \cong \frac{\overline{v^2_{nM2}} + \frac{\overline{i^2_{nM2}}}{g^2_{m2}}}{\left(\frac{1}{g_{m2}} + R_p \| \frac{1}{C_p s}\right)^2} \tag{4}$$

where $\overline{i^2_{o|M2}}$ is output current noise due to transistor M_2.

To improve the noise performance of the cascode design, the parasitic capacitance at the drain of M_1 is resonated out by adding an inductor to the source of casode. This improves the noise performance of the cascode considerably, as shown in Fig. 2. This inductor should be sized carefully in order to resonate the unwanted capacitances at the desired frequency of operation.

The size of the transistors are optimized for noise minimization at 11 GHz. To lower the noise figure, the transistors are biased very close to maximum f_T of process. The peak f_T of 52GHz is achieved at a certain gate bias voltage. At higher gate bias voltage, the f_T drops due to high field mobility degradation. For power efficiency, the transistor should be biased slightly before reaching this optimum f_T point. By backing off slightly from this point, the noise degradation is small but power saving is large.

Because the optimum noise resistance is not equal to 50Ω, the transistors are not matched exactly, but rather the matching is traded off for low noise figure. Due to the high frequency of operation, the degeneration inductance, used for matching is very small and this necessitates careful consideration of the loop return currents in the layout.

IV. Layout and Stability Issues

A. LNA Layout Consideration

In high frequency circuits, the most important effects tend to be the most difficult to simulate. For calculating the effective reactance of spiral inductors, we must consider the contribution of routing and ground/supply inductance. For instance, in the input matching network shown in Fig. 2 , the inductance from the source node of M_1 to the input voltage ground terminal contributes to the inductive degeneration. To capture this extra inductance, we must also include the effects of the currents flowing on the ground plane return path. A custom simulation tool ASITIC [6] was used to estimate these parasitic effects.

The layout of the transistors were optimized to achieve low noise at high frequency. To minimize the impact of transistor substrate resistance, a ringed substrate contact structure was placed as close as possible to the transistors. A multi-finger transistor layout is employed to decrease the gate resistance. This translates to higher f_{max} and lower device noise. Even though a double-gate contact lowers the gate resistance even further, this was not employed in this design.

B. LNA Stability Consideration

Stability is an important consideration in the design of amplifiers, especially at higher frequencies. One important node prone to oscillation at high frequencies is the gate of the cascode transistor. Since the input impedance of a capacitively degenerated device has a negative real part, a high Q parasitic inductance at the gate of cascode can form a Colpitts oscillator. If we ignore C_{gd}, the input resistance in Fig. 4 is given by

$$Z_{in} = \frac{1}{sC_{gs}} + Z_p\left(1 + g_m \frac{1}{sC_{gs}}\right) \tag{5}$$

The real part is given by

$$R_{in} \cong \frac{R_p}{(R_p C_p \omega)^2 + 1} - \frac{g_m R_p^2 C_p \omega^2 C_{gs}}{(R_p C_p C_{gs} \omega^2)^2 + (C_{gs}\omega)^2} \tag{6}$$

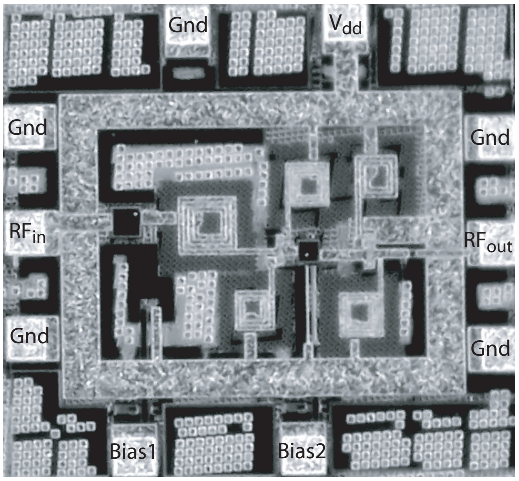

Fig. 5. Die photo of the two-stage LNA test chip.

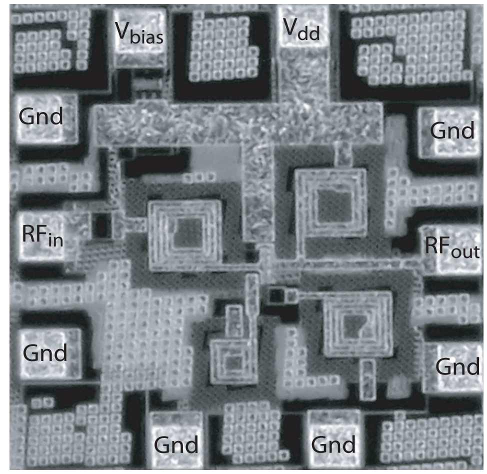

Fig. 6. Die photo of the single-stage LNA test chip.

where we have used

$$Z_p = \frac{R_p}{R_p C_p s + 1} \tag{7}$$

To improve the stability of the cascode amplifier, a resistor was added to the gate of cascode to de-Q the resonator. In this design, we estimated conservatively a parasitic gate inductance of 150 pH. A stabilizing resistor of value $R_{ex} = 10\Omega$ was added to the gate of the cascode transistor of LNA. The value of this resistor cannot be chosen arbitrarily large, as it degrades the noise figure and reduces the efficacy of the bypass capacitor.

V. Measurement Results

The two prototype LNAs were fabricated and measured. As shown in Fig. 2 and Fig. 3, the outputs are matched directly to 50Ω. Capacitors are implemented by Metal-Insulator-Metal (MIM) capacitors that provide good linearity and small parasitic capacitance. $C_2 - C_5$ are output matching capacitors, R_2 and R_5 are stabilizing resistors and C_r is a coupling capacitor for separating the series resonant tank at the source of M_2 at DC. The gates of the two-stage LNA are biased at 0.9V and the gate of single-stage LNA at 1.05V. The optimum width is selected ($\frac{57*2\mu}{180n}$), which is approximately the same for all the transistors. The inductor values for the two-stage LNA range from 300pH - 900pH. For the cascode LNA the inductor values range from 250pH - 1.11nH.

The test chips are fabricated using a $0.18\mu\text{m}$ CMOS technology. The die photos are shown in Fig. 5-6. The single-stage LNA occupies an area of $0.56 \times 0.58\,\text{mm}^2$ and the two-stage LNA occupies an area of $0.66 \times 0.72\,\text{mm}^2$ (including pads). The simulated and measured S-parameter data are shown in Fig. 7-9. The experimental results show that single-stage LNA has a peak gain of $8\,\text{dB}$ at 11GHz, and the two-stage LNA a peak gain of $12\,\text{dB}$ also at 11GHz. As expected, the S_{12} of two-stage LNA is more than $10\,\text{dB}$ better than single-stage LNA.

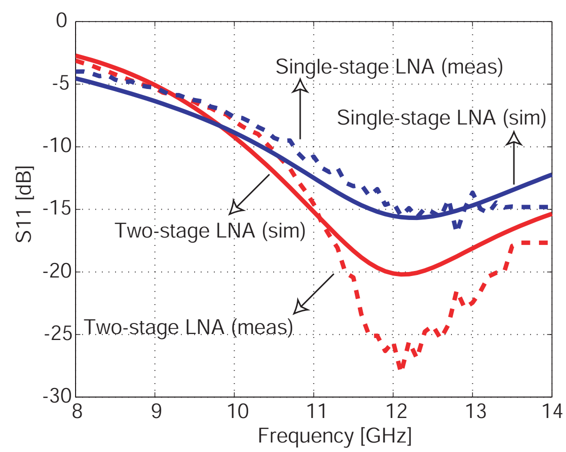

Fig. 7. Measured and simulated input match (s_{11}).

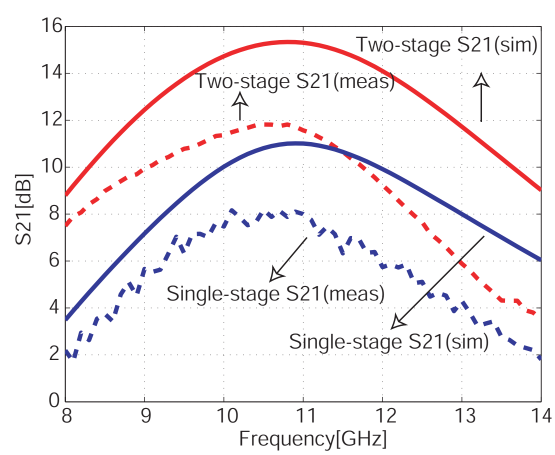

Fig. 8. Measured and simulated voltage gain (s_{21}).

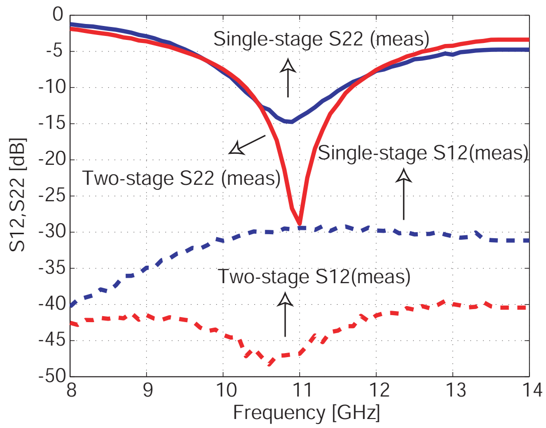

Fig. 9. Measured output match and isolation (s_{22},s_{12}).

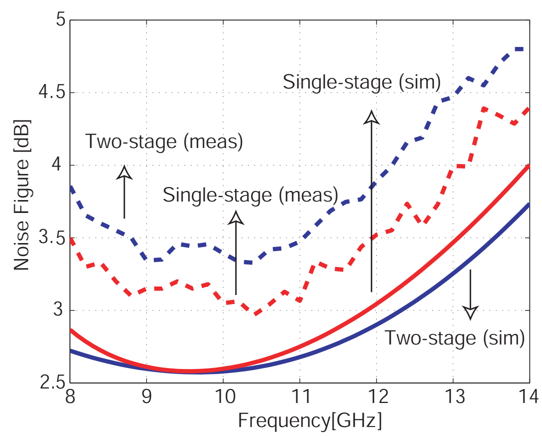

Fig. 10. Measured and simulated noise figure.

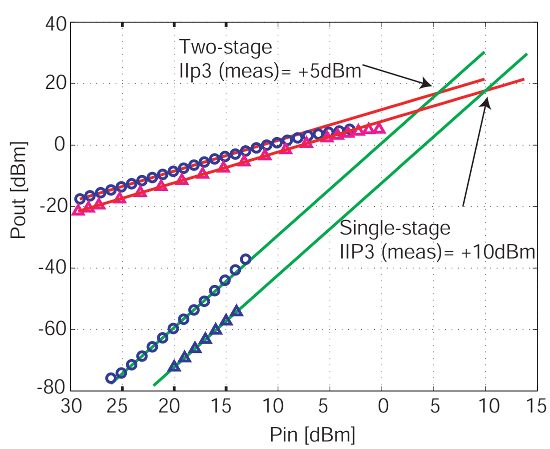

Fig. 11. Measured IIP_3 at 11GHz.

In Fig. 10 we plot the noise figure data of the two LNAs. Cable losses have been measured separately and de-embedded from the data. The minimum noise figure for both designs happen at around $10-11$GHz, at $3\,\mathrm{dB}$ for the single-stage design, and $3.3\,\mathrm{dB}$ for the two-stage LNA. Careful layout and passive modeling resulted in fairly close agreement between simulations and measurements, especially with regards to the center frequency. The absolute value of gain, though, is lower by about $3\,\mathrm{dB}$ compared to simulation. The pad loss or inaccurate transistor models could account for the difference, and the source of this error is currently under investigation. Model inaccuracy could also be accounted for difference between measured and simulated noise figure. The measured noise figure of the two-stage LNA is about $0.3\,\mathrm{dB}$ higher than the other design. The decrease in gain of the first stage in the two-stage LNA design could increase the noise contribution of the second stage and increase the overall noise figure.

A two-tone test for third-order intermodulation distortion is performed for the two LNAs with two signals around 11GHz separated by 10MHz from each other and is shown in Fig. 11. The IIP_3 is $+5\,\mathrm{dBm}$ and $+10\,\mathrm{dBm}$ and the input 1-dB compression point is measured at $-8.5\,\mathrm{dBm}$ and $-2.25\,\mathrm{dBm}$ for two-stage and single-stage LNA respectively. The single-stage LNA has better IIP_3 compared to two-stage design. The linearity of the LNA is important in sub-1dB low noise applications where the CMOS LNA will be preceded by an ultra-low noise preamplifier.

VI. Conclusion

Two different topologies for a X/Ku band CMOS LNA have been tested and compared. A series resonant tank was added to the source of cascode transistor in single-stage LNA to improve noise figure at high frequencies. The effects of layout on frequency tuning, noise, and stability have been addressed in the design.

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