

A 1.2V, 2.4GHz Fully Integrated Linear CMOS Power Amplifier with Efficiency Enhancement

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Abstract -- A 2.4GHz power amplifier is implemented with standard thin-oxide transistors in a 1.2V, 0.13 μm CMOS process. The output matching network is fully integrated on chip. The PA transmits up to 24dBm linear power with 25% drain efficiency at -1dB compression point. When driven into saturation, it transmits 27dBm peak power with 32% drain efficiency. A technique for enhancing average efficiency is proposed and demonstrated. This technique does not degrade instantaneous efficiency at peak power and maintains constant power gain with power back-off.

I. INTRODUCTION

There is a growing interest in utilizing CMOS technology for RF power amplifiers (PAs) [1]. This is driven by the desire for increased level of integration, since CMOS technology has been proven to be a cost-effective platform to integrate the digital base-band and RF front-end circuitry. Although several advances have been made recently to enable full integration of PAs in CMOS, it is still among the most difficult challenges in achieving a truly single-chip radio system in CMOS. This is exacerbated by supply voltage reduction due to CMOS technology scaling and on-chip passive losses due to the conductive substrate used in deep submicron CMOS processes.

It is well known that a PA can only achieve maximum efficiency at peak output power. As output power decreases, efficiency drops rapidly. However, the need to conserve battery power and to mitigate interference to other users necessitates the transmission of power levels well below the peak output power of the transmitter. As an example, the probability-density function (PDF) of a single carrier mobile transmitter is shown in Fig. 1 [2]. Moreover, since spectrum is a scarce commodity, modern transmitters for wireless communications employ spectrally efficient digital modulations with time varying envelope. Because of these reasons, the PA transmits much lower than peak output power under typical operating conditions.

To date, there has been relatively little research on the design of a CMOS PA targeting good average efficiency. This paper discusses a power control and average efficiency enhancement technique demonstrated with a fully integrated PA implemented in 0.13 μm CMOS technology.

II. TRANSFORMER BASED POWER COMBINING

Whether to use a number of smaller PAs versus a single bigger PA is one of the most important decisions in selection of architecture. Even when it is possible to design a single bigger PA, using a number of smaller PAs offers several advantages, such as better phase linearity, lower chip temperature, and less heat removal requirements. When the required output power cannot be achieved by a single transistor, power combining is necessary to generate the required power from several units. Various methods have been used to split and combine RF signals. Among those, transformers have been widely adopted as a means for splitting and combining RF power [3, 4]. For example, a circular-geometry distributive active transformer, known as DAT, functions as an eight-way power combiner with good efficiency at peak output power, implemented with 0.35 μm CMOS transistors [5].

Fig. 2 shows the conceptual diagram of the transformer based power combining amplifier prototype described in this paper. Unlike other power combining transformers, the topology used here provides great flexibility to access and control individual amplifiers. For instance, this is utilized to control output power and improve efficiency with power back-off as demonstrated in this work.

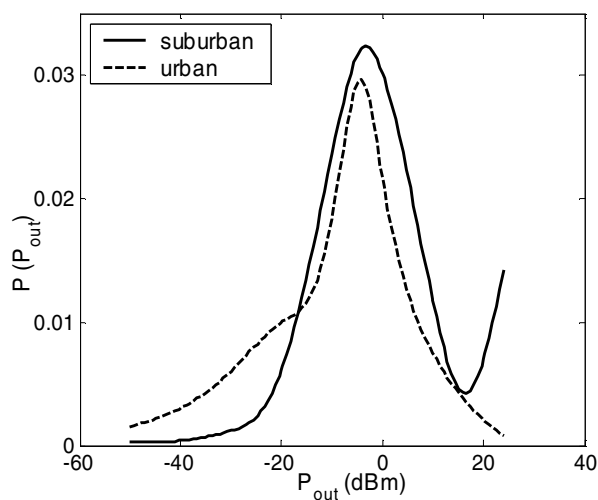


Fig. 1 – Output Power PDF of a single carrier mobile transmitter

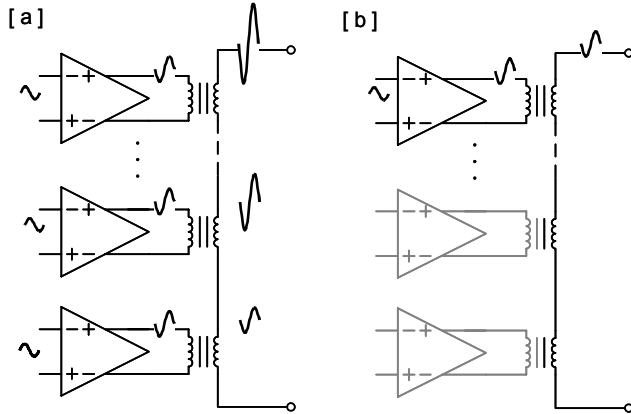


Fig. 2 – Conceptual diagram of the transformer based power combining amplifier: (a) peak power mode; (b) power back-off mode

III. POWER CONTROL AND EFFICIENCY ENHANCEMENT TECHNIQUE

Efficiency is a critical factor in PA design. Since peak power is rarely needed, PAs typically work at many dBs back-off. Thus improving average efficiency is at least as important as improving instantaneous efficiency at peak output power. Usually this is achieved by making systems adaptive, such as varying bias current, varying supply voltage, or varying load impedance. The Doherty Technique [6] is probably the most well known technique that varies effective load impedance as power back-off, requiring a quarter-wave transmission line (or lumped equivalent [7]) for functionality.

The power combiner used in this project naturally varies the load impedance seen by each amplifier as individual amplifiers turn on or off. When all of the N independent amplifiers are on, the impedance transformation ratio is N . Now if peak power is not needed, only M out of the N independent amplifiers need to be on and the rest are turned off, lowering the impedance transformation ratio to M . For example, in a four-way power combined amplifier, at peak power when every amplifier is on, a load resistor of $R_{LOAD}/4$ is presented to each amplifier. Suppose the power needed is lowered by 6-dB, so that only 2 amplifiers need to be on, and the other 2 amplifiers can be turned off. Now the load seen by each amplifier remaining on is increased to $R_{LOAD}/2$. This allows a full rail-to-rail output swing to be maintained for each independent amplifier that is on, to achieve optimum efficiency. Furthermore, the power gain remains constant as amplifiers are controlled. The simplified schematic of the prototype is shown in Fig. 3, in which 4 pseudo-differential amplifiers are combined.

IV. AMPLIFIER DESIGN CONSIDERATIONS

There are many challenges associated with power amplifier design. The most challenging part is in the output stage. Thus, a single-stage CMOS PA was designed with standard thin-gate-oxide transistors in a 0.13 μm CMOS technology.

This process offers two thick upper metal layers, 3- μm and 4- μm thick respectively. These are used to implement the integrated transformer. High density MIM capacitors are also available in this process. The substrate resistivity is very low.

A. Pseudo-Differential Pair

Single-ended topology should be avoided from the perspective of integration. Thus, a pseudo-differential pair serves as main building block for the power amplifier. This topology creates an ac virtual ground at the common source node and V_{DD} supply node for the fundamental frequency and odd-order harmonics, minimizing the impact of package parasitics on amplifier performance. Each side of the pair sees a load down-transformed by a factor of 2 without any loss. This is very important, since the on-chip matching network is usually lossy. Fig. 4 shows the detailed schematic of a pseudo-differential pair designed in this work.

B. Cascode

Cascode configuration is used to improve reliability. To avoid degradation of RF performance, only standard thin-gate-oxide devices are used. The transconductor device (m1) and the cascode device (m2) have the same size (2400/0.16), so that they could be laid out with a shared junction to minimize the parasitic capacitance at the cascode node. This helps to improve the efficiency of the amplifier. The cascode gate is connected to the supply node when the individual amplifier is on, and it is grounded to turn off the individual amplifier for power back-off.

C. Biasing

Class-AB biasing is chosen because both power efficiency and linearity are of prime concern in advanced wireless communication systems. In this work, the g_m of input devices is the major source of nonlinearity. It is known that when MOS devices are biased from weak inversion region to moderate and strong inversion region, g_m changes sign from positive to negative. Therefore, the input transistors are biased slightly beyond threshold to leverage this behavior. To reduce the inter-modulation products from the mixing products of inputs and even-order harmonics, a large on-chip bypass capacitor connects the center-tap of the transformer with the common source. This significantly reduces even-order harmonics, and prevents it from the contribution to the odd-order distortion.

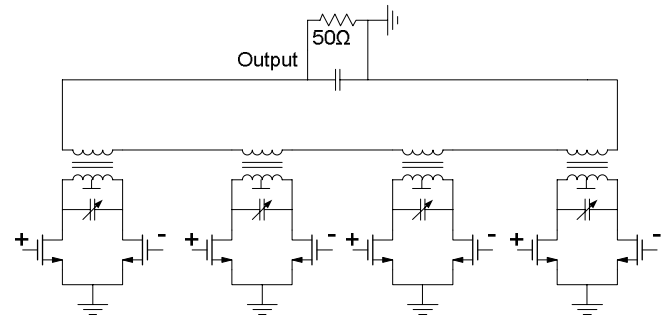


Fig. 3 -- Simplified schematic of the proposed PA

D. Transformer

The transformer used in this work plays two roles. First, it is used to down transform the 50Ω load. Second, it converts a differential signal into a single-ended signal so that it can be connected to the antenna directly. High efficiency of the transformer is the prerequisite in order to achieve high efficiency of the entire PA. High component Q and tight magnetic coupling are crucial to reduce the loss in the transformer. One-turn “hair pin” style inductors are implemented to construct the primary and the secondary coils of the transformer. To improve the magnetic coupling, an overlay structure is adopted wherein the secondary coil is put directly on top of the primary coils. The magnetic coupling factor k is ~ 0.7 with this structure. A metal shield (M1) is used to reduce capacitive coupling to the conductive substrate. The efficiency of the on-chip transformer is approximately 80%, simulated with ADS Momentum and HFSS.

V. EXPERIMENTAL RESULTS

A fully-integrated power combined amplifier was fabricated using a $0.13\ \mu\text{m}$ CMOS process to demonstrate the concept. It combines power generated from 4 independent amplifiers, whose inputs are connected together and driven in parallel. The chip area is $2\text{mm} \times 1\text{mm}$, including pads. A microphotograph of the prototype is shown in Fig. 5. The amplifier was tested with a 1.2V power supply. It drew 114mA DC current without RF signals applied.

During measurements, the chip was directly glued to the printed circuit board using conductive adhesives. All the pads, including input and output pads, were wire bonded on the board. No off-chip impedance matching elements are needed or used in this design. The input is driven by a commercial driver amplifier through an off-chip balun. Since the input is not matched, power gain is not known exactly. According to simulation, the power gain is 10 dB.

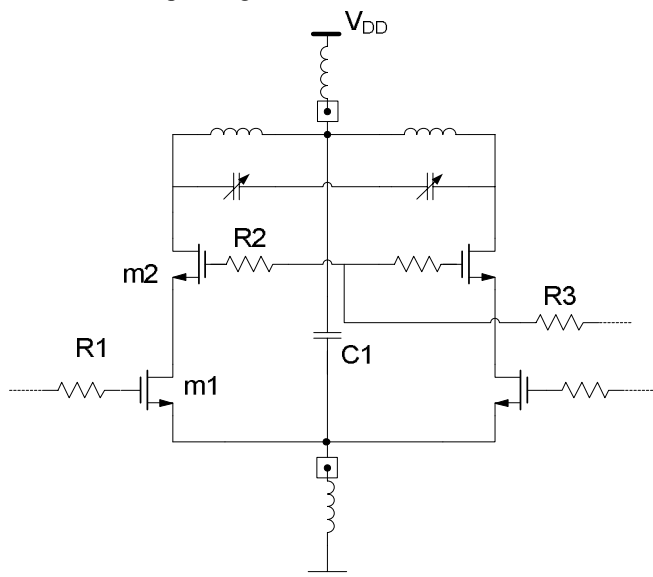


Fig. 4 – Detailed schematic of a pseudo-differential pair

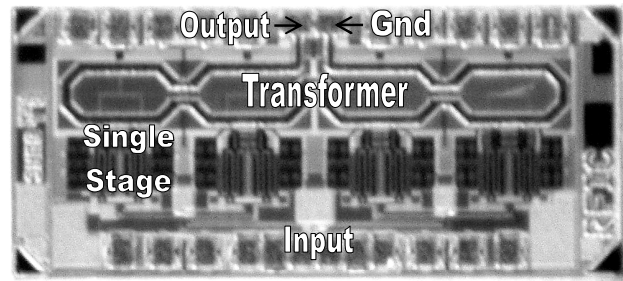


Fig. 5 – Die Microphotograph of the Prototype

The output was directly connected to a power meter with two 6-dB attenuators for power measurements. All system losses were calibrated out, while the measured results included losses on the board and bond wire losses. Output power and drain efficiency versus input power (read from the signal generator) for a single-tone test is shown in Fig. 6. The PA transmits up to 24dBm linear power with 25% drain efficiency, centered at 2.4-GHz. When driven into saturation, it delivers 27dBm power with 32% drain efficiency. Under the same bias conditions, a two-tone test was performed at 2.4GHz with 1kHz tone spacing. Little asymmetry was observed during testing. The results are shown in Fig. 7. When the average output power per tone is 18dBm, measured IM3, IM5 and IM7 are -29dBc, -36dBc and -42dBc respectively.

To verify the concept of the average efficiency enhancement technique, two PAs are compared. They use the same devices and the same power combining transformer, with the exception that one employs the efficiency enhancement circuitry. Fig. 8 shows the measured results which matches simulated results.

With 1.2V power supply, a peak power of 27dBm is measured with 32% drain efficiency, when all of four amplifiers are on. When output power is at 2.5dB back-off from peak power, in the PA employing efficiency enhancement circuitry, one amplifier is turned off and the other three remain on. The drain efficiency is measured as 31.5% at 24.5dBm, very close to the drain efficiency at peak output power. In contrast, drain efficiency is 5% lower in the conventional PA at 2.5dB back-off.

In fact, as shown in Fig. 9, further enhancements of efficiency in the back-off region can be obtained by turning off the remaining amplifiers sequentially, when output power is at 6-dB and 12-dB back-off.

VI. CONCLUSION

In this paper, a simple yet elegant technique was described to achieve high efficiency at peak power as well high average efficiency. A prototype was fabricated with only thin-gate-oxide transistors in a $0.13\ \mu\text{m}$ CMOS technology to demonstrate the concept. With 1.2V supply, it transmits linear

power up to 24dBm with 25% drain efficiency. When driven into saturation, it transmits 27dBm peak power with 32% drain efficiency. As one of the four amplifiers is turned off for 2.5dB power back-off from 27dBm, drain efficiency is improved from 26.5% to 31.5%, very close to instantaneous drain efficiency at peak power.

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REFERENCES

[1] K-C. Tsai, and P. Gray, "A 1.9GHz, 1-W CMOS Class-E power amplifier for wireless communications", *IEEE J. Solid-State Circuits*, vol. 34, no. 7, pp. 962-970, July 1999.

[2] F.H. Raab, P. Asbeck, S. Cripps, P.B. Kenington, Z.B. Popovic, N. Pothecary, J.F. Sevic, and N.O. Sokal, "Power Amplifiers and Transmitters for RF and Microwave", *IEEE Transactions on MTT*, vol. 50, no.3, pp. 814-826, March 2002.

[3] W. Simburger, H. -D. Wohlmut, P. Weger and A. Heinz, "A monolithic transformer coupled 5-W silicon power amplifier with 59% PAE at 0.9 GHz", *IEEE J. Solid-State Circuits*, vol. 34, no. 12, pp. 1881-1892, December 1999.

[4] T.S.D. Cheung, and J.R. Long, "A 21-26GHz SiGe bipolar power amplifier MMIC", *IEEE J. Solid-State Circuits*, vol. 40, no. 12, pp. 2583-2597, December 2005.

[5] I. Aoki, S. Kee, D. B. Rutledge and A. Hajimiri, "Fully integrated CMOS power amplifier design using the Distributive Active-Transformer architecture", *IEEE J. Solid-State Circuits*, vol. 37, no. 3, pp. 371-383, March 2002.

[6] W. H. Doherty, "A new high efficiency power amplifier for modulated waves", in *Proc. IRE*, vol. 24, pp. 1163-1182, September 1936.

[7] N. Wongkomet, L. Tee and P. Gray, "A 1.7GHz 1.5W CMOS RF Doherty Power Amplifier for Wireless Communications", *IEEE ISSCC Digest of Technical Papers*, pp. 486-487, February 2006

[8] D.R. Webster, G. Ataei, and D.G. Haigh, "Low Distortion MMIC Power Amplifier Using a New Form of Derivative Superposition", *IEEE Transactions on MTT*, vol. 49, no. 2, pp328-332, February 2001

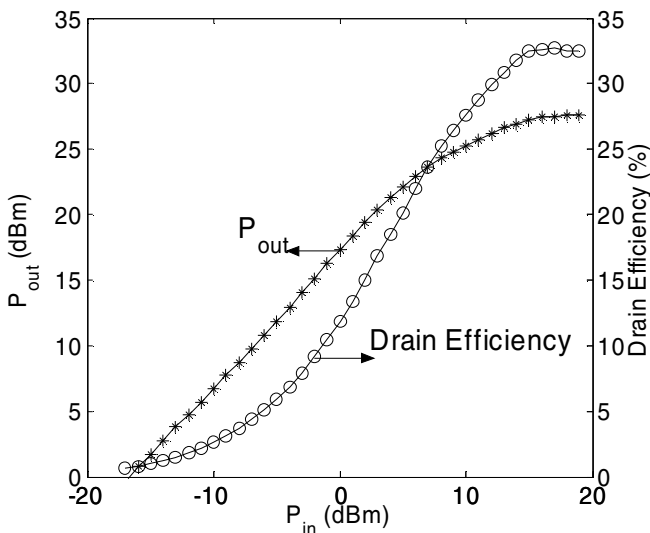


Fig. 6 – Measured output power and drain efficiency from single-tone test

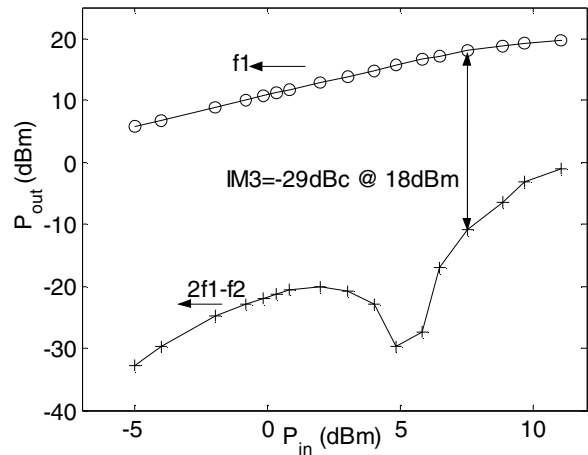


Fig. 7 – Measured output power and IM3 from a two-tone test with 1kHz tone spacing

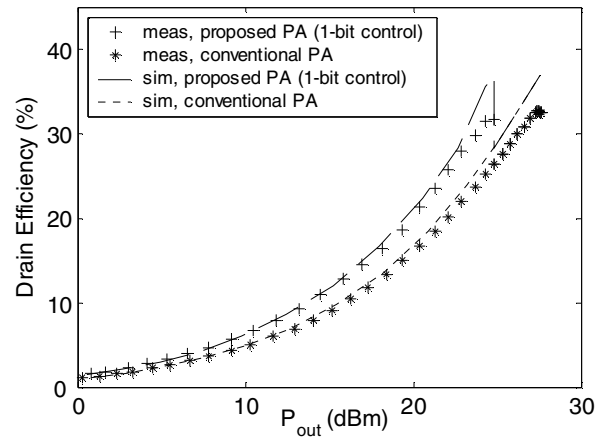


Fig. 8 – Simulated and measured drain efficiency of the proposed PA, in comparison with those for the conventional PA

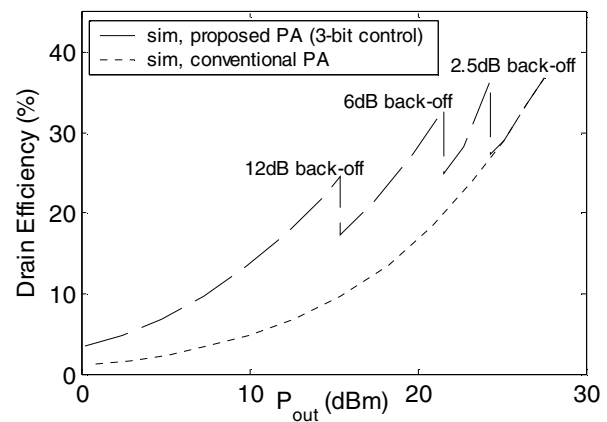


Fig. 9 – Simulated drain efficiency of the proposed PA with power back-off, in comparison with that for the conventional PA