

A 1.5MS/s 6-bits ADC with 0.5V supply

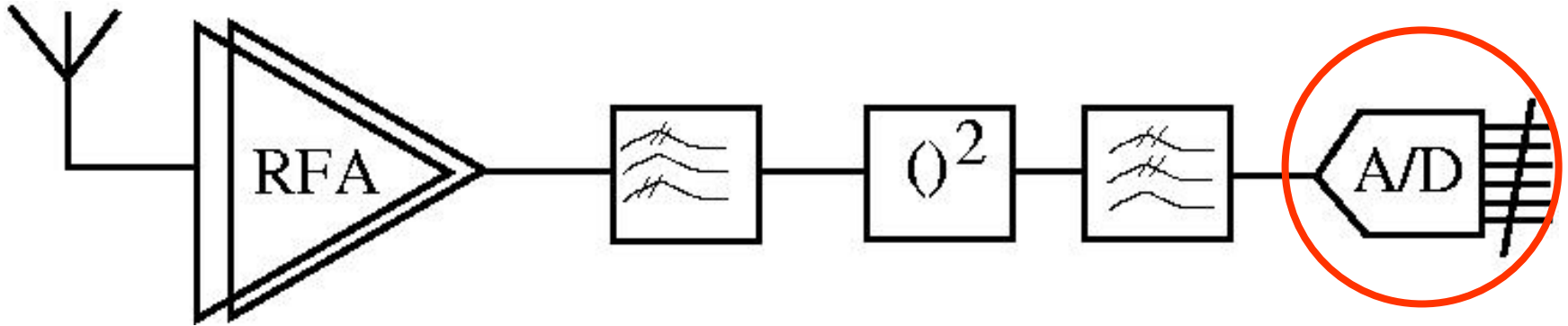
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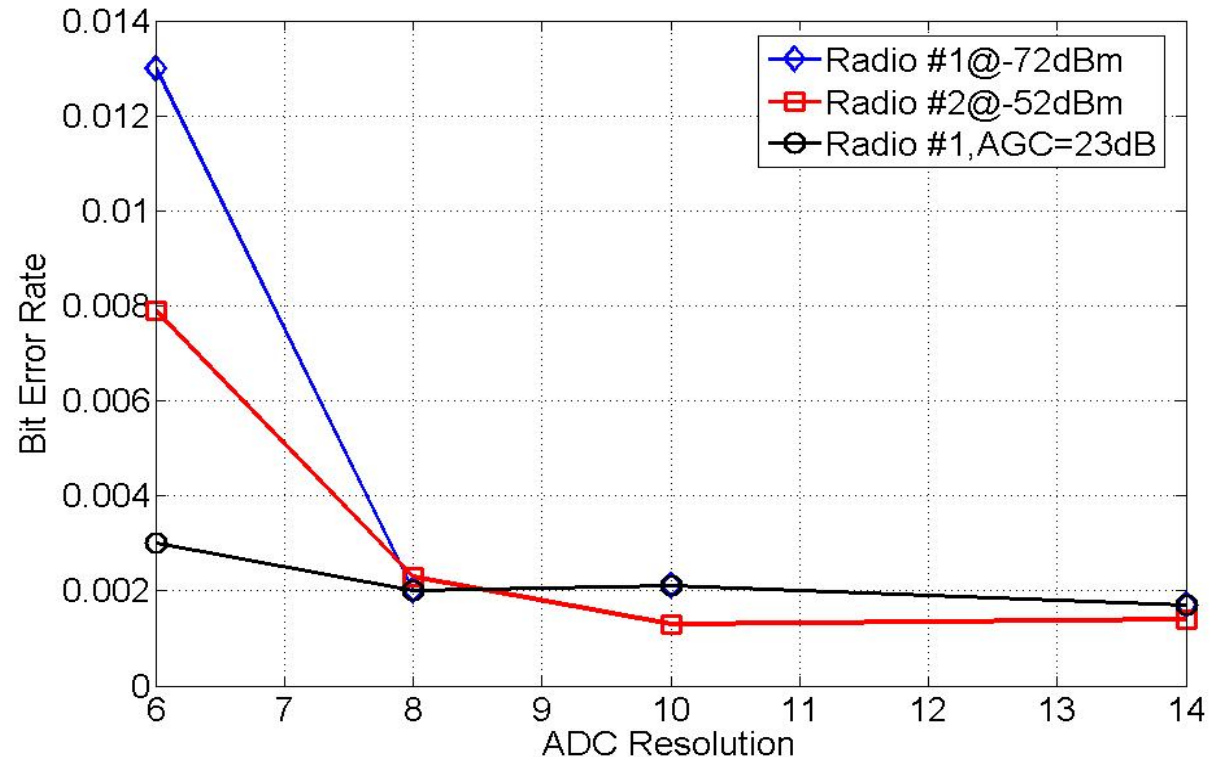
Paper Outline

- WSN Converter Specifications
- Charge Leakage issues
- Digital to Analog Converter Design
- Other Building Blocks
- Experimental Results
- Performance summary and comparison with literature

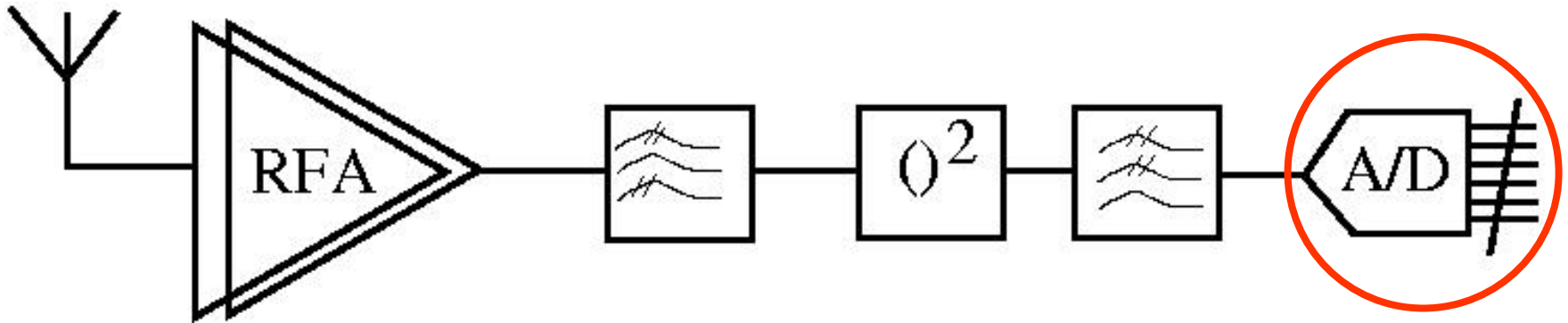
Wireless Sensor Radio



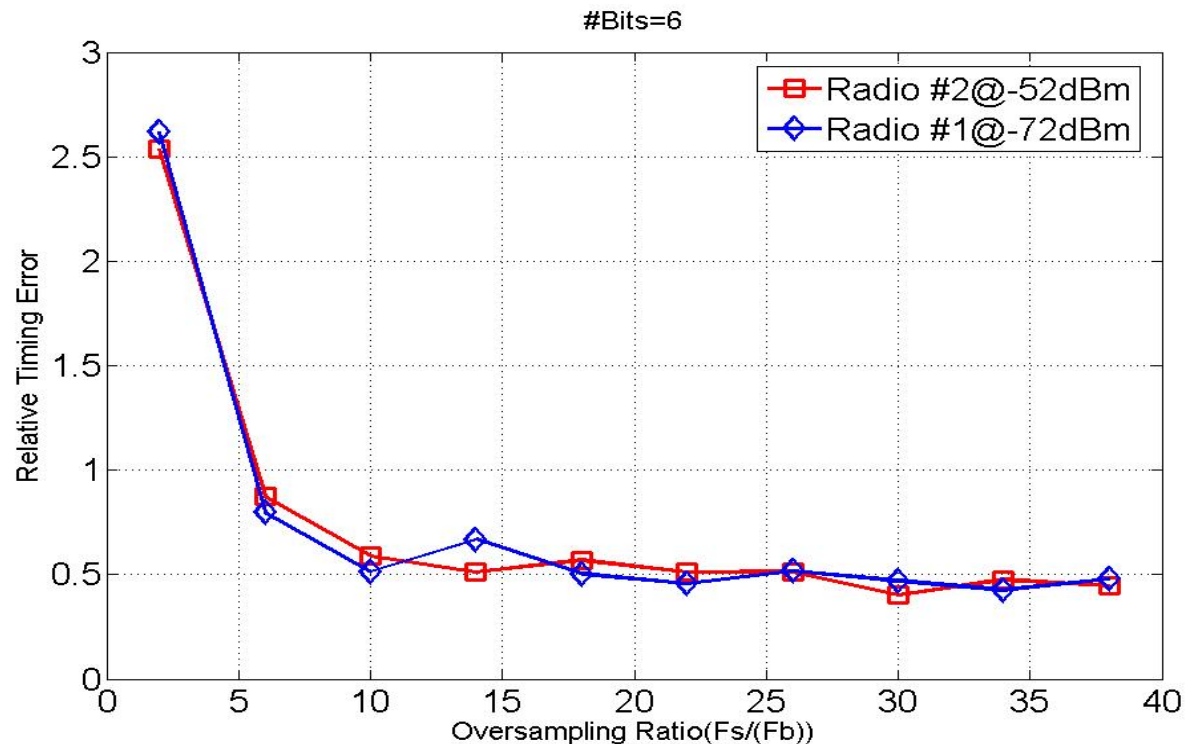
1. Aggressive front-end voltage scaling to reduce power
2. Envelope detection downconversion dominates receiver noise



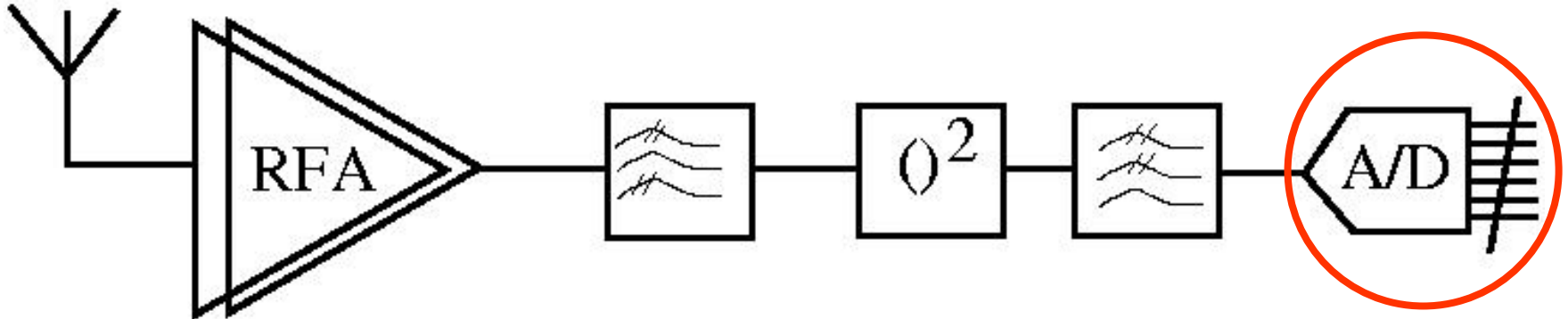
Wireless Sensor Radio



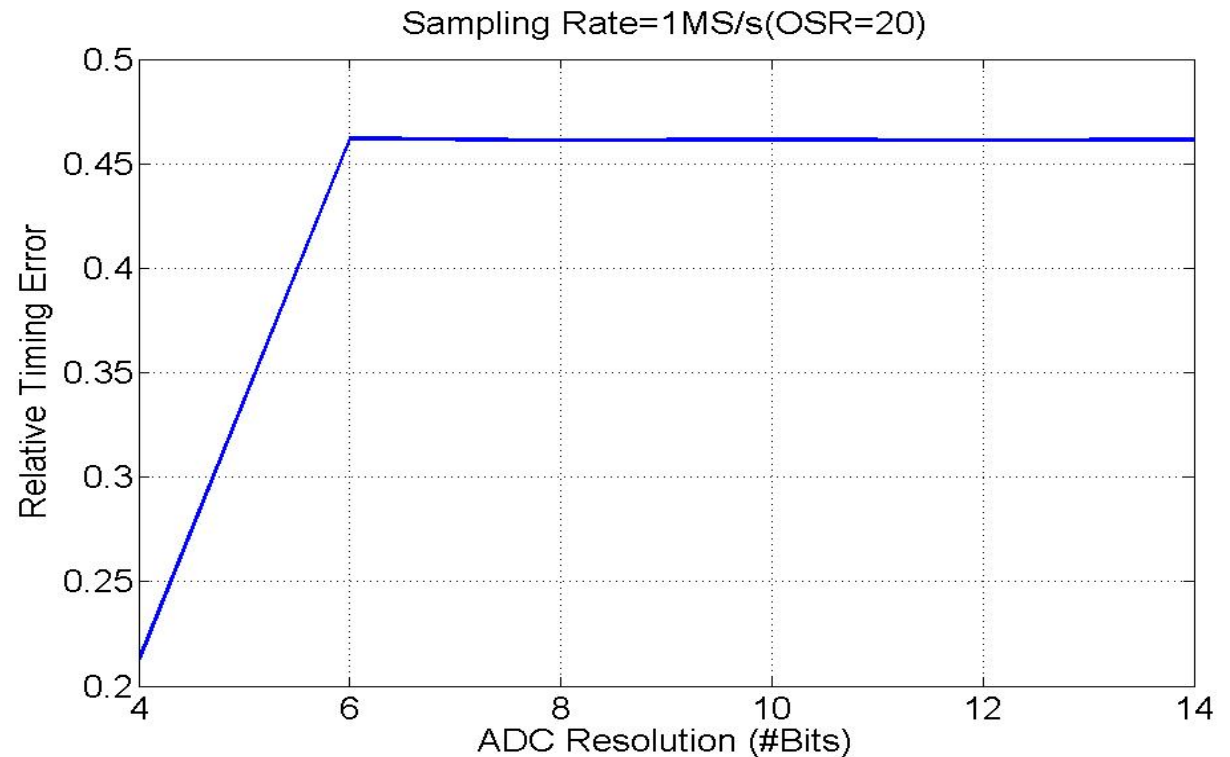
Performance requirements during timing acquisition



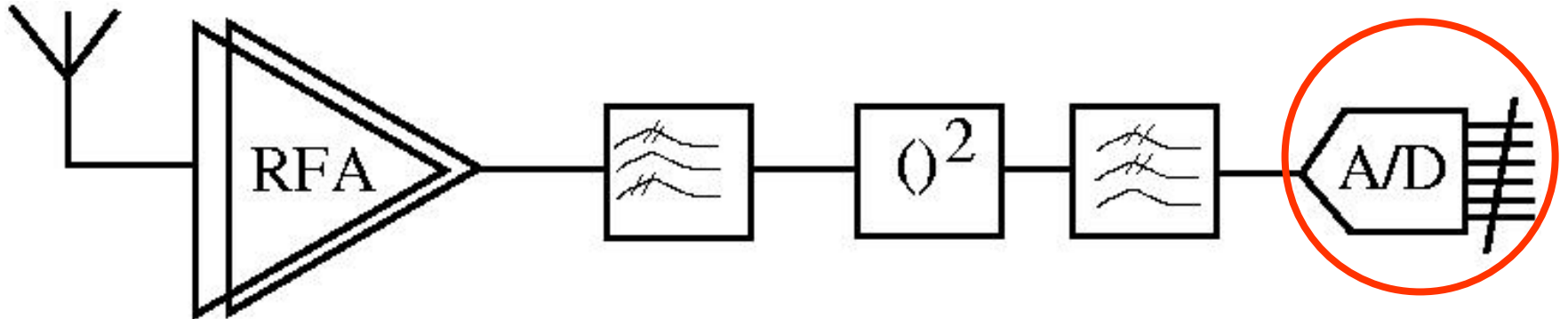
Wireless Sensor Radio



Performance requirements during timing acquisition



Converter Specifications



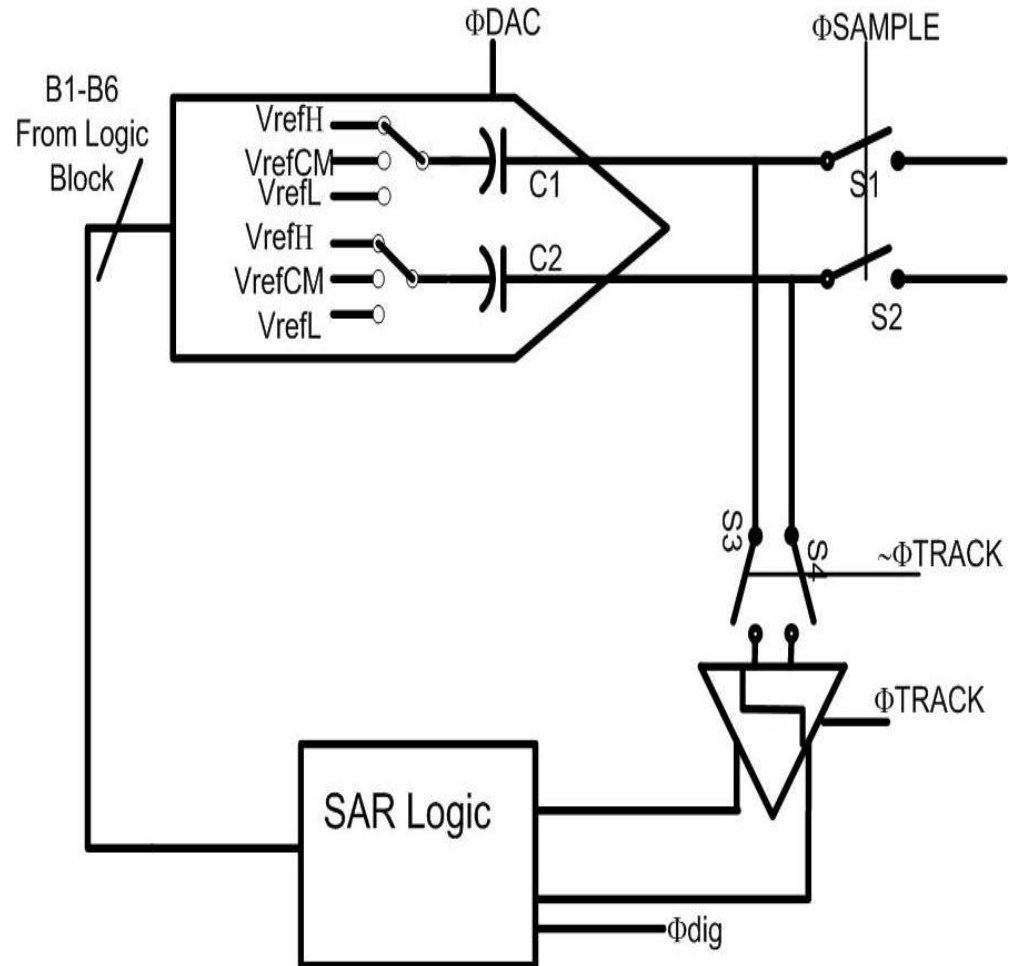
Quite different specifications from traditional ULP converter literature, mostly focused on data acquisition

Low Voltage operation most difficult

Resolution	6 bits
F_s	>.5 MS/s
V_{dd}	0.5V
P_d	<20 μ W
Input Cap.	Minimize

Successive Approximation Converter

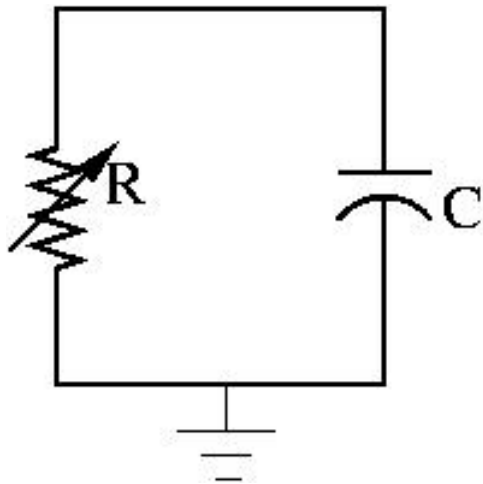
- Minimizes the number of precision analog components
- Design of comparators and digital not a problem down to .25V
- Sampling Switches reduced R_{off}/R_{on} ratio major bottleneck
- Tri-level unit-element DAC to minimize capacitance for given matching



Sampling Switch Leakage

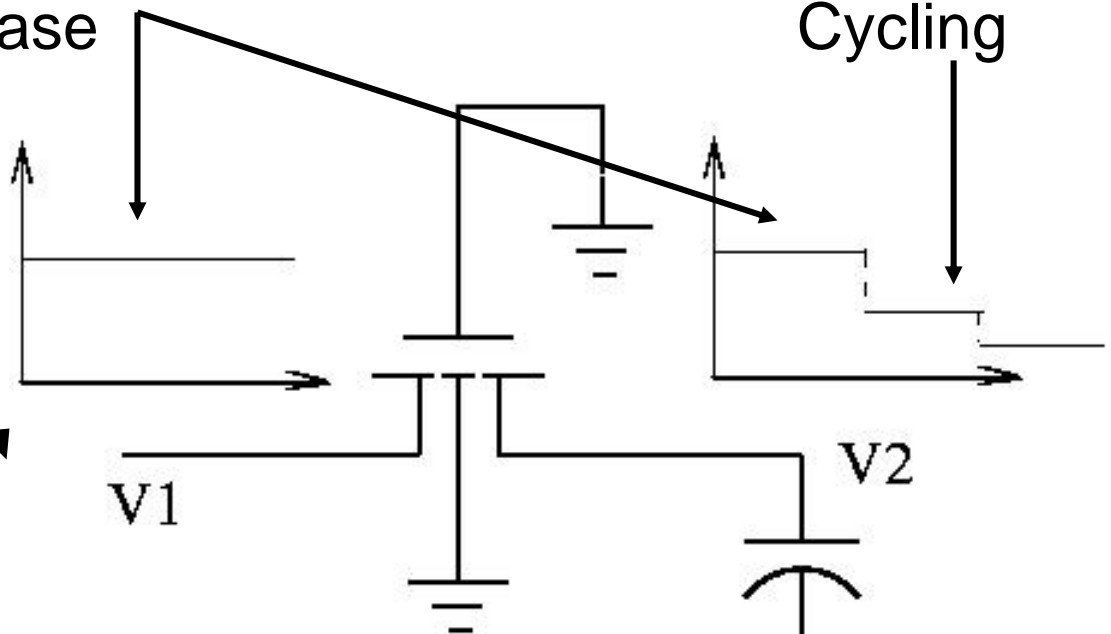
Switch off-resistance
small and code
dependent

DISTORTION



Tracking
Phase

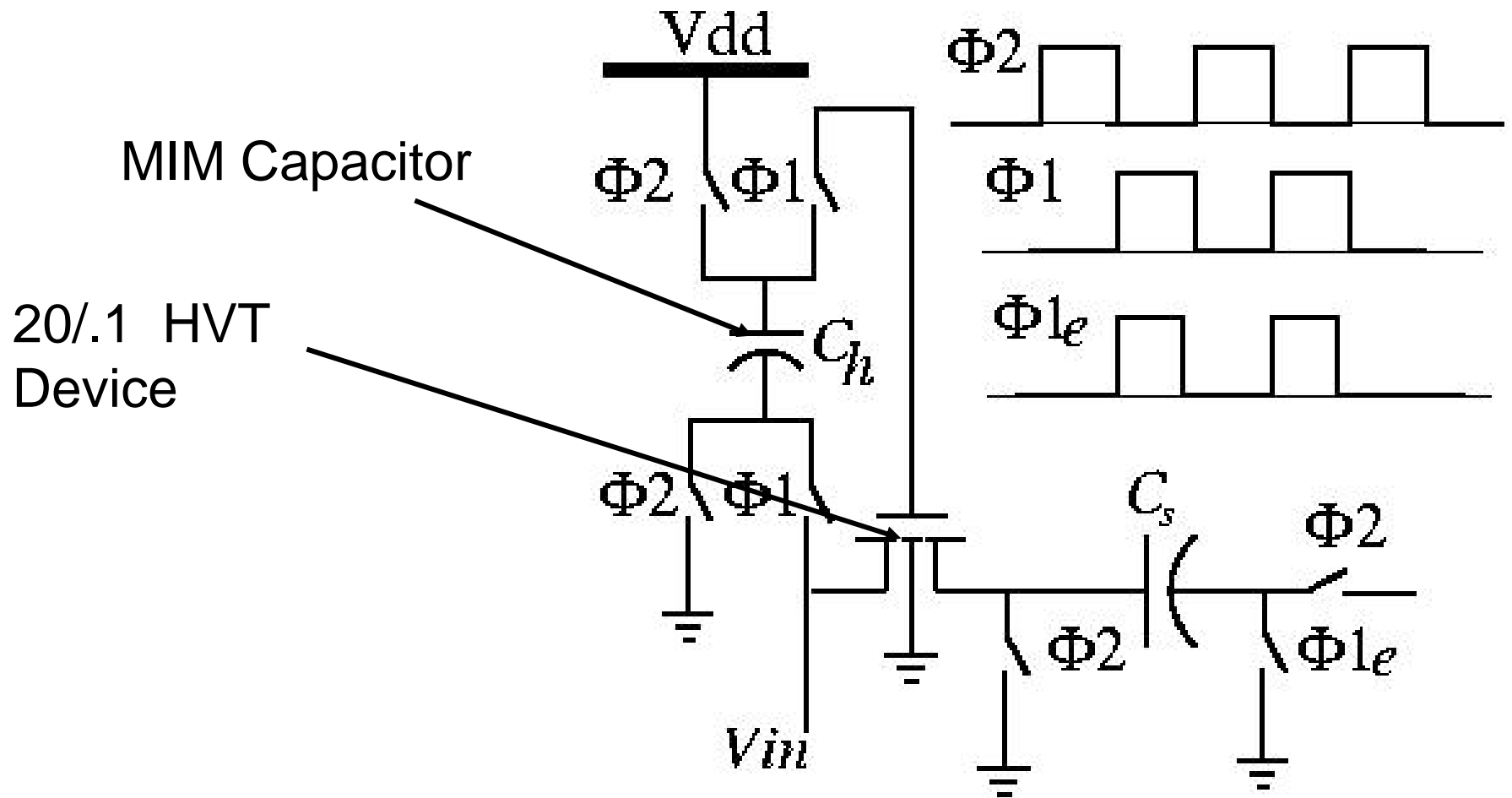
Bit
Cycling



Control Bits
From Logic

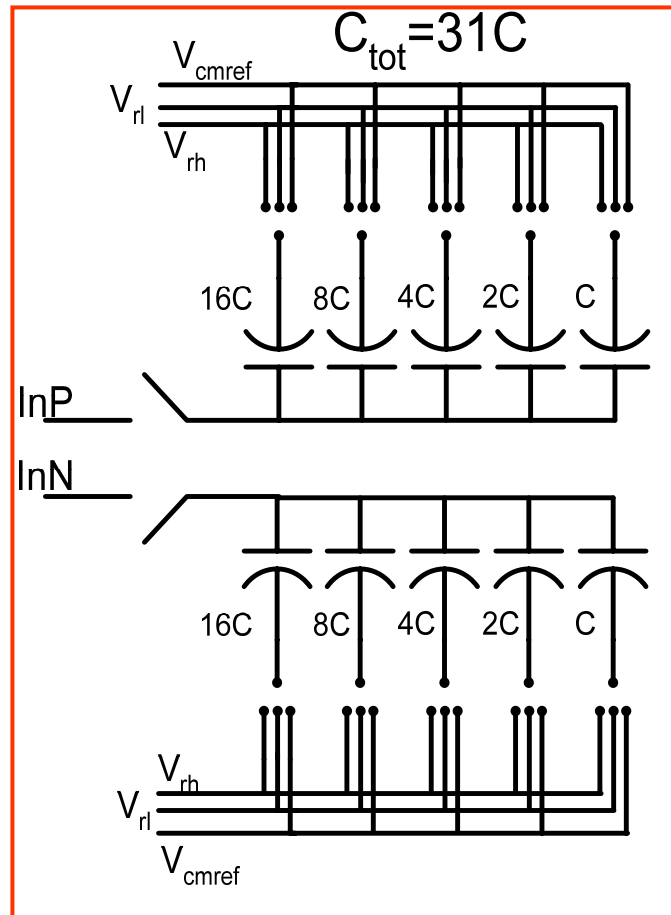
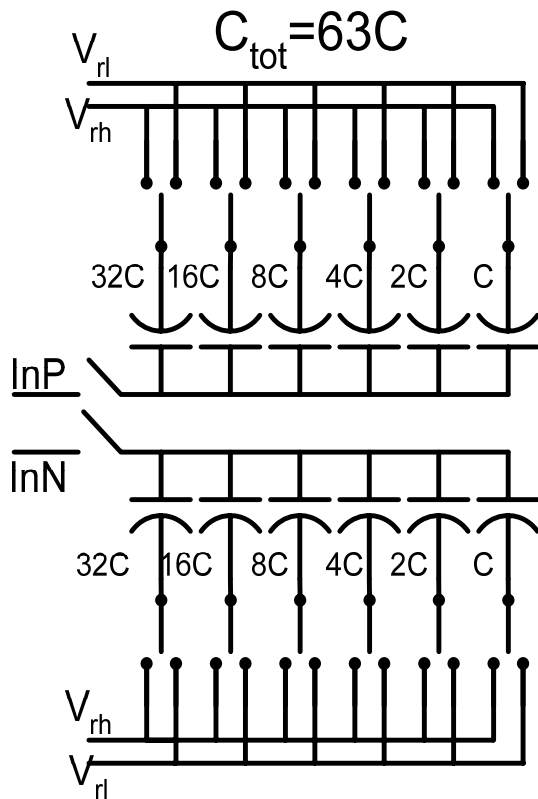
Sampling Switch Design

Solution: Bootstrapped Sampling [Abo] + HVT devices



DAC design

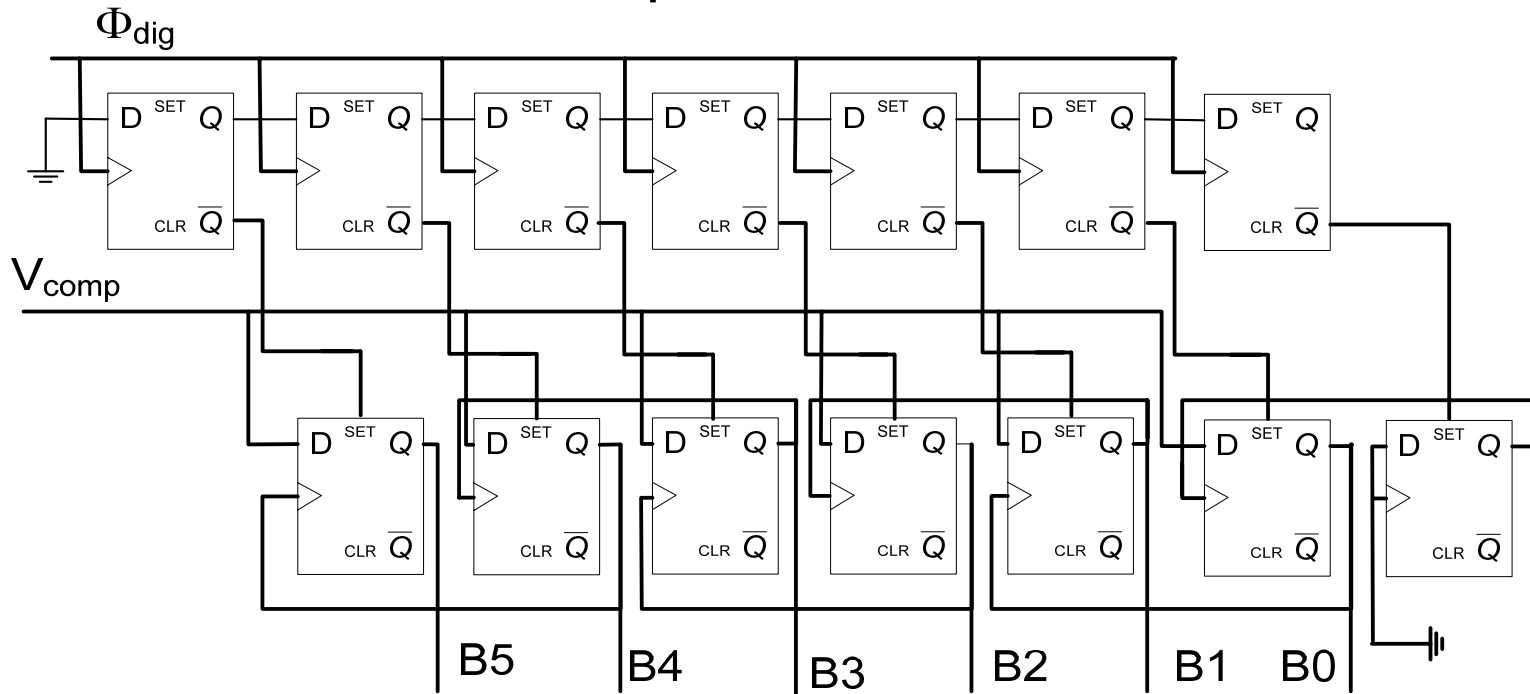
Goal: Minimize Input Capacitance/Satisfy linearity



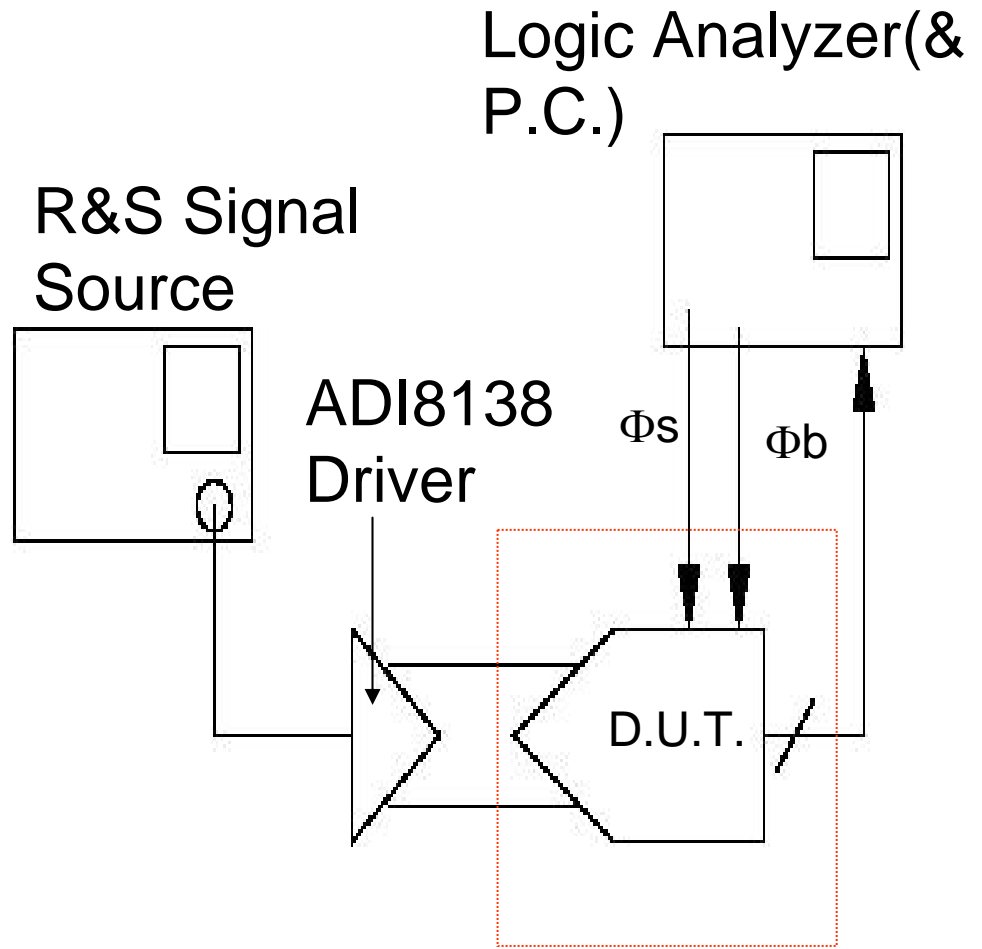
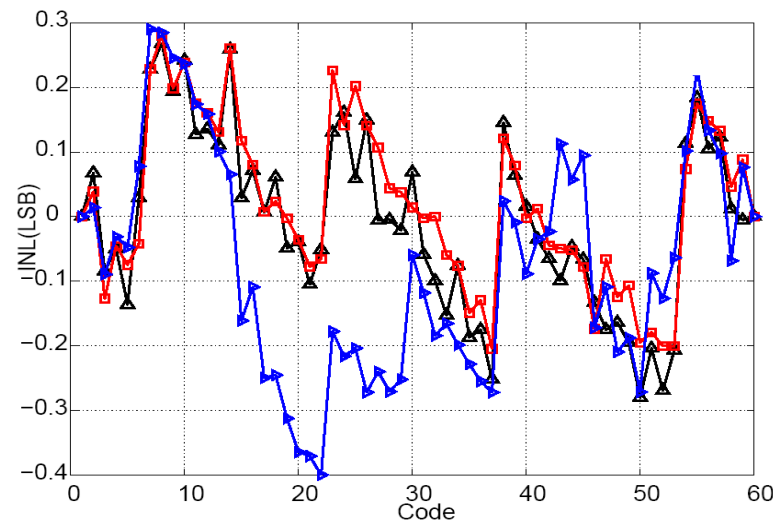
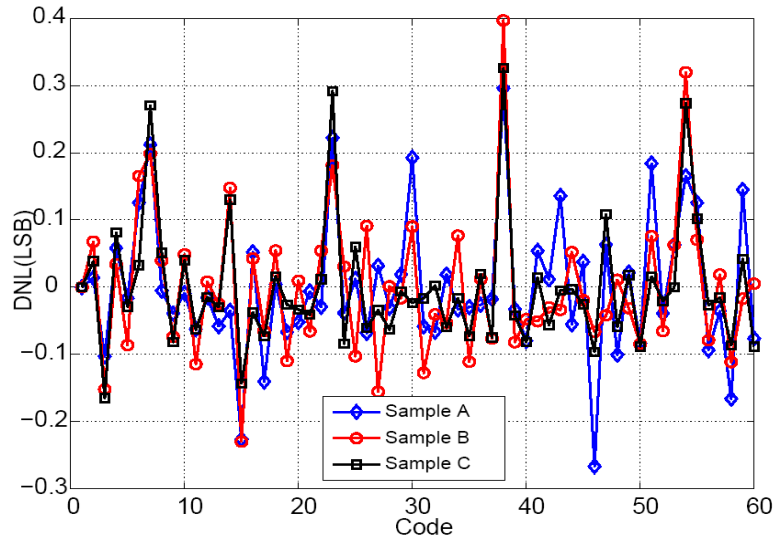
- Sign-Magnitude Coding
- Tri-level unit element (Trit)
- Low-density metal5-metal6 native caps
- 10fF Unit Capacitance \rightarrow 310fF total input cap

Digital Logic Design

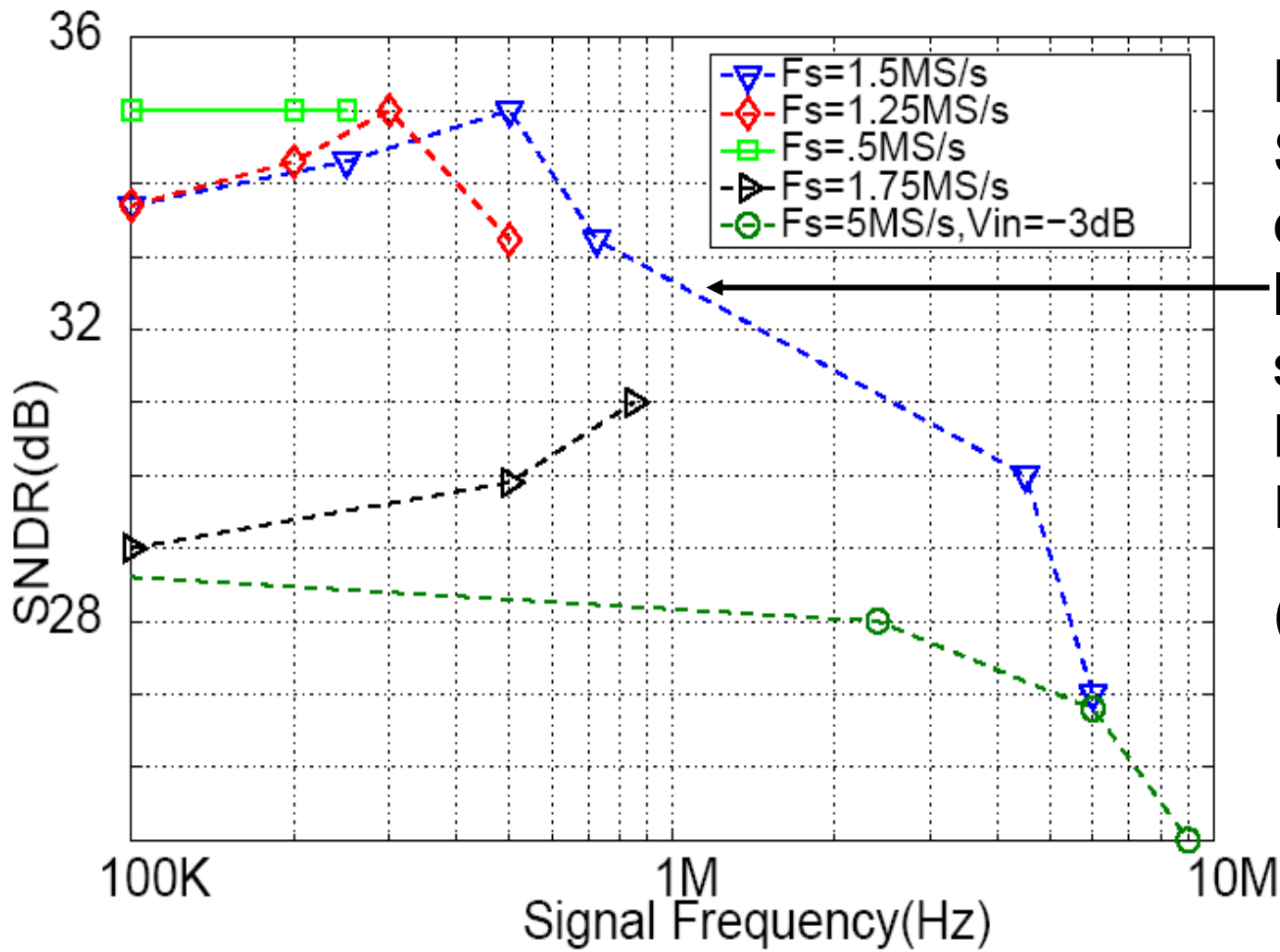
- Double Shift Register Approach After Scott, ESSCIRC 2002
- Redundant Flip Flops
- Non optimized Implementation using SVT Standard Cells
- Simulated Power Consumption $\sim 3\mu\text{W}$



Experimental Results

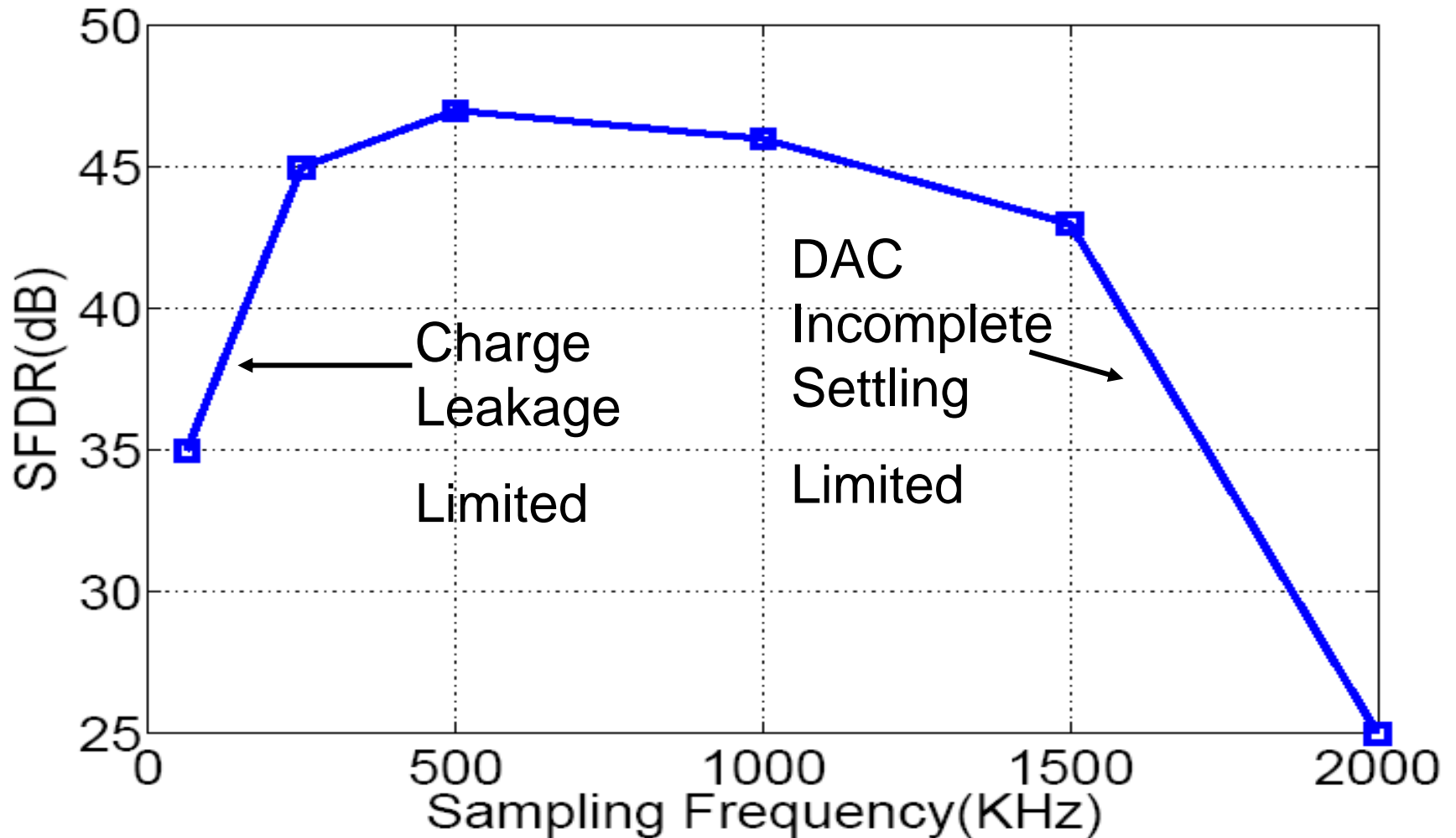


Experimental Results



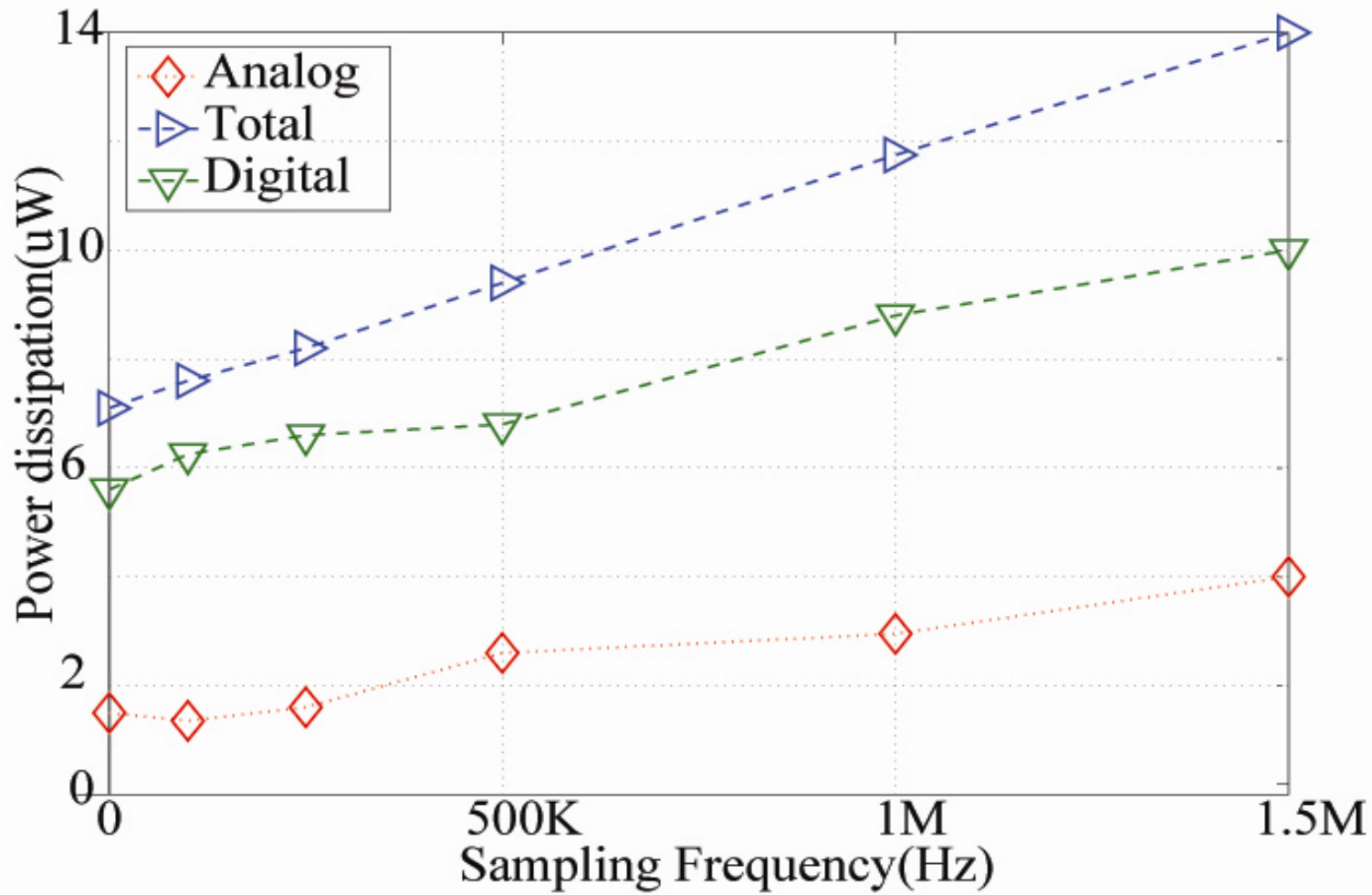
Bootstrapped Sampling enables high linearity sampling above Nyquist Frequency (Sub-sampling)

Experimental Results

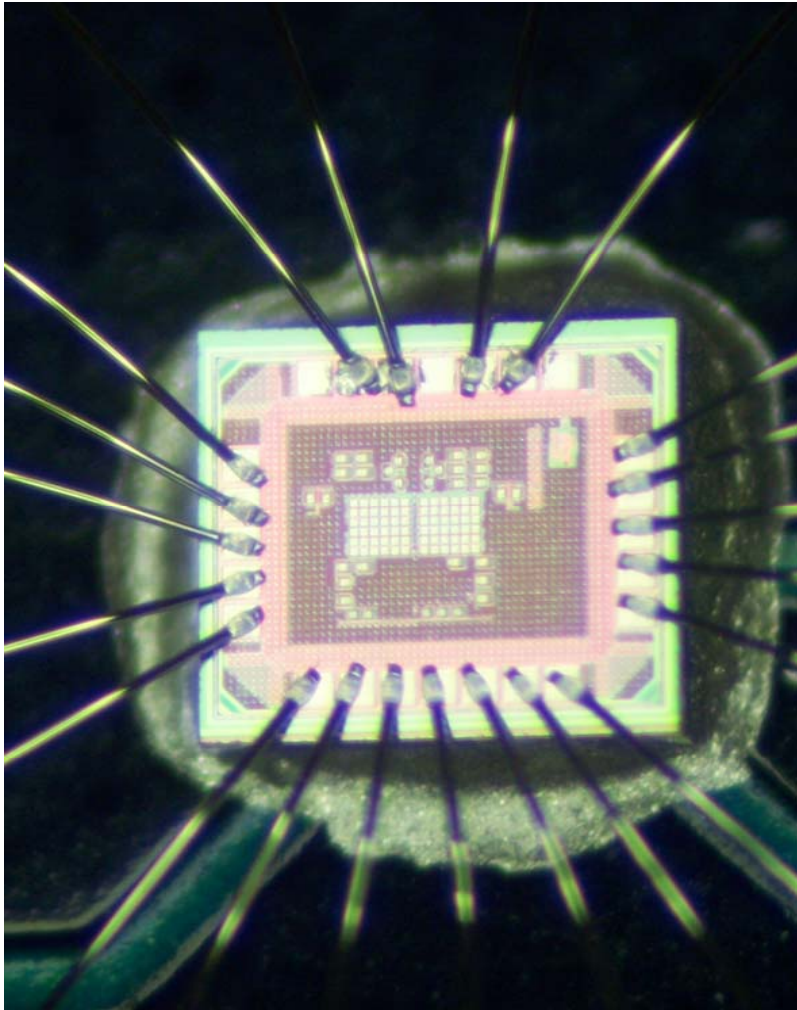


Experimental Results

- Very high leakage (11 μA), about 3x w.r.t. simulation
- Need to run fast to recover efficiency

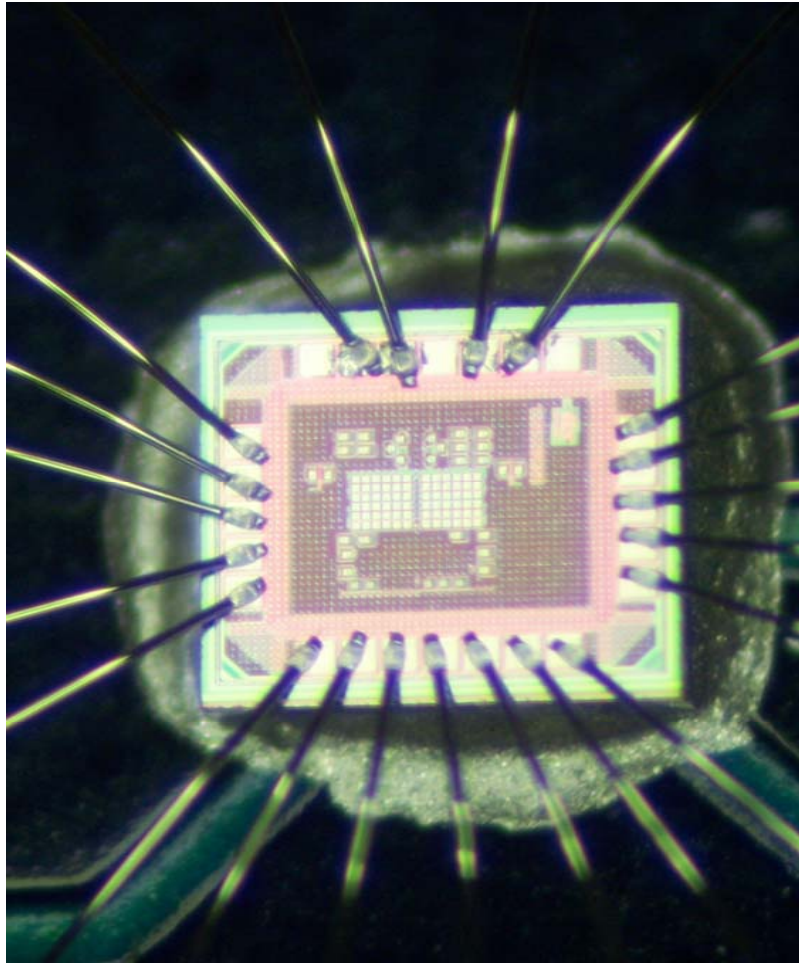


Performance Summary



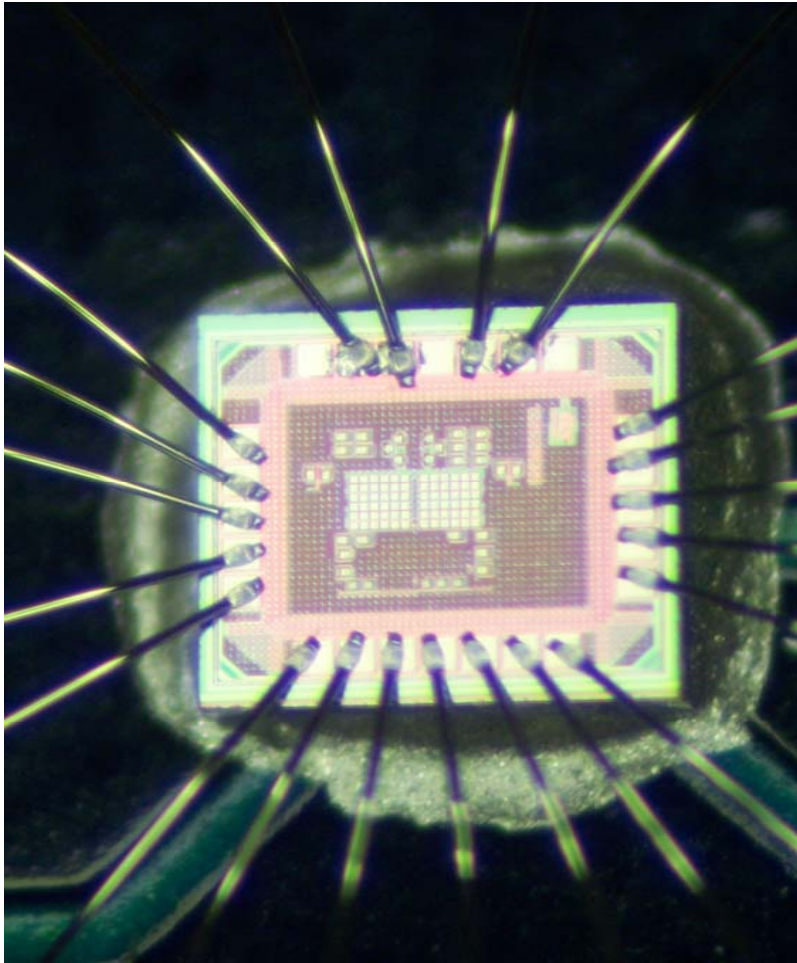
Process Tech.	90nm 7M2P w/MIM
Resolution	6bits
Sampling Frequency	1.5MS/s
SFDR	42dB
Peak SNDR @ Nyq.	35dB(5.5ENOB)
DNL	<.5LSB
INL	<.8LSB
Offset	<4LSBs
Power Dissipation	14uW
Input Capacitance (Sim.)	155fF diff.(310fF/side)
Typical Operating Voltage	.5V
Minimum Op.Voltage	.3V(Ana.)/.45V(Digital)
Active Die Area	340umX340um

Comparison with literature



	FOM(p J/conv .Step)	FOM (Pd/Fs/2 ^(2*ENO B))	FOM_SA R (Pd/Fs/E NOB)
Simpleton	.2	6.4e-15	1.7e-12
Scott ESSCIRC 2002	.23	1.28e-15	5.6-12
Verma ISSCC 2006	.16	9.5e-17	15e-12
Sauerbrey ESSCIRC 2002	.35	2.7e-15	11e-12

Conclusions



- First example of A/D converter specifically targeting WSN radio applications
- State of the art power efficiency, despite high digital leakage & reduced supply
- MHz Rate 0.5V conversion is possible in 90nm CMOS
- In fact, running slower than a few MHz is a problem in 90nm CMOS
- Power higher than expected due to model inaccuracy on leakage & non-optimized digital design

Any Questions?

Thanks to audience and committee

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