

Implementation Considerations for a Sub-sampling Impulse Radio

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Abstract—This paper describes the implementation issues of the proposed sub-sampling impulse radio architecture [1]. By using link budget analysis and system-level simulations with measured pulse and ambient noise, the system specifications of the critical blocks are provided. From circuit implementation perspective, the most challenging block is the high-speed analog-to-digital converter (ADC) which is required to sub-sample RF signals. A low-power, low-cost and fully-integrated CMOS prototype of a sub-sampling ADC has been developed to prove the feasibility of the proposed radio architecture. Finally, a system prototype built with discrete components is used to demonstrate a wireless link.

I. INTRODUCTION

This work is the continued development of the proposed UWB radio architecture [1]. The analytic signal processing in the digital domain has been used to fully exploit UWB signal characteristics as well as compensate the non-idealities of the analog front-end. The proposed system follows the concept of an impulse radio [2][3] rather than heterodyne transceiver, the most popular architecture in existing narrow-band systems. To date, most of the published UWB system solutions [4][5][6][7][8][9] have adopted a direct-conversion radio architecture, as shown in Fig. 1(a). A major challenge of this approach is that the overall complexity is on the order of present 802.11 systems which means a dramatic cost and power reduction from the current wireless solutions is unlikely. On the other hand, an impulse radio simply uses a pulser to drive the antenna, and radiates a passband pulse shaped by the response of the wideband antenna and any possible bandpass filter, as shown in Fig. 1(b). The hardware elimination of mixers and local oscillators for mixing and the reduced linearity requirement imply lower complexity implementations of a transmitter.

On the receiver side, the direct-conversion architecture utilizes two paths (I and Q) of local oscillator (LO), frequency synthesizer and mixer to down-convert the passband signal to baseband prior to the ADCs. According to the published literatures, these extra analog circuit blocks for frequency translation can contribute significant portion of the total power consumption. Alternatively, the frequency translation can be done in the sampling process, so called sub-sampling, as a part of ADC. The noise folding issue associated with sub-sampling is greatly reduced in UWB case [1]. This leads to only one receive path and dramatically reduce the component counts compared to direct-conversion architecture. The remaining analog blocks prior to ADC are amplifiers and bandpass filters.

The sampled data are processed by a digital matched filter in order to reach the matched filter bound for optimal detection [10]. The proposed system avoids wideband analog processing by adding more processing to the digital backend, which results in a more efficient solution.

In this paper, we will further explore the implementation aspects of the system. The remaining of the paper is organized as follows. Section II discusses the expected received SNR through link budget analysis. The system specifications and implementation issues of bandpass filtering, gain stages, sampling clock, sub-sampling mixer and ADC are analyzed. A circuit example of a sub-sampling ADC implemented in 0.13 μm CMOS is provided. Section III performs system level simulations to verify the implementation loss due to various circuit impairments. In the end, a discrete prototype is built to demonstrate the feasibility of the proposed transceiver in section IV.

II. IMPLEMENTATION SPECIFICATIONS AND ISSUES

A first-order link budget analysis including circuit implementation loss will be provided for the entire receiver chain up to ADC. The analytical approach is to treat each individual non-ideality as an independent and additive noise source. The circuit specification of each block should be made to minimize the implementation loss, defined as the gap between output and received SNR. The received and output SNR can be expressed as:

$$SNR_{received} = \frac{P_{signal}}{P_{ambient}} \quad (1)$$

$$SNR_{out} = \frac{P_{signal}}{P_{ambient} + P_{ckt} + P_{jitter} + P_{SH} + P_{adc}} \quad (2)$$

,where

P_{signal} : received signal power;

$P_{ambient}$: received ambient thermal noise plus interference power within communication band;

P_{ckt} : input-referred thermal noise power caused by amplifiers and filters;

P_{jitter} : input-referred clock jitter induced sampling noise;

P_{SH} : input-referred sample and hold (subsampling mixer) noise;

P_{adc} : input-referred quantization noise power of ADC.

The following analysis is based on transmitting a 1GHz UWB pulse centered at 3.5 GHz with a sampling rate of 2 Gsa/s. However, one may easily apply this analytical approach



Fig. 1. Radio architecture comparisons.

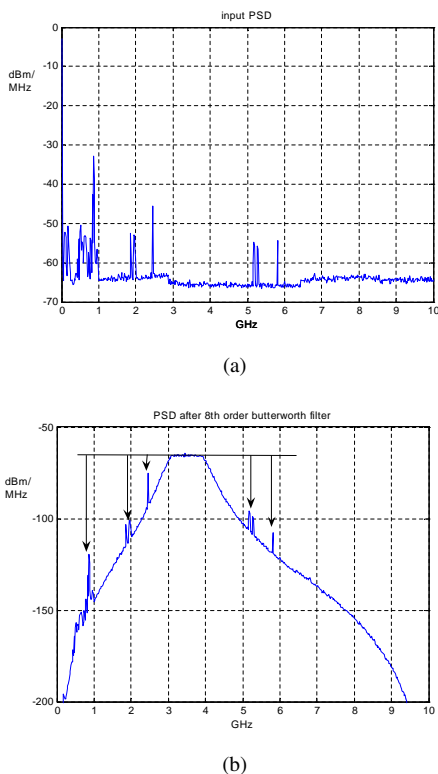


Fig. 2. (a) Measured noise and interference using TEM horn antenna; (b) Spectrum after 8th order Butterworth bandpass filter.

to a different communication band and sampling frequency as long as there is no signal aliasing. Later, we will include these realistic circuit impairments into system-level simulations using measured noise and interference samples.

A. Received SNR

According to FCC regulation [11], the transmission power spectral density is under -41 dBm/MHz. Given a 1 GHz wide signal bandwidth, the maximum transmission power is -11 dBm. However, the received power is attenuated through the wireless channel. According to our S21 measurements using spiral and elliptical wideband antennas [12] as well as literature reports [13][14], the path loss can be 40 to 60 dB from 1 to 10 meters between transmitter and receiver. Therefore, the expected received signal power in the following analysis is within -51 to -71 dBm range.

The ambient noise level is strongly coupled with the operation environment. Figure 2(a) shows a noise spectrum measured by TEM horn antenna and spectrum analyzer (HP 8563E) in the lab of Berkeley Wireless Research Center

(BWRC), USA. The measured data was recorded one whole day with maximum and hold, which represents the worst-case scenario. Most of the interference comes from <1 GHz, the 1.9 GHz PCS band, and the 2.4 GHz ISM band. Note that due to the popularity of WiFi systems, we also measured interference from the 5 GHz UNI band. From the measurement results, received interference power can vary from -50 to -30 dBm. The received thermal noise power under a power matched front-end is -174 dBm/Hz [15]. For 1 GHz bandwidth and ideal bandpass filtering, the total thermal noise power is -84 dBm, which sets the minimum bound on noise level.

B. Bandpass Filter Response

The aggregate receiver response, including antenna, matching network, amplifiers and filters, requires a bandpass response for image rejection and channel selection if a multi-band operation is desired. Due to the wideband nature (low Q) of UWB, the requirement of bandpass filtering is largely relaxed as opposed to narrowband system. From thermal noise perspective, the undersampling ratio (less than 10) determines the required stop band attenuation in order to suppress the aliased out-of-band thermal noise well below in-band noise level. Nevertheless, the real requirement of stop band attenuation depends on out-of-band interferers in Fig. 2(a). The unfiltered out-of-band interference will alias back to the signal band and corrupt the SNR. The proposed bandpass response attenuates any out-of-band interference at least 10 dB below in-band thermal noise level. Shown in Fig. 2(b), an 8th order Butterworth bandpass filter between 3 to 4 GHz meets the requirement. Note that one may relax the order of bandpass response if additional notch filter is used to block high interference band.

C. Gain

Sufficient gain is required to amplify the input received level to the full swing of the ADC in order to fully utilize its dynamic range. On the other hand, the gain should be limited to avoid saturating front end. Saturation of receiver will cause large distortion as well as enhancing noise power. Not only is it difficult to perform good matched filtering in the digital domain, but we also lose the ability to reject in-band interference by any digital signal processing technique. As described in section 5.1, the input received power is within -51 dBm to -71 dBm. Given a measured 3-4 GHz UWB pulse, the peak signal level varies from 100 's μ V to a couple mV, assuming there is no further duty cycling. According to FCC's regulation, one may increase the pulse energy by lowering

pulse repetition rate up to 20 dB. If a system adopts duty cycling, one should further reduce receiver gain.

On the noise side, considering 1 GHz thermal noise (-84 dBm) plus 20 dB margin for noise figure of receiver front-end, aliased noise power and insertion loss of matching network, the standard deviation is about 200 μ V on 50 ohm input impedance. Since the signal and noise are independent, the total received signal variance is the summation of the two. For the pulse shape we measured, the total received signal standard deviation is around 1mV. Using three-sigma rule, the input-referred single-ended swing is about 3 mV for 0.3% probability of saturation. As the supply voltage of CMOS process keeps scaling down, the input full swing of ADC is reduced to the order of 100's mV, especially for high-speed operation. This implies the gain should not exceed 40 dB. Note that this analysis does not consider AGC loop in order to reduce the receiver complexity. Regarding wideband amplifier implementations, there are several published 3-10 GHz low noise amplifiers (LNAs) [15][16][17] that achieve about 10 dB gain consuming \sim 10 mW.

D. Sampling Clock

The only oscillator required in the sub-sampling front-end is the sampling clock. The two most important specifications of clocking are precision and jitter. The sampling offset will rotate the analytic matched filter output, which in turn limits the number of pulses that can be used for pulse shape estimation. The proposed specification on clock precision constrains the sampling offset to at most 1% of the sampling period during the channel estimation phase, which is about a 6 degree rotation. For example, a 10 ppm, 100 MHz oscillator can tolerate about 50 pulses for channel estimation, calculated by the following equation:

$$\frac{1}{f_{osc}} \cdot \frac{P_{off}}{10^6} \cdot \frac{\# \text{ cycles}}{\text{pulse}} \cdot \# \text{ pulses} \leq T_s \cdot 1\% \quad (3)$$

,where

f_{osc} : oscillator frequency;

P_{off} : clock frequency offset measured in part per million (ppm);

cycles/pulse: number of oscillator cycles within a pulse repetition period;

pulses: number of pulses required for channel estimation.

Another critical specification of the clock is jitter, especially for a subsampling receiver. In a traditional worst-case jitter analysis, the clock is assumed to sample at the sharpest edge. Jitter is constrained such that it contributes negligible noise compared to one LSB of ADC. For example, a 4-bit ADC sampling 5-GHz sine wave requires jitter less than 4 picoseconds. However, for a UWB signal, the energy is distributed over a wide frequency band. Thus, a worst-case analysis is too pessimistic. A noise modeling considering the input signal spectrum is more appropriate [16].

$$P_{jitter} = \int_{-\infty}^{\infty} |S(j\omega)|^2 \cdot (1 - e^{-\frac{\omega^2 \sigma_j^2}{2}}) d\omega \quad (4)$$

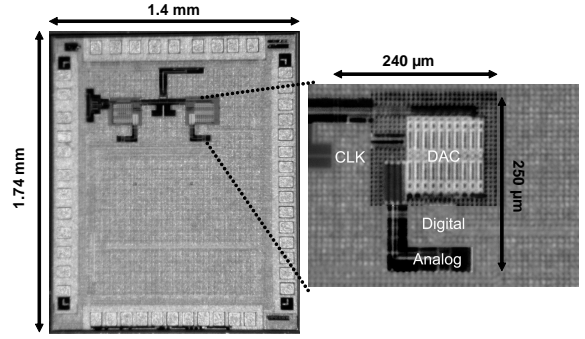


Fig. 3. Die micrograph of the asynchronous ADC prototype.

, where P_{jitter} is the equivalent noise power due to clock jitter, $S(j\omega)$ is the signal spectrum and σ_j is the RMS jitter of the clock source.

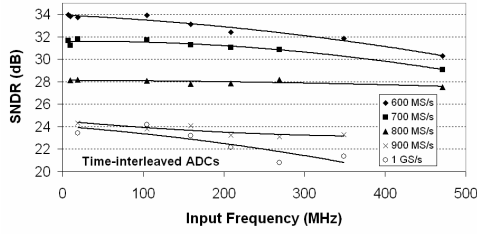
Once the UWB pulse is known, one may calculate the jitter induced noise power for the link budget analysis. In section III, we will perform system simulations to get more insights on the impact of clock jitter.

E. Sub-sampling Mixer and ADC

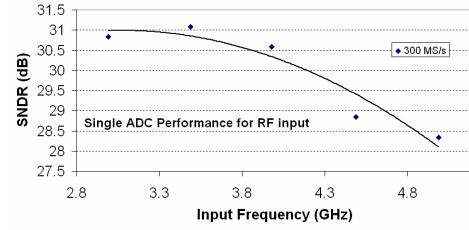
Conventionally, quantization noise power contributed from ADC is modeled as $LSB^2/12$ assuming quantization noise is uniformly distributed [18]. As bit resolution decreases, this noise modeling becomes less accurate. Therefore, we will determine the ADC resolution in system simulations. In a back of envelope calculation, the quantization noise power of a 4-bit ADC is about the same as ambient noise given in section II-C.

One key issue with the proposed system is the implementation cost of a high speed and ultra-wide input bandwidth ADC to perform as a sub-sampling mixer. Previous state-of-the-art high speed (\sim GHz) and medium resolution (6-8 bit) ADCs [19][20][21][22][23][24][25][26] consume at least tens milliwatts to couple watts and only supports up to Nyquist input. The recent development of a high-speed 6-bit asynchronous ADC [27] has pushed the power consumption down to 5 milliwatts at 600 MS/s in 0.13 μ m CMOS process. The ADC prototype utilizes two time interleaved asynchronous ADCs to double the maximum conversion speed that a single ADC can achieve. The core area of a single ADC consumes only 0.06 mm² as shown in Fig. 3. The small occupied silicon area makes it feasible to parallel more ADCs for further speed up in proportion. Deriving from the measured result, a 6-bit ADC with 1 GHz sampling rate consumes less than ten milliwatts.

Another benefit of the proposed ADC architecture is the easy tradeoff between signal-to-noise-plus-distortion-ratio (SNDR) and conversion speed, as it scales from 34 dB at 600 MS/s to 24 dB to 1 GS/s, as shown in Fig 4(a). As the input frequency sweeps from 3 GHz to 5 GHz (Fig. 4(b)), SNDR still remains above 30 dB for input frequency goes beyond 4 GHz. The first prototype is designed for 3-5 GHz band, however, the input bandwidth can be further scaled up



(a) Measured SNDR versus input frequency and sampling rate for two time-interleaved ADCs.



(b) Measured SNDR for RF input signal for a single ADC.

Fig. 4. Dynamic performance of the ADC prototype.

by trading slightly more power consumption on the bigger sampling switches. Besides, as the technology continues to scale down, the intrinsic frequency of a transistor will increase while the sampling capacitance for medium resolution ADC can be kept very small. For example, a sampling capacitance larger than 10's fF has negligible thermal noise for 8-bit ADC. The greatly reduced power and area of a sub-sampling ADC makes the proposed radio architecture promising for low-cost implementation.

III. SYSTEM SIMULATIONS

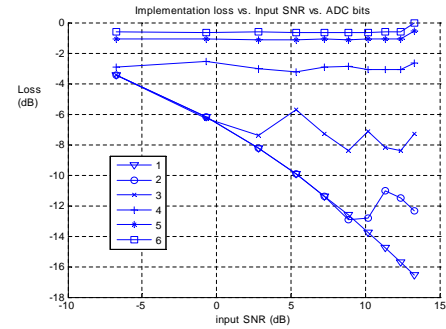
While the previous section provides an analytical approach of designing the proposed system, we now include these circuit non-idealities into system-level simulations using measured noise samples. The simulation takes measured pulses generated from a pulser and TEM horn antenna, whose frequency response is flat between 3 to 10 GHz. For interference and noise, sixty million samples were acquired by the TEM horn antenna and Agilent DSO (54855A), which is capable of sampling at 20 Gsa/s. The measured pulse shape and noise samples were post-processed in Matlab. The pulse is bandlimited to 3-4 GHz and subsampled at 2 Gsa/s.

In the simulation framework, signal and noise are each oversampled at higher rates and filtered by the same bandpass (anti-aliasing) filter. A random jitter can be introduced while downsampling to 2 Gsa/s. The system simulation allows us to investigate input sensitivity, clock jitter, bandpass filter response, gain, ADC bits along with the whole digital signal processing blocks. For the time being, we will focus only on the specifications of analog blocks, while keeping all the digital blocks in floating point.

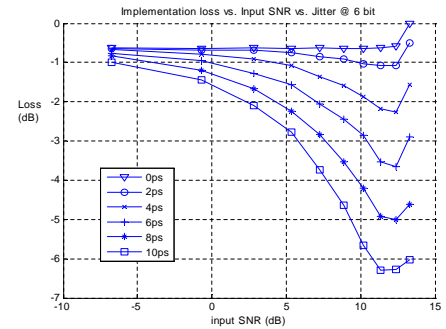
The figure of merit of the proposed design methodology is implementation loss between input (received) SNR and analytic matched filter output SNR, which is measured without any sampling offset or channel estimation error. Next, the relationship between implementation loss and critical system parameters, such as ADC bits, jitter, in-band interference level, and input SNR, will be examined.

- ADC Quantization effect

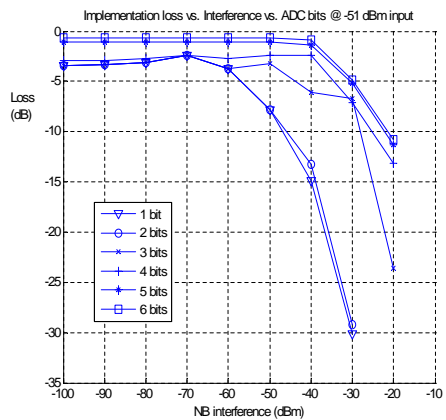
The input signal level is scaled from -51 dBm to -71 dBm as explained in section 5.1. Shown in Fig. 5(a), more than 4-bit quantization is sufficient to keep implementation loss within 3 dB for all input SNR. This is fairly close to hand analysis



(a)



(b)



(c)

Fig. 5. (a) Implementation loss versus input SNR and ADC bits; (b) Implementation loss versus input SNR and jitter; (c) Implementation loss versus in-band interference level and ADC bits.

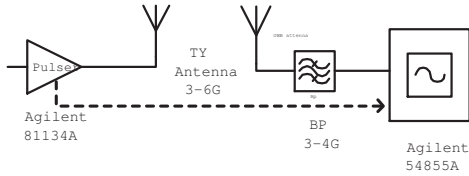


Fig. 6. Discrete prototype configuration.

results. Note that, in the low SNR region, 1-bit ADC does not degrade system performance by much.

- Jitter

In the jitter simulation, a 6-bit ADC is used and RMS jitter varies from 0 to 10 picoseconds. Figure 5(b) shows that a jitter greater than 6 picoseconds can cause more than 3 dB implementation loss. The jitter requirement is relatively stringent; however a fixed frequency clock tends to produce less phase noise than a tunable frequency one [28]. We can also conclude that jitter induced noise dominates the total noise power in high SNR region.

- In-band interference Immunity

Depending on the operating environment, UWB is highly vulnerable to the in-band interference. Therefore, we purposely inject an in-band sine wave to investigate the interference immunity. The simulation results do not include any interference cancellation that can be potentially incorporated into the system. Observing from Fig. 5(c), larger than -40 dBm interference power in general degrades system performance more than 3 dB, because the input-referred saturation level is set around 3 mV (amplitude of -40 dBm interference on 50 ohm impedance). Therefore, input-referred saturation level is a trade-off between interference immunity and quantization noise. We can also observe that more than 3-bit ADC shows a better in-band interference immunity.

IV. SYSTEM PROTOTYPE

A sub-sampling system prototype was set up as shown in Fig. 6 to perform a wireless link. The passive components, such as UWB antenna and bandpass filters, are donated from Taiyo Yuden. The antenna is driven by Agilent 81134A pulse/pattern generator to generate UWB pulses. On the receiver side, Agilent 54855A samples the received signal immediately after antenna and bandpass filter. The oscilloscope front end has a bandwidth of 7 GHz, and around 7 bit built-in ADC. The sampling RMS jitter is reported to be 3 ps.

Using this system prototype, we can verify the proposed complex signal processing technique under sub-sampling front-end. We performed the following experiments:

1. Frequency mismatch of local oscillator between transmitter and receiver introduces the sampling offset as mentioned in the previous section. An experiment was done by transmitting 250 MHz pulse rate with LOS, and sampling rate of 5 Gsa/s. One million samples were taken and the matched filter outputs are shown in Fig. 7(a)–(b). The constellation of matched filter outputs rotate at the rate of frequency offset.

2. Movement of the Tx and Rx under LOS scenario has the similar phenomenon as frequency mismatch, except the

amplitude variation. This experiment was done in 20 Gsa/s sampling mode in order to reduce the triggering uncertainty. The sampled data was decimated by four times in Matlab. The signal was captured at various distance between transmitter and receiver with 3 cm steps. We can see both the time domain view and the trajectory of analytic matched filter output on Euler plane in Fig. 7(c)–(d). The trajectory is composed of phase portrait of the pulse itself and the amplitude attenuation due to free space propagation.

V. CONCLUSION

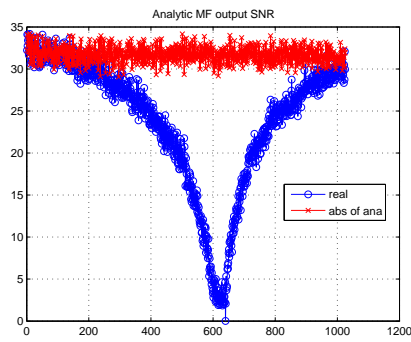
The proposed sub-sampling impulse radio architecture minimizes the building blocks for a low-complexity implementation with the potential of full CMOS integration given the recent demonstration of a high-speed and low-power sub-sampling ADC in a 0.13 μm purely digital CMOS process. A first-order link budget analysis including circuit impairments is provided. The specifications of the critical blocks are verified by both analytical analysis and system-level simulations. A discrete prototype is also built to prove the feasibility of the proposed transceiver architecture. Following the presented design approach, one may determine the optimal circuit specifications of the proposed radio architecture for low-rate ranging systems or high-speed data communications.

ACKNOWLEDGMENT

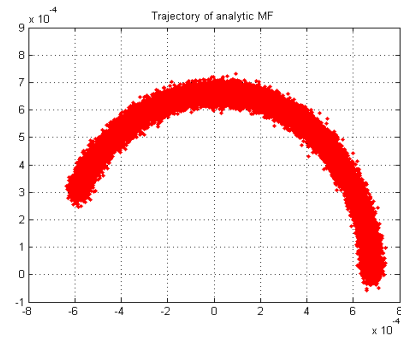
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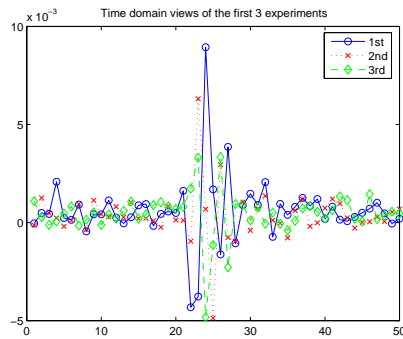
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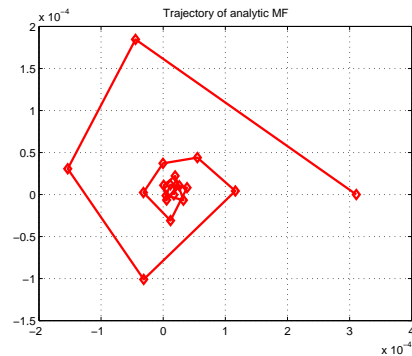
(a) Output SNR of analytic MF.



(b) Trajectory of analytic matched filter output within 0.2 msec.



(c) Time domain views of the first three measurements.



(d) Trajectory of analytic matched filter output of all measurements.

Fig. 7. (a)–(b) Local oscillator frequency mismatch effect; (c)–(d) Measurements with various distance.

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