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**A Radio Frequency Bandpass  $\Sigma\Delta$  A/D**

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**Research Project**

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# Chapter 1

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## *Introduction*

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Direct conversion of a radio signal into digital representation is highly desired. Such a system would allow all radio signal processing to be done completely in the digital domain. This is beneficial for many reasons. First, it allows for an RF system to take full advantage of the availability of inexpensive digital computation brought by modern digital CMOS processes. Second, computation in the digital domain is scalable to accommodate large signal dynamic range with adequate resolution. Last and most importantly, digital signal processing of radio signal is highly programmable. With the increasing demand for multi-standard capable wireless devices, this approach provides a good platform to support any of the existing wireless standards as well as to adapt to the needs of future wireless standards.

So far, such an approach is still not a viable option. The main problem with this approach is that the performance achievable in today's A/D technology is nowhere near the type of performance needed to directly convert a radio signal. Because of this reason, a radio receiver typically precedes an A/D. The radio receiver effectively pre-conditions the radio signal for analog-to-digital conversion. This is done by performing frequency downconversion as well as filtering to reduce the radio signal's dynamic range.

A bandpass  $\Sigma\Delta$  A/D offers an attractive alternative in achieving direct digital conversion of radio signals. A conventional A/D architecture requires both a large dynamic range and a large band-

width of operation in order to convert a radio signal with sufficient fidelity. On the other hand, a bandpass  $\Sigma\Delta$  A/D is able to selectively enhance conversion resolution at a specific frequency band, by moving the quantization noise energy away from that band. Effectively, a bandpass  $\Sigma\Delta$  A/D is able to capture an RF signal faithfully with using a low resolution conversion hardware. The flip side of this approach is the need for a loop filter in order to appropriately suppress quantization noise at the desired frequency band.

Implementing a bandpass  $\Sigma\Delta$  A/D that can operate at radio frequencies still presents a difficult challenge. First, the loop filter has to be able to operate at a high frequency; which pushes the limits of filter design with the available integrated circuits technologies. Second, in order to accommodate for operation in multiple bands, some flexibility has to be built into the filter so that it can be tuned to different frequency bands.

In this project, we address some of the issues and challenges in designing a RF sampling bandpass  $\Sigma\Delta$  A/D through a combination of circuit and system techniques. We present a bandpass  $\Sigma\Delta$  A/D architecture utilizing a passive, discrete-time N-path filter structure as a possible implementation solution.

## **1.1. Scope of this Research**

The goal of this project is to develop, analyze and evaluate system level techniques that would permit the implementation of a direct RF sampling bandpass  $\Sigma\Delta$  A/D.

The main focus of this report would be to discuss the architectural choices made and the reason behind it. Circuit level and implementation details are only provided as far as describing its impacts to the choices made in the architectural level.

The full implementation of the proposed architecture is an ongoing effort and will be discussed in future reports.

A mathematical analysis will be provided when appropriate. Most of the calculations presented in this report have been verified using Simulink or through SpectreRF circuit simulation.

## **1.2. Related Work**

The concept of bandpass  $\Sigma\Delta$  A/D for direct conversion of radio signal is first proposed in [39]. The first successful monolithic implementation of a bandpass noise-shaping modulator is presented in [40]

Over the years the development of bandpass  $\Sigma\Delta$  A/D has been limited to capturing signal at an intermediate frequencies, from the MHz range to low hundred MHz range [38-46]. Nevertheless these examples have very well described the challenges of implementing a bandpass SD A/D, as well as illustrated the difficulty of pushing the center frequency to GHz range frequencies.

Several bandpass modulator structures have been proposed which are able to obtain a very high frequency of operation. One example uses an LC resonator structure in order to achieve the desired response [35, 36]. The problem with this approach is the limited Q-factor of integrated inductor. The quality of the inductor effectively dictates the achievable performance in this architecture. Two examples utilize a combination of frequency modulator-demodulator and a low-pass filter in order to synthesize a bandpass type frequency response [33, 34]. This implementation have some similar aspects to the N-path based loop filter that will be discussed in this report.

The concept of frequency sampling and N-path filter is presented in [18]. The use of N-path filters in a  $\Sigma\Delta$  modulator loop is first introduced in [29]. The two-path bandpass SD A/D architecture

that we developed in section 5.2.1 was later found to have a lot of similarity with the implementation in [17].

The concept of time-interleaving several lowpass  $\Sigma\Delta$  A/D's has been presented in [26-28]. However, in the three papers mentioned the purpose of time-interleaving is simply to increase the oversampling ratio of the  $\Sigma\Delta$  modulator, which is different than the motivation of using the N-path structure discussed in this report.

The concept of performing signal processing in the charge-domain as well as the circuitry needed to build such a system draws a lot of inspiration from [2]. The concept of performing high-order IIR filtering with only switches and capacitors is also presented the same paper, although it has also been discussed elsewhere [47]. We later found that the front-end integrate-and-sample concept was first introduced in [7], and was further analyzed in [8] and [9].

### **1.3. Thesis Organization**

Chapter two describes the motivation of exploring a bandpass  $\Sigma\Delta$  architecture based on current demands placed on future radio receiver designs, as well as the limitation of conventional receiver architectures.

Chapter three provides an overview of the proposed architecture, with the emphasis being on how the pieces fit together in the overall architecture

Chapter four to seven is dedicated to explaining each of the four major enabling techniques in the architectures.

Chapter four presents an analysis on a windowed-charge-sampler circuit, which proves to be a versatile building block for our architecture.

Chapter five describes how a bandpass type frequency response can be synthesized using an N-path filter built using discrete-time integrators.

Chapter six is devoted into explaining a technique to build high-order filters using passive components; i.e. switches and capacitors.

In chapter seven, we introduce a background digital calibration technique that would mitigate the effect of mismatches in the proposed N-path filter structure.

Finally, in chapter eight we conclude by stating the contributions made by this project as well as outlining our planned future efforts in the topic.



# Chapter 2

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## *Motivation*

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In this chapter, we discuss the current demands that are driving new designs in the wireless semiconductor industry. We would then translate these demands into requirements and challenges for a receiver architecture as well as the associated RF circuits. We conclude by discussing a bandpass  $\Sigma\Delta$  A/D as a potential alternative for future receivers.

### **2.1. Demand for a Highly Reconfigurable CMOS Receivers**

Currently there are two major driving force for innovations in the wireless integrated circuits industry. The first is the demand for a higher level of integration. The second is the desire for a more flexible, more programmable, multi-standard capable wireless devices.

Cost is usually the main motivation for achieving a highly integrated solution. Recent case studies on ‘single-chip’ quad-band GSM phones from three different companies claim cost savings up to 50% in favor of their respective single chip solution [4]. Integration to a single-chip solution also reduces the board space required for the wireless transceiver module, which potentially opens up space for additional functions to be implemented in the wireless device.

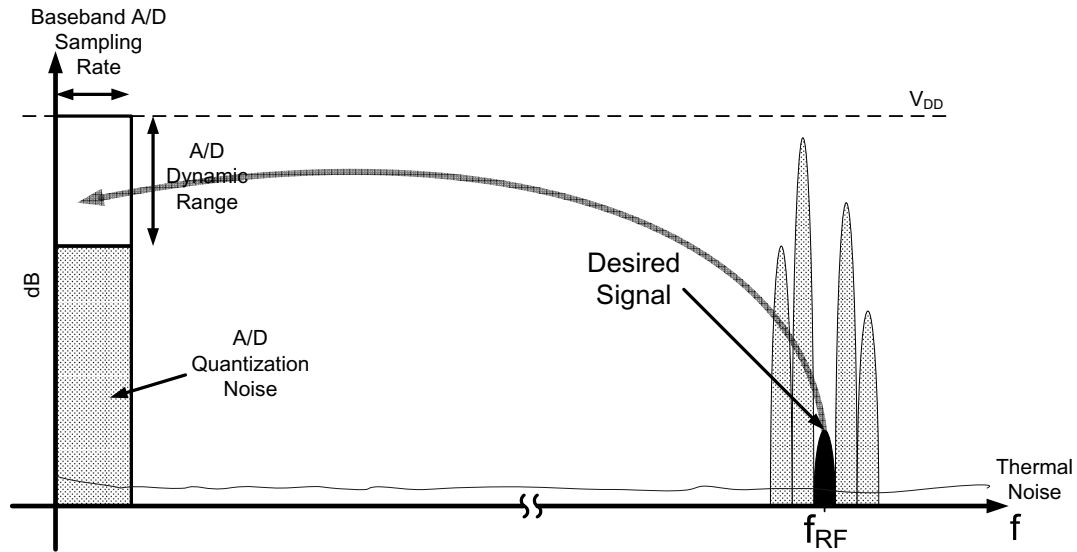
On the other hand, the demand for reconfigurability usually stems from the need to support multiple wireless standards. Initially, maintaining backward compatibility is the primary, and perhaps the only, reason for supporting multiple wireless standards in a single device. However as the

wireless application space grows, different usage scenarios arise, and with them different wireless standards are created for each. For example, current high-end handsets might support GPRS/EDGE for anywhere/mobile data access, WiFi for high-speed data transfer, and Bluetooth for short-range wireless communication between devices. Each of the standards mentioned above is tailored towards a specific usage model; but when they are combined together in a single wireless device, they complement each other in providing a comprehensive wireless connectivity options to the user.

We argue that these two requirements set the stage for a reconfigurable CMOS radio receiver. Currently CMOS still offers the highest level of integration at a reasonable cost; other technology such as BiCMOS might offer better RF performance, however they can not achieve the same level of integration while maintaining a reasonable cost. Reconfigurability is key in achieving a power, area and therefore cost effective solution in a multi-standard receiver. Having several dedicated receivers for each wireless standards might offer a fast time-to-market ad-hoc solution, however it probably does not offer the most efficient solution. Being able to reconfigure a receiver for different wireless standards are much more desired. In this manner, much of the radio components can be shared between the different wireless standards

## **2.2. Function of Radio Frequency Receiver**

One can view the function of a radio receiver simply as a signal conditioner for an A/D. Since almost all radio today takes advantage of some amount of digital processing, it is reasonable to assume that an A/D will be present in any radio receiver. Signal conditioning is necessary since an A/D performance is typically limited, and can not extend to the frequency and the dynamic range required to capture a radio signal directly.



**Figure 2-1.** Function of RF Receiver

This viewpoint is depicted in figure 2-1. The desired RF signal is present at some high frequency; and it is buried in noise and large nearby interferers. Near the origin of the graph, we showed a typical mask for the A/D. The mask represents the limitations of the A/D; sampling rate in the horizontal axis, and number of bits or dynamic range in the vertical axis. The function of a radio receiver is to process the RF signal so that it fits within the A/D mask; and even more, so that it can take maximum advantage of the A/D available dynamic range. At the same time, this processing has to be done in such a way so that the fidelity of the desired RF signal is maintained. The two main adversaries in accomplishing this particular task is circuit noise and the generation of spurious signals due to nonlinear interaction within the circuit [12, 13]. Typically suppression of noise and nonlinearity in integrated circuits is rather costly, both in terms of area and also power.

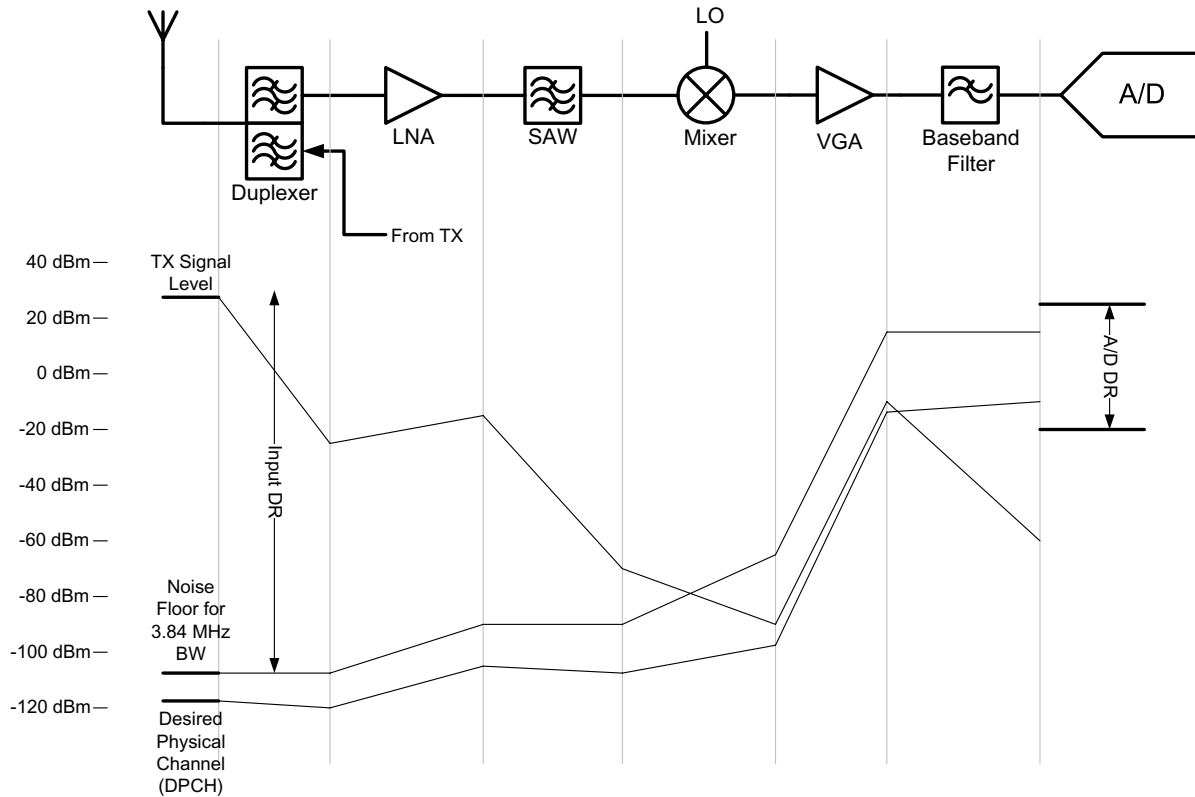
The viewpoint taken to describe a radio receiver as a signal conditioner for an A/D is important in illustrating the difficulties and challenges that are present in order to adapt conventional receiver architectures for multi-standard operation. Furthermore, this viewpoint also illustrates well our

approach of using a bandpass  $\Sigma\Delta$  A/D as a good alternative. In a bandpass  $\Sigma\Delta$  A/D we absorbed the radio receiver function completely into the A/D. A bandpass  $\Sigma\Delta$  A/D simply moves the A/D mask to be centered around the desired carrier frequency and at the same time increases its dynamic range through oversampling and noise-shaping. By doing so, the A/D can capture the desired signal directly, without much of signal conditioning.

### **2.3. Cost of Reconfigurability in Radio Receiver**

In order to develop an intuition on what compromises had to be made to incorporate reconfigurability in radio receiver, it is worthwhile to analyze a typical radio receiver chain. In figure 2-2 we showed a dynamic range calculation along a receive path for a mobile W-CDMA handset. The calculation, along with the performance assumptions on each of the blocks, are adapted from [15] and [16]. At the top of the figure is the architecture of the receiver. On the bottom part of the figure, we showed the power levels of three different signals as each traverses the receive chain. The left and right boundary conditions in this analysis are set by the signal levels at the antenna, and the dynamic range or resolution of the A/D respectively. The three signals that we analyzed in this case is, the desired channel (called DPCH in W-CDMA standard), the noise floor integrated for the channel width, and one interfering signal. The particular interfering signal shown in this analysis is the signal leakage from the transmitter through the duplexer. This analysis can be further extended to include more interferer or blocking signals, to see how each possible interfering signal affects the specifications of each constituent blocks in the receive chain.

The analysis depicted in figure 2-2 illustrates the importance of frequency-selective blocks in managing the dynamic range requirements in a radio receiver. The large dynamic range requirement for constituent blocks in a receiver is most likely reserved for large blocker signal, not for



**Figure 2-2.** Dynamic range calculation along a receive path in a W-CDMA receiver

the desired signal. Since blocker signals are separated in frequency with the desired RF signal, filtering is a natural solution to reduce the dynamic range requirements for any of the blocks in a receiver.

Unfortunately, often times filtering can be highly incompatible with reconfigurability. A SAW filter is a good example; it provides up to 40 dB in interferer rejection, however at the same time it is not programmable. If the front-end SAW filter is to be removed, then the downstream blocks have to accommodate and somehow absorb 40 dB more dynamic range.

A similar case can be made for the baseband filters. Although baseband filters operate at low frequencies, they are often times quite complex. This is typically due to a very stringent in-band droop requirement, governed by the system specification. A fifth or seventh order filter is not

uncommon for baseband filters in a direct conversion receiver [6, 32]. Baseband filters can be made programmable; however, it is not without cost. Additional circuitry has to be built-in to accommodate programmability. Furthermore, if the filter is made with continuous-time circuitry, then a tuning loop is necessary to obtain the correct critical frequencies.

This example underlies the main challenge in implementing a highly reconfigurable receiver. Conventional receiver architectures utilize filtering extensively to manage signal dynamic range as it traverses through the receiver. Unfortunately, programmable filters available at the present is still very cumbersome. In order to obtain reconfigurability in a radio receiver, one might be forced to remove some filtering stages, such as the front-end SAW filter. Removing filters in a receiver, in turn would result in a more stringent and difficult to achieve linearity as well as dynamic range requirements on each blocks in a receiver.

## **2.4. Bandpass $\Sigma\Delta$ A/D as a Radio Receiver**

A radio signal is actually a very good candidate to be processed by a bandpass  $\Sigma\Delta$  modulator. A radio signal typically has a small bandwidth, however it is centered at a high frequency. In order to accommodate the high center frequency, a high sampling rate is necessary. However, the signal itself is constrained within a relatively small fraction of the necessary sampling frequency; thus giving rise to the natural oversampling ratio. Because of the above reason, a bandpass  $\Sigma\Delta$  A/D architecture appears quite attractive to be used as a radio receiver.

Perhaps the main advantage of a bandpass  $\Sigma\Delta$  A/D is the fact that it samples the signal directly at RF; in other words it captures the signal as is. Because of this reason it is immune to the problems commonly found in conventional receiver architectures, such as  $1/f$  noise problems, DC offsets,

and overlaps with undesired images, quadrature signal, as well as low frequency intermodulation products.

In the context of re-programmability, a bandpass  $\Sigma\Delta$  A/D is attractive because the channel selection and demodulation can be accomplished digitally. By performing these two operations digitally, one would expect that it would be relatively easy to reconfigure it to a different wireless standard.

The main challenge in implementing a bandpass  $\Sigma\Delta$  A/D is in the implementation of the modulator loop filter. First, this loop filter has to be able to run at high frequencies. Second, the loop filter determines the critical frequencies of the quantization noise shaping. Therefore, some form of programmability must also be built into the loop filter to accommodate multi-standard operation. Last, these filters would also need to have a large dynamic range in order to accommodate an RF signal as it is seen at the antenna.

Other parts of a  $\Sigma\Delta$  modulator, such as quantizer and feedback D/A also needs to operate at a high frequency, and therefore the design of each could also be quite challenging. However, we viewed that these circuits will not be the bottleneck in the overall design process.

There are many examples in the literature [17, 33-38] in the use of a bandpass  $\Sigma\Delta$  A/D for capturing radio signals at an intermediate frequency. However there is only a handful example where a bandpass  $\Sigma\Delta$  A/D is used to capture an RF signal directly. The main limitation here typically originates from the difficulty in creating a good high-frequency amplifiers in order to synthesize a bandpass filter at RF.

Despite these challenges, there is much room for exploration for a receiver based on a bandpass  $\Sigma\Delta$  A/D. If such bandpass  $\Sigma\Delta$  A/D can be realized, it has the potential to make possible the real-

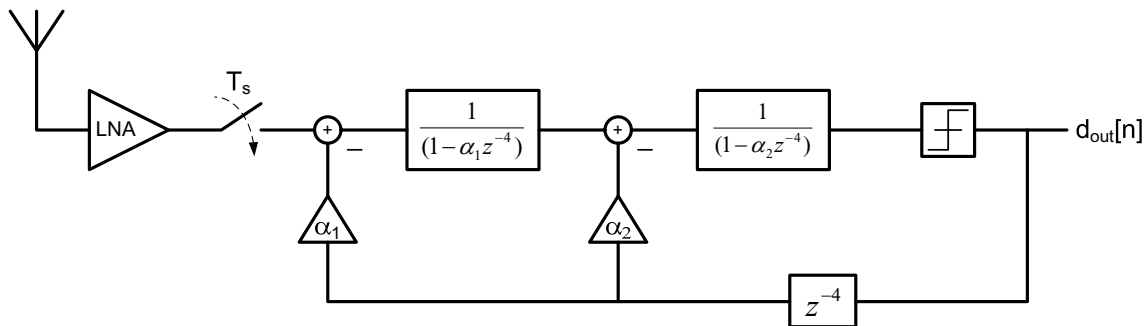
ization of a true software defined radio; where the degree of programmability in a receiver can be pushed to almost limitless. As a research project, we viewed that there is a reasonable balance between benefits and challenges so as to make this an interesting research direction.

# Chapter 3

## Architecture Overview

In this chapter we will provide a short overview of the proposed bandpass  $\Sigma\Delta$  A/D architecture. The architecture contains four key components: a sampler, an N-path loop filter, a passive high-order filter, and a digital calibration routine. These four components will be discussed in great detail in the next four chapter. The purpose of this chapter is to provide an overview on how each of the four parts fit together in the architecture level.

A model of the architecture is shown in figure 3-1. An LNA is used to provide an input match to the antenna as well to provide some voltage gain. The output of the LNA will be directly sampled and converted to digital through the use of a bandpass  $\Sigma\Delta$  A/D. The bandpass  $\Sigma\Delta$  A/D is built using a discrete-time signal processing circuit. The resulting noise-shaping is of a second-order type, with a center frequency of  $\frac{f_s}{4}$ , where  $f_s$  is the A/D sampling frequency. The sampling frequency is set to be four times the carrier frequency of the RF signal, so that the desired RF signal



**Figure 3-1.** Proposed bandpass  $\Sigma\Delta$  receiver architecture

falls exactly within the quantization noise notch generated by the  $\Sigma\Delta$  modulator. The signal and noise transfer function of the proposed architecture is given below:

$$STF = 1 \quad (3.1)$$

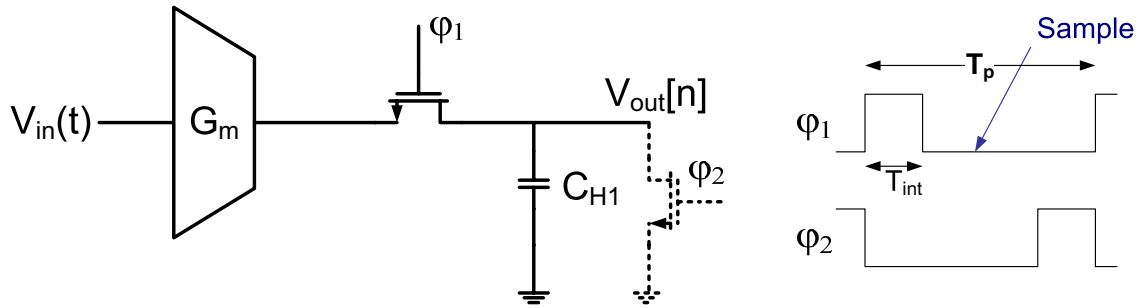
$$NTF = (1 - \alpha_1 z^{-4})(1 - \alpha_2 z^{-4}) \quad (3.2)$$

A 1-bit quantizer as well as a 1-bit feedback DACs are used in the loop. An oversampling ratio in the order of one thousand is typical, considering that most wireless standard has a bandwidth in the order of 1 MHz, with a carrier frequency in the GHz range.

Direct RF sampling is usually desirable, since most of the channel selection and final demodulation process can be done in the digital domain. Noise shaping in a bandpass  $\Sigma\Delta$  modulator can selectively enhance conversion resolution exactly around the desired RF band, by using a simple low-resolution quantizer. Furthermore, due the discrete-time nature of all the signal processing operation, the architecture is fully clock-programmable to adapt to different frequency bands.

Sampling a continuous-time signal at radio frequencies presents a formidable challenge, especially if a high signal fidelity is to be maintained. A typical track-and-hold circuit, commonly found in most A/D, would require a lot of power in order to maintain the high bandwidth necessary while keeping the circuit noise low enough. In this architecture a novel windowed-charge-sampler is proposed.

A typical track-and-hold circuit samples the instantaneous input voltage to the circuit. A windowed-charge-sampler circuit, on the other hand, integrates the input current over a period of time, and then samples the resulting value. When the sampling switch is closed, an incoming input current is integrated into the sampling capacitor. At the instant when the switch is opened,



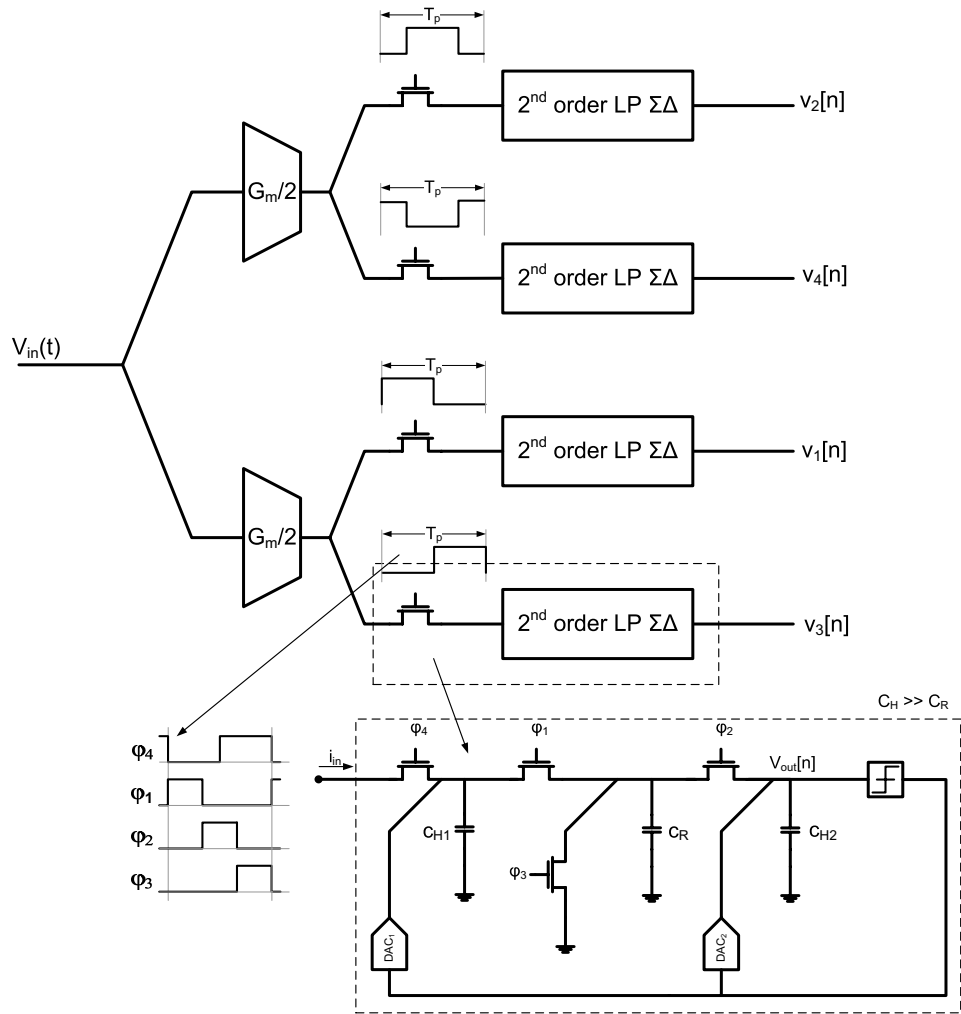
**Figure 3-2.** Windowed-charge-sampling front-end

the resulting integration value is sampled. The current integration operation is analogous to performing a rectangular windowing on the continuous-time input signal before the sampling operation. In the frequency domain, the rectangular windowing results in a sinc-shaped frequency response. This sinc-shaped frequency response actually partially protects the system against aliasing of undesired signals at harmonic frequencies of the RF carrier frequency.

The reset phase after each integrate-sample operation can be omitted to implement a discrete-time integrator within the same capacitor. By not periodically resetting the sampling capacitor, this capacitor continuously adds the value of new samples to an existing running sum. Therefore a discrete-time integrator is realized.

The main disadvantage that has precluded this sampling approach from widespread use in conventional A/D, is the sinc frequency response distortion due to the integration operation. However, since in our application the RF signal bandwidth is actually very small when compared to the sampling frequency, the frequency distortion over the bandwidth of interest would be insignificant.

Realizing a  $\Sigma\Delta$  loop filter to operate at RF has so far been significantly limited by the difficulty of implementing a reasonable amplifier that can operate at high frequencies. From linear system theory, we know that an integrators are all that is needed to implement a general filter function. In



**Figure 3-3.** Four-path bandpass  $\Sigma\Delta$  A/D with second-order noise shaping

integrated circuits, a capacitor is actually a perfect (charge) integrator. The problem arises when several of these integrating capacitors are to be linked together; or when a feedback path is needed. In both cases an active linear amplifier is necessary, usually to perform some kind of a voltage-to-current conversion.

The loop filter of the proposed bandpass  $\Sigma\Delta$  A/D is built using a four-path structure. Each of the four paths consisted of a cascade of two lossy integrators; which give rise to the second-order noise shaping.

A general N-path filter structure enables a  $z^N \rightarrow z$  transformation. In this context, we utilized this transformation to allow us to build a bandpass type frequency response using discrete-time integrators as a building block. An N-path filter built using N discrete-time integrators effectively allows us to place N poles which are radially equispaced around the z-plane unit circle. Hence, in a four-path implementation, the filter produces poles at  $z = \pm 1$  and at  $z = \pm j$ , which give rise to the desired transfer function. By cascading two integrators per path, we are able to put two poles, instead of one, on each of the four locations mentioned. The result is greater attenuation for the in-band quantization noise.

The complete loop filter is implemented without any active amplifiers, except for the transconductor that drives the windowed-charge-sampling circuit. The first integrator in the cascade for each of the four path is actually built using the discrete-time integrator embedded in the sampler circuit. The second integrator is built using another capacitor ( $C_{H2}$ ). Instead of using an active amplifier to link the two capacitors, a small rotating capacitor  $C_R$  is used. That is, instead of performing a V-I conversion as in a conventional filter structure, the state of one integrator is relayed to the next integrator through charge transfer. This is done by physically disconnecting a small capacitor from one integrating capacitor and connecting it to the next. However, since a small fixed fraction of the charge inside each capacitor is used up in the process, both integrators in the cascade become lossy.

Since the A/D architecture is essentially a time-interleaved A/D, matching between the different paths is crucial. Mismatch between paths in this architecture would give rise to similar effects as I/Q imbalance and DC leakage problem in homodyne architecture. An online background digital calibration will be used to compensate for these mismatches.



# Chapter 4

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## *Windowed Charge Sampling*

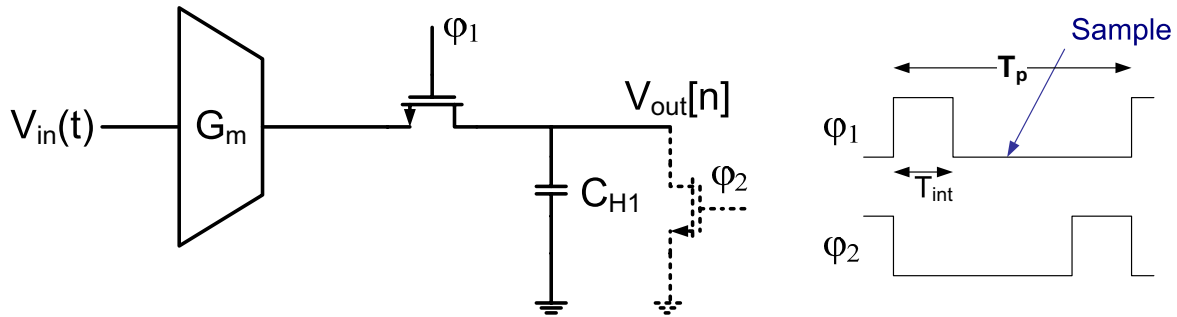
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The front-end sampler is arguably the most important part of any analog, discrete-time signal processing system. Since this circuit is typically located at the very front of the system, any signal degradation resulting from this circuit would severely impact the overall performance of the system. Noise and linearity requirement of this front-end circuit is usually very stringent; as any impairments generated by this stage is usually irreversible by the succeeding circuits. Because of this reason, it is quite common to have this front-end circuit to be the dominant power consumer of the overall system.

In this chapter, we would introduce an alternative sampling circuit, which we would call a windowed-charge-sampling circuit. We will discuss the details of a windowed-charge-sampler circuit, as well as the impact of various parasitics towards the performance of the circuit.

### **4.1. Charge Sampling**

In a traditional track-and-hold sampling circuit, a large voltage buffer drives a sampling capacitor to equalize the input voltage with the voltage of the sampling capacitor. When the sampling switch is opened, the sampling capacitor stores the instantaneous voltage of the input. In other words, a track-and-hold circuit **samples the instantaneous value of the input voltage.**



**Figure 4-1.** Windowed charge sampler circuit

On the other hand, a windowed-charge-sampling circuit **samples an integrated value of the input current** (charge) over a time window  $T_{int}$  (figure 4-1). When  $\phi_1$  is high, the current from the transconductor is continuously integrated in the capacitor. At the instant when  $\phi_1$  goes low, the integrated value is sampled and stored in the hold capacitor  $C_{H1}$ . A reset phase is provided by a second switch. Before the beginning of the next integration phase,  $\phi_2$  goes high and the capacitor voltage is reset back to zero. The current integration operation is equivalent to performing a rectangular windowing on the continuous-time input signal before the sampling operation. We used the term **charge sampling** to emphasize the fundamental physical quantity being manipulated in this circuit. Current is nothing more than a measure of charge flow over time. This distinction is very important in later chapters, where multiple charge-domain manipulation is performed within circuits with very few components. In those cases, analysis in charge domain becomes much more intuitive. Conversion to a voltage value can be done at the very end of the signal processing operation, through a simple division with an appropriate capacitance value

Let  $q_{in}[n]$  be the total amount of charge transferred to the hold capacitor on each sampling period. We can write  $q_{in}[n]$  as:

$$q_{in}[n] = G_m \int_{nT_p}^{(nT_p + T_{int})} V_{in}(t) dt \quad (4.1)$$

where  $T_p$  denotes the sampling period. The output voltage to be read out is simply:

$$V_{out}[n] = \frac{q_{in}[n]}{C_{H1}} \quad (4.2)$$

By manipulating equation 4.2, we can emphasize the windowing operation being performed in the circuit;

$$q_{in}[n] = G_m \int_{-\infty}^{(nT_p + T_{int})} V_{in}(\tau) p_{T_{int}}(nT_p + T_{int} - \tau) d\tau \quad (4.3)$$

where  $p_{T_{int}}(t)$  is a pulse from the origin with width  $T_{int}$ , or:

$$p_{T_{int}}(t) = \begin{cases} 1 & 0 \leq t \leq T_{int} \\ 0 & \text{otherwise} \end{cases} \quad (4.4)$$

We can evaluate the frequency response of the circuit by directly inputting a hypothetical complex sinusoid of frequency  $\Omega$  and carrying out the analysis as follows:

$$\begin{aligned}
H_w(\Omega) &= G_m \int_0^{T_{int}} e^{-j\Omega\tau} d\tau \\
&= je^{\frac{j\Omega T_{int}}{2}} G_m \left[ \frac{\sin\left(\frac{\Omega}{2} T_{int}\right)}{\frac{\Omega}{2}} \right]
\end{aligned} \tag{4.5}$$

Simplify by multiplying top and bottom with  $T_{int}$  and taking the magnitude to get:

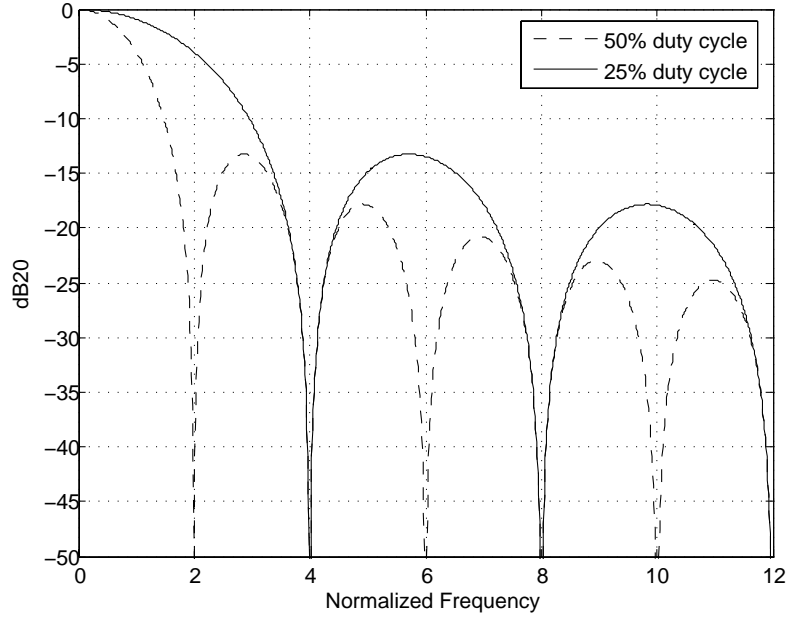
$$|H_w(\omega)| = G_m T_{int} \left| \frac{\sin\left(\omega\pi \frac{T_{int}}{T_s}\right)}{\omega\pi \frac{T_{int}}{T_s}} \right| \tag{4.6}$$

where  $\omega$  is the normalized sampling frequency, i.e.:

$$\omega = \frac{\Omega}{2\pi \frac{1}{T_p}} \tag{4.7}$$

The sinc-shaped frequency response of a rectangular window becomes apparent in the above equations.

Let us now define the constant gain factor  $G_m T_{int}$  as the **sampling gain** of the windowed-charge-sampler circuit. The naming is consistent with the fact that, if the input to the circuit is a constant DC voltage, then the total charge transferred to the sampling capacitor equals to the DC voltage multiplied with the sampling gain. The factor  $\frac{T_{int}}{T_p}$  corresponds to the **duty-cycle** of the sampling circuit; that is, the fraction of integration window length when compared to the sampling period (in percent).



**Figure 4-2.** Frequency response of prefilter

Figure 4-2 shows the frequency response for the rectangular window with a duty-cycle of 25% and 50%. The sampling-gain factor is taken out in this figure. We see that with at 25% and 50% duty-cycle, the rectangular window nulls out signals at multiples of four times and two times of the sampling frequency respectively.

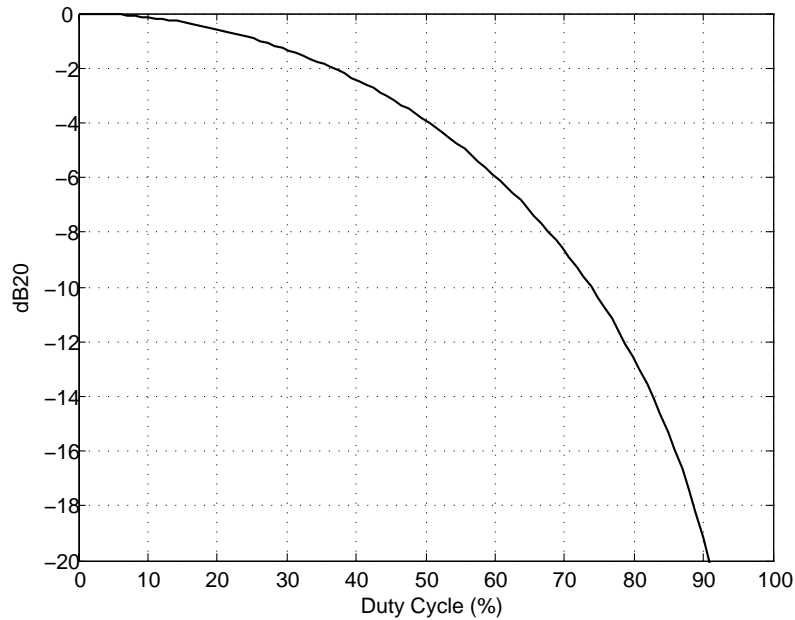
Figure 4-3 shows the effect of changing the duty cycle towards the signal gain at the sampling fre-

quency  $f_p$ , if the sampling gain  $G_m T_{int}$  is kept constant. Note that the factor  $\frac{G_m T_{int} V_{in}^2}{T_p}$  denotes

the energy per sampling period that is needed to drive the sampler circuit. Therefore, keeping

$G_m T_{int}$  constant is actually a good proxy to requiring the power consumption of the  $G_m$  transcon-

ductor to remain the same.

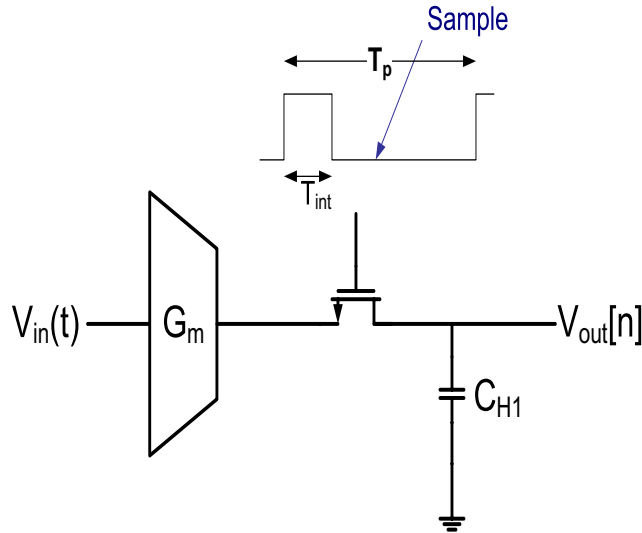


**Figure 4-3.** Signal gain at  $f_s$  vs. duty cycle

The significance of signal gain at the sampling frequency becomes more obvious once we considered the bandpass  $\Sigma\Delta$  architecture proposed in this project. Suffices to say that, because of the time-interleaved structure of the A/D, the RF signal of interest will be located at  $f_p$ .

From figure 4-2, we note that the windowing operation is actually quite beneficial for our proposed architecture. The rectangular window actually provides protection against aliasing of the harmonics of the RF signal. For example, if we use a 50% duty cycle, the prefilter will protect against all even harmonics of the desired signal. If we use a 25% duty cycle instead, we only achieve protection against aliasing from multiples of four of the desired signal's frequency. However, the circuit with 50% duty cycle has about 3dB (dB20) less sampling gain at  $f_{RF}$ .

In short, a windowed-charge-sampler circuit samples the *integrated input current*, instead of sampling an input voltage. The integration operation is analogous to a rectangular windowing operation, and therefore is frequency selective. We showed the relationship between the relative length



**Figure 4-4.** Windowed charge sampler with embedded discrete-time integrator

of the window with respect to the sampling period (duty-cycle), towards the frequency response of the sampler circuit. We would like to emphasize the function of this circuit as a sampler, despite the presence of an embedded continuous-time prefilter. This circuit is the interface between the continuous-time and the discrete-time domain. The output  $q_{in}[n]$  will be viewed simply as a discrete-time signal from this point on.

We can also embed a discrete-time integrator that operates on the input samples, within the same circuit. By omitting the reset phase on each period, each new input samples is added to an existing running sum, and thus a discrete-time integrator is also realized. Let  $v[n]$  be the output of the embedded discrete-time integrator, then we can write

$$v[n] = v[n - 1] + q_{in}[n] \quad (4.8)$$

where  $v[n - 1]$  indicates the existing running sum inside the capacitor, and  $q_{in}[n]$  is defined as in eq. 4.1. In this case, the output voltage  $V_{out}[n]$  is:

$$V_{out}[n] = \frac{v[n]}{C_{H1}} \quad (4.9)$$

The distinction that we made earlier on operating in charge domain becomes somewhat relevant here. If we were to analyze this circuit in charge domain, it becomes difficult to separate the integration operation from the charge-sampling operation.

In the proposed bandpass  $\Sigma\Delta$  architecture, the reset phase is omitted. This embedded discrete-time integrator actually forms the first-stage of the  $\Sigma\Delta$  loop filter.

## 4.2. Effects of Parasitic Loading in Windowed Charge Sampler Circuit

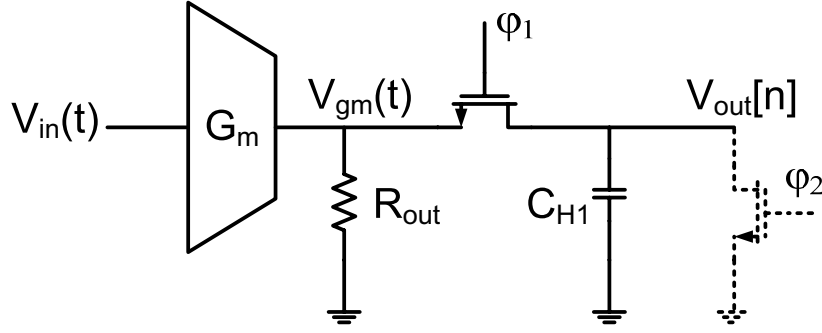
In this section, we will analyze the effects of circuit parasitics on the windowed-charge-sampler circuit. Specifically, we will analyze the impact of output resistance, and output capacitance of the  $G_m$  cell to the response of the sampler circuit.

### 4.2.1. Impact of $G_m$ Output Resistance

Let  $R_{out}$  be the output resistance of the  $G_m$  cell. For the purpose of this discussion let  $V_{gm}$  be the output voltage of the  $G_m$  cell. Note that  $V_{gm}$  is a continuous-time signal, whereas  $V_{out}[n]$  is a discrete-time signal. We will first analyze the case when the capacitor is reset periodically.

To analyze the impact of  $R_{out}$  towards the sampler's response, we start by writing KCL at the  $V_{gm}$  node, when  $\phi_1$  is high:

$$\begin{aligned} G_m V_{in}(t) &= \frac{V_{gm}(t)}{R_{out}} + C_{H1} \frac{dV_{gm}(t)}{dt} \\ \frac{dV_{gm}(t)}{dt} &= -\frac{V_{gm}(t)}{R_{out}C_{H1}} + \frac{G_m V_{in}(t)}{C_{H1}} \end{aligned} \quad (4.10)$$



**Figure 4-5.** Impact of  $G_m$  output resistance

We assumed zero switch resistance to simplify the analysis. We can solve for the above differential equation:

$$V_{gm}(t) = e^{-\frac{t}{R_{out}C_{H1}}}V_{gm}(0) + \frac{G_m}{C_{H1}} \int_0^t e^{-\frac{1}{R_{out}C_{H1}}(t-\tau)} V_{in}(\tau) d\tau \quad (4.11)$$

Since in this case the capacitor is reset before the integration period begins, at the end of each integration period, we have:

$$V_{gm}(T_{int}) = \frac{G_m}{C_{H1}} \int_0^{T_{int}} e^{-\frac{1}{R_{out}C_{H1}}(T_{int}-\tau)} V_{in}(\tau) d\tau \quad (4.12)$$

Using the previous definition of  $q_{in}[n]$  as the total integrated input charge on each sampling period, we can directly identify  $q_{in}[n]$  from eq. 4.12 as:

$$\begin{aligned} q_{in}[n] &= G_m \int_0^{T_{int}} e^{-\frac{1}{R_{out}C_{H1}}(T_{int}-\tau)} V_{in}(nT_p + \tau) d\tau \\ &= G_m e^{-\frac{T_{int}}{R_{out}C_{H1}}} \int_0^{T_{int}} e^{\frac{\tau}{R_{out}C_{H1}}} V_{in}(nT_p + \tau) d\tau \end{aligned} \quad (4.13)$$

We can rewrite eq. 4.13 as a convolution of the input signal with a windowing function similar to eq. 4.3. In this case the windowing function  $p_{T_{int}}(t)$  is:

$$p_{T_{int}}(t) = \begin{cases} e^{-\frac{t}{R_{out}C_{H1}}} & 0 \leq t \leq T_{int} \\ 0 & otherwise \end{cases} \quad (4.14)$$

Intuitively, the new windowing function results from the RC-decay formed by the output resistance of the  $G_m$  cell with the sampling capacitor  $C_{H1}$ .

To evaluate the frequency response of the new windowing function, we can input a complex sinusoid to the sampler:

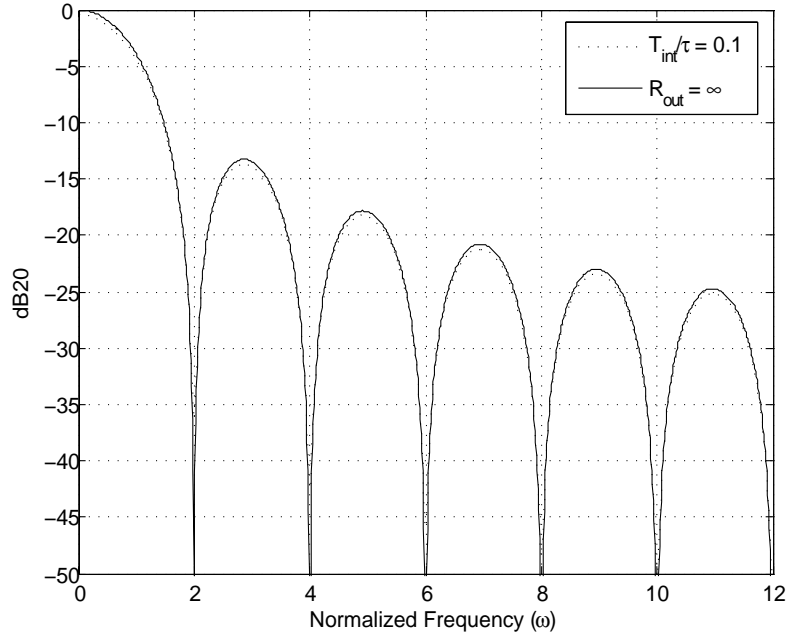
$$\begin{aligned} H_w(\Omega) &= G_m e^{-\frac{T_{int}}{R_{out}C_{H1}}} \int_0^{T_{int}} e^{\frac{\tau}{R_{out}C_{H1}}} e^{-j\Omega\tau} d\tau \\ &= G_m e^{-\frac{T_{int}}{R_{out}C_{H1}}} \int_0^{T_{int}} \exp\left\{\left(\frac{1}{R_{out}C_{H1}} - j\Omega\right)\tau\right\} d\tau \end{aligned} \quad (4.15)$$

which we can solve and simplify to:

$$H_w(\Omega) = \frac{G_m T_{int}}{\frac{T_{int}}{R_{out}C_{H1}} - j\Omega T_{int}} \left[ e^{-j\Omega T_{int}} - e^{-\frac{T_{int}}{R_{out}C_{H1}}} \right] \quad (4.16)$$

Using the same definition for  $\omega$ , and let  $\tau = R_{out}C_{H1}$ ,

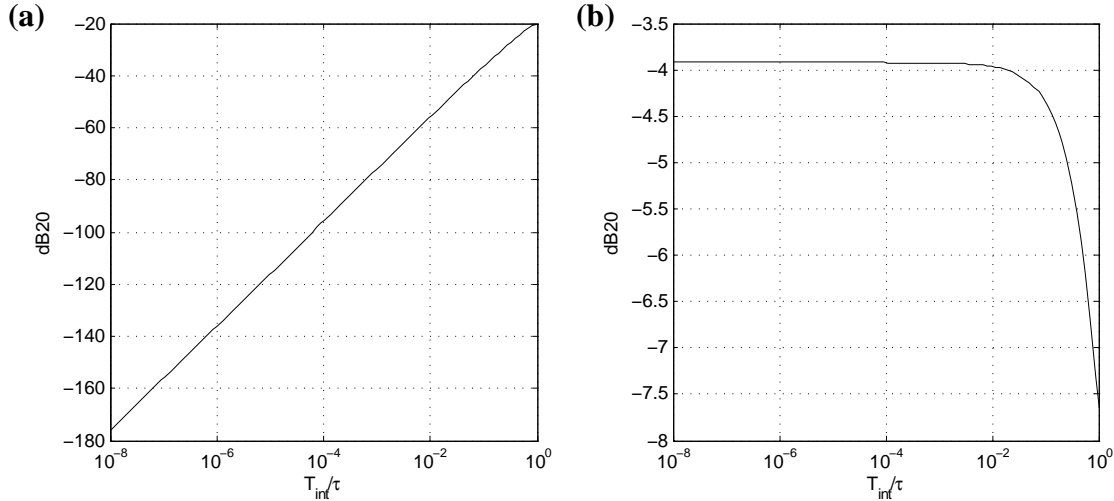
$$H_w(\Omega) = \frac{G_m T_{int}}{\frac{T_{int}}{\tau} - j2\pi \frac{T_{int}}{T_p} \omega} \left[ e^{-j2\pi \frac{T_{int}}{T_p} \omega} - e^{-\frac{T_{int}}{\tau}} \right] \quad (4.17)$$



**Figure 4-6.** Frequency response of sampler circuit with  $R_{out}$

From eq. 4.17, the sampling gain, and the duty cycle factor is apparent. We also have one more ratio,  $\frac{T_{int}}{\tau}$  which indicates the ratio between the length of the window and the bandwidth of the sampling circuit.

Figure 4-6 compares the response of the original sampler circuit with one that includes the effect of output resistance  $R_{out}$ . Figure 4-7 displays the frequency response of the circuit at two frequencies corresponding to response to signal at  $f_p$  ( $\omega = 1$ ) and  $2f_p$ . With respect to the  $\Sigma\Delta$  modulator, these two frequencies corresponds to the desired RF signal frequency, and the (undesired) first even-order harmonic of the RF signal. As long as  $\frac{T_{int}}{\tau}$  ratio is smaller than 0.01, the output resistance of the transconductor have negligible impact towards the RF signal gain. On the other hand, the  $\frac{T_{int}}{\tau}$  ratio have a one-to-one relationship to the magnitude of the second order harmonic sig-



**Figure 4-7.** Frequency response of sampler circuit vs.  $T_{int}/\tau$   
**(a)** at  $\omega = 2$ , **(b)** at  $\omega = 1$

nal. Therefore, whereas in the ideal sampler the signal at  $2f_p$  is perfectly rejected; with a finite  $R_{out}$  of the transconductor, this rejection is reduced and is a function of  $\frac{T_{int}}{\tau}$ . This statement also applies to all other even harmonics of the RF signal in a 50% duty-cycle sampler circuit. In short, the output resistance of the transconductor reduces the effectiveness of the built-in anti-aliasing capability of the sampler circuit.

To put the analysis above in perspective, it is worthwhile to work out a numerical example. Suppose the size of  $C_H$  is 10 pF, and we used a 50% duty cycle, with a sampling rate  $f_p$  of 1 GHz. An output resistance of 5k $\Omega$ , would amount to  $\frac{T_{int}}{\tau}$  ratio of 0.01. This means that the rejection at even multiples of  $f_p$  is around -40 dB, and the sampling gain at  $f_p$  is  $\sim$ -4dB less than at DC.

It is worth noting the different resulting requirements on  $R_{out}$  between a track-and-hold circuit and this windowed-charge-sampler circuit. In a track-and-hold circuit, it is desirable to keep the output resistance of the buffer circuit to be as small as possible. In contrast, in a windowed-charge-

sampling circuit, one can argue that a large output resistance is desired. Although, from figure 4-7, and the example above, one can see that this requirement is quite relaxed.

We can extend the analysis to the case where the capacitor is not periodically reset. We begin this analysis from eq. 4.11; since the capacitor is not reset, the initial condition on the capacitor on each integration period is not zero. At the end of each integration period, we can write:

$$V_{gm}(nT_p + T_{int}) = e^{-\frac{T_{int}}{R_{out}C_{H1}}} V_{gm}((n-1)T_p) + \frac{G_m}{C_{H1}} \int_0^{T_{int}} e^{-\frac{1}{R_{out}C_{H1}}(T_{int}-\tau)} V_{in}(nT_p + \tau) d\tau \quad (4.18)$$

That is, the initial condition for the  $C_{H1}$  on each integration period, is equal to the final value from the previous integration period. Let  $v[n]$  be defined as in eq. 4.9, i.e. let  $v[n]$  be the output of the embedded discrete-time integrator, then:

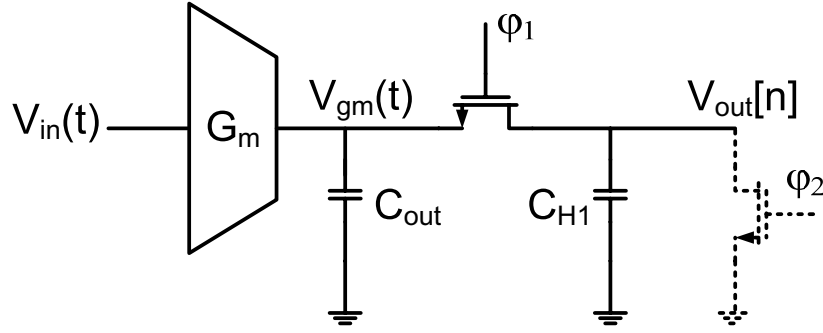
$$v[n] = e^{-\frac{T_{int}}{\tau}} v[n-1] + q_{in}[n] \quad (4.19)$$

Since the factor  $e^{-\frac{T_{int}}{\tau}}$  is less than one, the output resistance of the transconductor causes the embedded discrete-time integrator to become lossy.

DC gain is a frequently-used performance metric for an integrator. An ideal integrator has an infinite DC gain. If we used the numbers specified in the above example, then the DC gain of this discrete-time integrator is equal to 40 dB.

#### 4.2.2. Impact of $G_m$ Output Capacitance

We start the analysis by building up from the derivation on section 4.1. At the beginning of each sampling period,  $C_{H1}$  is empty due to the reset phase on  $\phi_2$ . The parasitic output capacitance  $C_{out}$



**Figure 4-8.** Impact of transconductor output capacitance

is never reseted, and thus it holds some charge corresponding to the output voltage from the last sampling period. Let  $q_o[n]$  and  $q_{H1}[n]$  be the charge stored in the parasitic capacitance  $C_{out}$  and hold capacitor  $C_{H1}$  (respectively) at the end of integration period  $\phi_1$ . Through charge conservation, we can write:

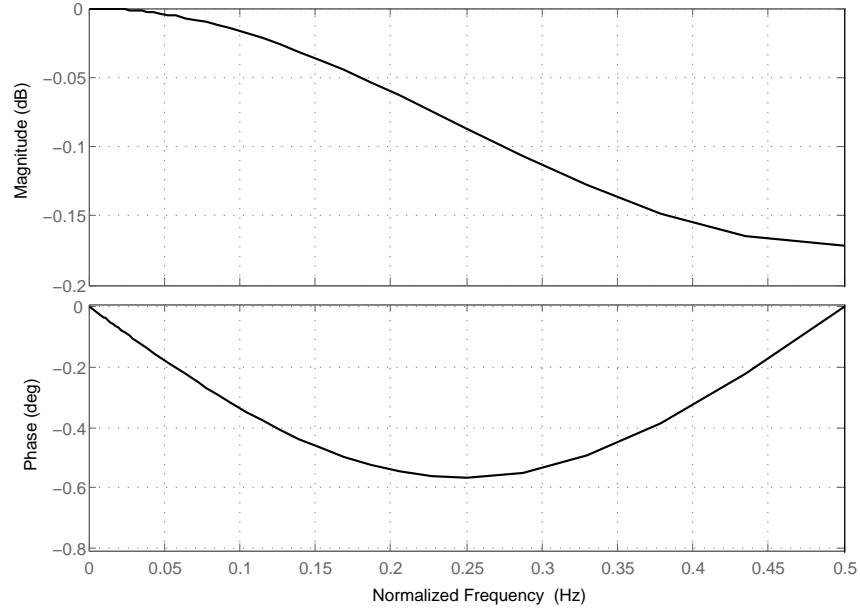
$$q_{H1}[n] + q_o[n] = q_o[n-1] + q_{in}[n] \quad (4.20)$$

where  $q_{in}[n]$  is defined as in eq. 4.1. The term  $q_{H1}[n-1]$  is excluded from eq. 4.20, because  $C_{H1}$  is periodically reset. Assuming complete settling is achieved during the integration period  $\phi_1$ , the voltage on the two capacitors will be the same, i.e.

$$C_{H1}q_{H1}[n] = C_{out}q_o[n] \quad (4.21)$$

We can combine eq. 4.20 with the relation given in eq. 4.21,

$$\frac{C_{H1} + C_{out}}{C_{H1}}q_{H1}[n] = \frac{C_{out}}{C_{H1}}q_{H1}[n-1] + q_{in}[n] \quad (4.22)$$



**Figure 4-9.** Frequency response distortion due to  $C_{out}$

Taking the z-transform of eq. 4.22, we get:

$$\frac{Q_{H1}(z)}{Q_{in}(z)} = \frac{1}{\frac{C_{H1} + C_{out}}{C_{H1}} - \frac{C_{out}}{C_{H1}} z^{-1}} \quad (4.23)$$

As a check; when  $C_{out} = 0$ , eq. 4.23 degenerates to a constant 1, which is expected, since in that case all incoming charge  $q_{in}$  is stored within  $C_{H1}$ . We see that there is a slight memory effect ( $q_{H1}[n-1]$  term) in the formation of new output samples. This is simply due to the fact that  $C_{out}$  is never reseted, and therefore it keeps some part of all past samples within it. Figure 4-9 displays

the magnitude and phase response of the transfer function in eq. 4.23, when  $\frac{C_{out}}{C_{H1}} = 0.01$ .

Since the output of the sampler is read in between  $\phi_1$  and  $\phi_2$ , we can write  $V_{out}[n]$  as:

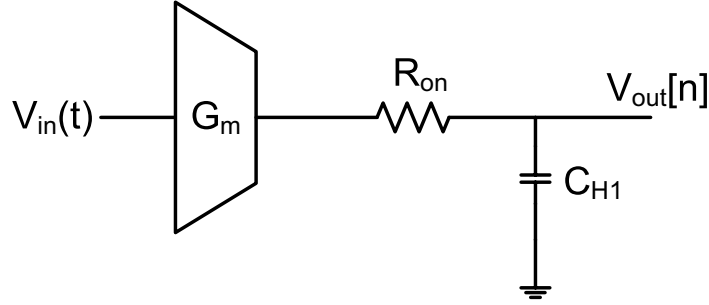
$$V_{out}[n] = \frac{q_{H1}[n]}{C_{H1}} \quad (4.24)$$

The analysis for the case when  $C_{H1}$  is not periodically reset is markedly different. In this case, both  $C_{H1}$  and  $C_{out}$  continuously integrate the input samples. On each integrating period, the input charge is distributed between  $C_{H1}$  and  $C_{out}$ , such that the voltage of the two capacitors remains the same, i.e. eq. 4.21 still holds. The net effect is that the incoming charge is integrated with a larger capacitor, of size  $C_{H1} + C_{out}$ , instead of  $C_{H1}$ . If we narrow down the definition of  $q_{in}[n]$  to be the total charge delivered to capacitor  $C_{H1}$  only, then the presence of output capacitance

$C_{out}$  effectively decreases the sampling gain by a factor of  $\frac{C_{H1}}{C_{H1} + C_{out}}$ . This gain reduction is due to the simple fact that part of the stored charge resides in  $C_{out}$ . The rest of the analysis is identical to the ideal non-reset case. The output voltage is read as:

$$V_{out}[n] = \frac{v[n]}{C_{H1}} \quad (4.25)$$

where  $v[n]$  is defined as in eq. 4.8.



**Figure 4-10.** MOS switch on resistance with ideal transconductor

### 4.3. Impact of MOS Switch On Resistance

When the transconductor is ideal, i.e. it has no output parasitics, the MOS switch on-resistance has no impact towards the performance of the sampler circuit. This is because all the current that is coming out of the transconductor can only go to one branch, and eventually it will be sunk inside  $C_{H1}$ . Therefore the integrating function that exists in this sampler circuit remains as in the ideal case.

#### 4.3.1. MOS $R_{on}$ with Transconductor $R_{out}$

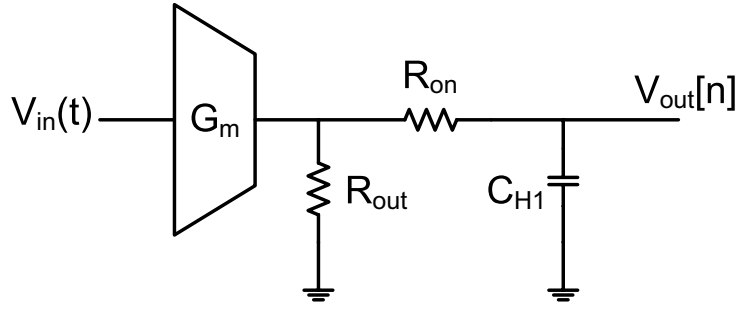
Using KCL, we can write the differential equation describing the circuit in figure 4-11 as:

$$G_m V_{in}(t) = \frac{V_{H1}(t) + i_{H1}(t)R_{on}}{R_{out}} + C_{H1} \frac{dV_{H1}(t)}{dt} \quad (4.26)$$

where  $i_{H1}(t)$  and  $V_{H1}(t)$  are the current and the voltage across the capacitor  $C_{H1}$ , respectively.

We can rewrite the equation above as follows:

$$\frac{dV_{H1}(t)}{dt} = \frac{1}{\left(\frac{R_{out} + R_{on}}{R_{out}}\right)} \left[ \frac{G_m V_{in}(t)}{C_{H1}} - \frac{V_{H1}(t)}{R_{out} C_{H1}} \right] \quad (4.27)$$



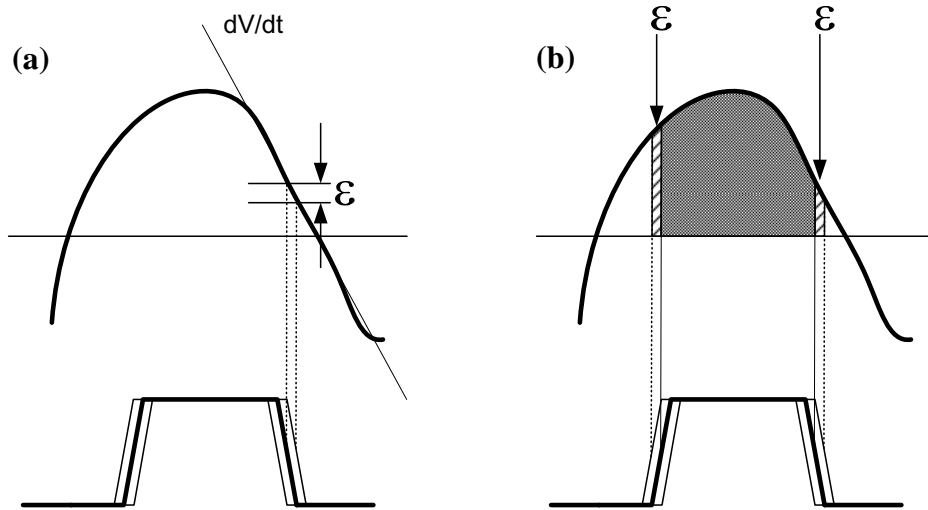
**Figure 4-11.** MOS switch on resistance combined with transconductor output resistance

With the exception of the  $\frac{R_{out} + R_{on}}{R_{out}}$  factor, the differential equation describing this system is exactly identical as the one which describes the system without the MOS switch resistance (section 4.2.1). We can thus use the derivation and analysis developed in section 4.2.1 to explain the behavior of this particular circuit.

Using the same definition as in previous sections, we can rewrite  $q_{in}[n]$  to reflect the impact of the MOS switch resistance;

$$q_{in}[n] = \frac{G_m R_{out}}{R_{out} + R_{on}} \int_0^{T_{int}} e^{-\frac{1}{(R_{out} + R_{on})C_{H1}}(T_{int} - \tau)} V_{in}(nT_p + \tau) d\tau \quad (4.28)$$

Intuitively, the  $\frac{R_{out}}{R_{out} + R_{on}}$  multiplier is present because only that part of the current is sunk to the capacitor  $C_{H1}$ , with the rest being dissipated by the resistor  $R_{out}$ . Furthermore, the charge inside  $C_{H1}$  is now continuously decayed by both  $R_{out}$  and  $R_{on}$ , since both resistors are in series with each other and with the capacitor  $C_{H1}$ .



**Figure 4-12.** Impact of clock jitter to sampling  
 (a) Voltage sampling, (b) Windowed charge-sampling

Noting the parallel between this system and the one without MOS switch resistance, the qualitative impact of the MOS switch resistance is exactly identical to the impact of finite output resistance of the transconductor; e.g. reduced alias rejection and a lossy discrete-time integrator.

#### 4.4. Sensitivity to Clock Jitter

In this section, we will analyze the impact of clock jitter in a conventional voltage-sampling track-and-hold circuit. We will then make a comparison with our proposed windowed-charge-sampling circuit.

Figure 4-12(a) shows an illustration of the impact of sampling clock jitter in a track-and-hold circuit. The sampling instant of a track-and-hold circuit is determined by the high-to-low transition of the sampling clock. Thus, when this transition deviates from the ideal time instant, the input signal would not be sampled at the right time position. If the input is time-varying, then the temporal deviation of the sampling instant would result in a net voltage error, denoted  $\epsilon$  in figure 4-12(a).

We can estimate the relation between timing error and the resulting voltage error in the voltage-sampling process, using a first-order linear approximation of the input signal [6]. Assuming that the time deviation is small enough, we can take the derivative of the input signal at the *ideal* sampling instant, and use that value as the conversion factor in relating timing error to voltage error. In other words, suppose the clock jitter at time  $nT_p$  is denoted by  $\Delta t$ , then the resulting voltage

error would be  $\Delta t \frac{dV}{dt} \Big|_{t=nT_p}$ .

When a track-and-hold circuit precedes a data conversion system, the resulting voltage error shown above has to be smaller than the quantization noise level. This is done so that the error resulting from timing uncertainty, will not limit the dynamic range performance of the system. For a B bits data converter sampled at  $f_p$ , we can calculate the jitter requirement for this system given a sinusoidal input.

$$\begin{aligned} \Delta t \frac{d}{dt} \left[ \frac{A_{FS}}{2} \cos(2\pi f_{max} t) \right] &\leq \frac{1}{2} \frac{A_{FS}}{2^B} \\ \Delta t \left[ \frac{A_{FS}}{2} 2\pi f_{max} \sin(2\pi f_{max} t) \right] &\leq \frac{1}{2} \frac{A_{FS}}{2^B} \end{aligned} \quad (4.29)$$

$A_{FS}$  is the peak-to-peak full-scale range of the system, and  $f_{max}$  is the maximum input frequency. The maximum frequency in this case is,  $f_p/2$ . Therefore the worst case voltage error can be calculated to be  $\Delta t \frac{A_{FS}}{2} \pi f_p$ . The requirement on the clock jitter is therefore:

$$\Delta t \leq \frac{1}{\pi f_p 2^B} \quad (4.30)$$

Similarly, we can also calculate the jitter requirement on the windowed-charge-sampling circuit. In this circuit, the timing uncertainty effects the *start and the end time of the integration period* (figure 4-12(b)). Assuming that the clock jitter only incurs small time deviation, we can write the resulting sampling error at time  $t = nT_p$  to be

$$\varepsilon = \Delta t_{start} G_m V_{in}(nT_p) + \Delta t_{end} G_m V_{in}(nT_p + T_{int}) \quad (4.31)$$

The value  $\varepsilon$  above corresponds to the shaded area to the left and right of the gray area in figure 4-12(b). In the worst case, the input signal is a constant DC at the maximum voltage level. The resulting jitter requirement is:

$$(\Delta t_{start} + \Delta t_{end}) G_m \frac{A_{FS}}{2} \leq \frac{1}{2} \frac{G_m A_{FS} T_{int}}{2^B} \quad (4.32)$$

$$(\Delta t_{start} + \Delta t_{end}) \leq \frac{T_p}{T_{int} f_p} \frac{1}{2^B} \quad (4.33)$$

where  $f_p = \frac{1}{T_p}$ .

We see that the worst case jitter for a windowed-charge-sampler circuit is comparable with a track-and-hold circuit; with the difference being only of a constant factor.

The analysis shown above assumes a worst case condition. For sinusoid input signal, we can write eq. 4.31 as:

$$\varepsilon = \Delta t_{start} G_m \frac{A_{FS}}{2} \cos(2\pi f(nT_p)) + \Delta t_{end} G_m \frac{A_{FS}}{2} \cos(2\pi f(T_p + T_{int})) \quad (4.34)$$

We see that depending on the frequency and phase of input signal the resulting error due to jitter would likely be smaller than what is shown in eq. 4.33. Nevertheless, eq. 4.33 serves as a good upper bound for the error.

# Chapter 5

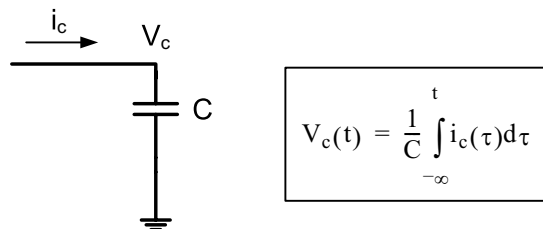
## *N-path Bandpass $\Sigma\Delta$ Loop Filter*

Realizing a bandpass  $\Sigma\Delta$  A/D to operate at radio frequencies has so far been significantly limited by the difficulty of implementing a loop filter that can operate at a high frequency. In this chapter we will elaborate on what limits the design of high-frequency filters using conventional structures as well as propose an alternative filter structure that can circumvent this limitation.

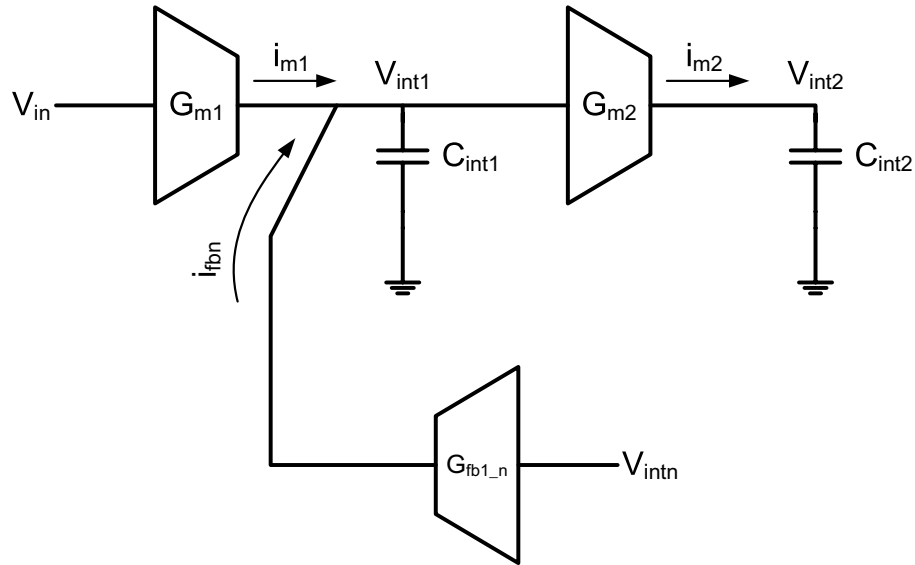
### 5.1. Challenges in High-Frequency Filters

A key part to the proposed RF bandpass  $\Sigma\Delta$  A/D is the modulator loop filter. The design of the loop filter is challenging, because it has to run at a very high frequency. In this section, we argue that the difficulty in implementing such a filter, both in continuous-time and discrete-time, stems from the lack of a good linear amplifier that can operate at a high frequency.

From linear system theory, we know that a general filter function can be entirely realized by using only interconnected integrators, with a combination of feedforward and feedback paths [19]. In the world of integrated circuits, a capacitor is actually a perfect integrator. A capacitor integrates



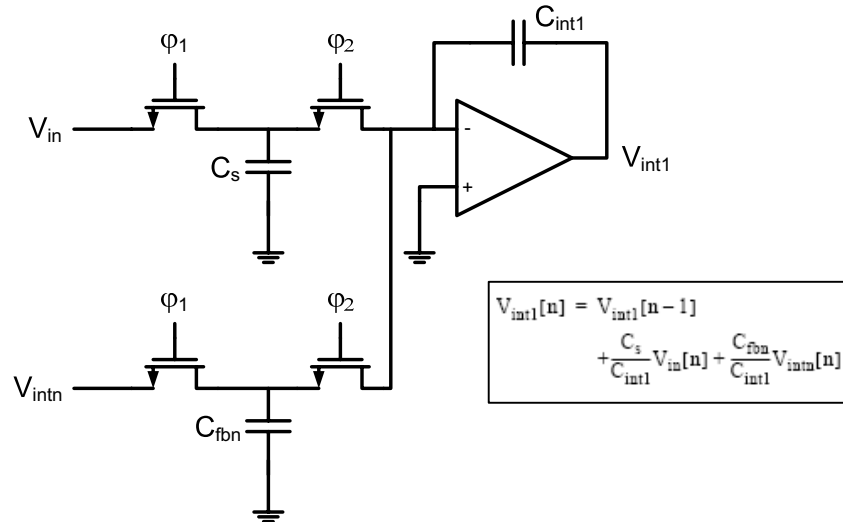
**Figure 5-1.** Capacitor is an integrator



**Figure 5-2.** Continuous-time filter structure

an input current and generates its output in the form of a voltage across itself. In implementing a filter in integrated circuits, the problem actually arises when several of these capacitors/integrators are to be linked together, or when a feedback path is needed. In both cases, an active linear amplification block is necessary. If the filter is to run at a high frequency, than the amplifier would also need to be able to run at a high frequency. For continuous-time filters, typically this amplifier is needed to perform a voltage-to-current conversion, so that the output (voltage) of one integrator can be used as an input (current) for another integrator.

Figure 5-2 shows a section of a continuous-time filter built using transconductors and capacitors. The capacitor is used simply as a current integrator. A transconductor is used to implement a feed-forward path, performing  $V$ -to- $I$  conversion on the input voltage, and also to implement feedback and interconnection paths, converting the output voltage of one integrating capacitor to a current to be fed to another integrating capacitor. This filter structure is called a  $G_m$ - $C$  filter. One can argue that a similar operation takes place in an opamp-RC filter structure [20]. Instead of a



**Figure 5-3.** Sampled-data domain filter structure

transconductor, the combination of a resistor and the virtual ground of an op-amp provides the active element necessary for voltage-to-current conversion.

In a switched-capacitor filter, a capacitor also acts as the necessary discrete-time integrator. Figure 5-3 shows an example realization of a discrete-time integrator with one op-amp. As in the continuous-time case, the input of this integrator is a linear combination of the input signal (feed-forward path) as well as the output of other integrators within the filter (interconnect and feedback paths). In this sampled-data realization, the input signal is represented as a *charge packet*, instead of a current or voltage signal. On  $\phi_1$ , the input voltage  $V_{in}$  is sampled, and its value is stored in the form of electrical charge inside the sampling capacitor  $C_s$ . Similarly, the output voltage of integrator  $n$ , denoted  $V_{intn}$ , is also sampled and stored in sampling capacitor  $C_{fbn}$ . These two charge packets act as an input to the discrete-time integrating capacitor  $C_{int}$ . As the circuit connections are reconfigured during  $\phi_2$ , the two sampling capacitors are discharged, and the value of the two input charge packets are added to  $C_{int}$ .  $C_{int}$  is never reset; it keeps a running sum of its inputs, and thus a discrete-time integrator function is realized.

In a switched-capacitor filter, an amplifier is needed to move charge packets from the sampling capacitors to the integrating capacitor. This is done by providing a virtual ground at the input of the op-amp, which forces the sampling capacitors to discharge and move their charge packets to the integrating capacitor.

In the paragraphs above, we discussed various filter topologies that are commonly encountered in today's integrated circuits. The topologies discussed are  $G_m$ -C and opamp-RC for continuous-time filters and a discrete-time switched-capacitor filter. Common to all these realization structures is the need for a linear amplifier, such as a transconductor or an op-amp.

We argue that this requirement is the fundamental bottleneck in implementing a high-frequency filter. Simply put, it is very difficult to implement a high-frequency amplifier with sufficient gain and linearity. Op-amps in today's CMOS technologies are limited to the range of 10 to 100 of MHz. Open-loop amplifiers can reach higher frequencies, however the linearity of such amplifiers are usually quite poor. Even when such high-frequency amplifier can be built, it usually consumes a lot of power and area.

In this and the following chapter, we will discuss two techniques that would enable us to make a high-order bandpass filter with the limitation of current CMOS technologies, namely limited gain and limited bandwidth. The key message from this section is that in order for the new filter structure to operate at a high frequency, it has to avoid the need for a high-frequency linear amplifier whenever possible.

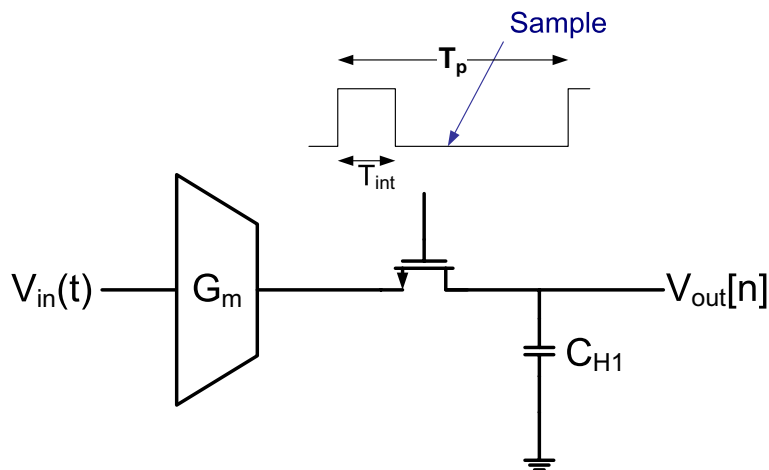
## **5.2. N-path Discrete-Time Bandpass Filters**

A discrete-time filter holds several advantages over a continuous-time filter. The critical frequencies of a discrete-time filter are usually constant fractions of the sampling frequency; where these

fractions are typically formed by ratios of capacitances in the circuit. In today's integrated circuits, both clock frequencies and ratios of capacitances are parameters that can be very well-controlled. Thus, the accuracy of the filter's critical frequencies can also be very good. This would eliminate the need for a complex tuning loop that are commonly needed in a continuous-time filter. Furthermore, changing the frequency response can be easily accomplished by changing the clock frequency, or by switching in/out additional capacitors.

There are two main disadvantages of a discrete-time filter, both stems from the inherent sampling operation that is needed in such a system. First, an anti-aliasing filter is needed to prevent aliases of the input signal to corrupt the band of interest. Second, a sample-and-hold circuit is needed. The performance of this sample-and-hold circuit is critical, as all impairments generated by this circuit will be propagated throughout the system and can not be reversed. This usually results in a high power consumption or a large circuit area for the front-end sample-and-hold circuit. These two disadvantages in some cases can make continuous-time filters more power and area efficient, despite the disadvantages mentioned in the above paragraph. However, in systems where a sampler is absolutely necessary, such as a filter preceding an A/D, then the cost of having a front-end becomes rather irrelevant.

In designing a high-frequency bandpass filter, the windowed-charge-sampler circuit, introduced in chapter three, actually provides a good starting point. The circuit provides an inherent partial anti-aliasing filter before the sampling process. It also provides an idle time period, where the charge inside the sampling capacitor is held constant and ready to be processed in a sampled-data domain. And, as an added bonus, the circuit can be easily modified to implement a discrete-time integrator as well.

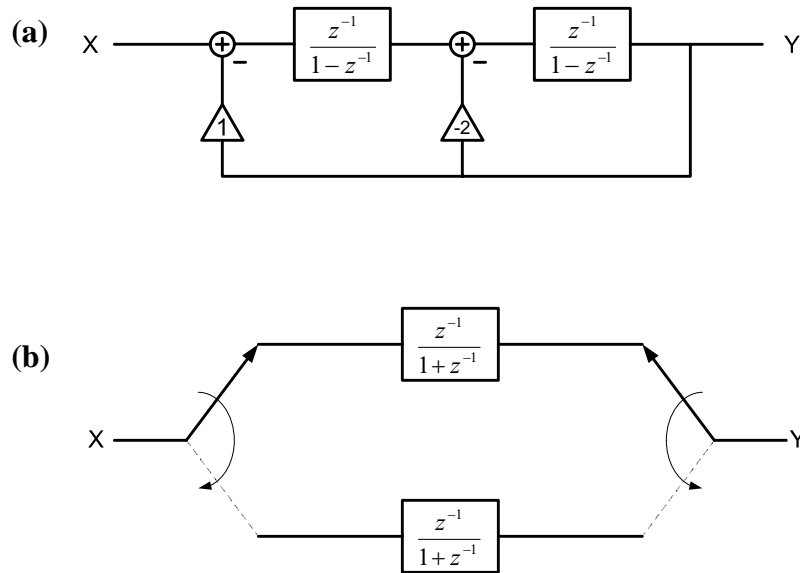


**Figure 5-4.** Windowed-charge-sampler with embedded integrator

In this section, we will discuss how we can use the windowed-charge-sampler as a building block in implementing a high-frequency bandpass filter. The main objective of the design is two folds. First, it should avoid the use of additional active amplifiers besides the transconductor needed to drive the sampler circuit. And second, it should take advantage of the inherent discrete-time integrator built into the sampler circuit.

We found that an  $N$ -path filter structure fits this requirement quite well. An  $N$ -path filter is a discrete-time filter built using  $N$  parallel and identical filter paths that are time-interleaved. If  $H_p(z)$  is the transfer-function of the constituent filters for each path, then the resulting transfer function of the  $N$ -path filter is  $H_p(z^N)$ . The key idea here is that the  $N$ -path filter enables a  $z^N$  to  $z$  transformation in the original filter's transfer function. By doing so, we hope to be able to decompose a bandpass type filter into a simpler terms that can be more easily implemented using the available building blocks.

In the following two subsections we will discuss a two-path and a four-path bandpass filters. As it has been discussed in earlier chapters, the goal is to implement a bandpass filter with center fre-



**Figure 5-5.** Discrete-time resonator implementations  
 (a) Direct form - using feedback, (b) N-path

quency at  $f_s/4$ , where  $f_s$  is the sampling clock frequency. When this filter is put in a  $\Sigma\Delta$  loop, the expected response should have a noise transfer function notch at  $f_s/4$ .

### 5.2.1. Two-path Bandpass Filter

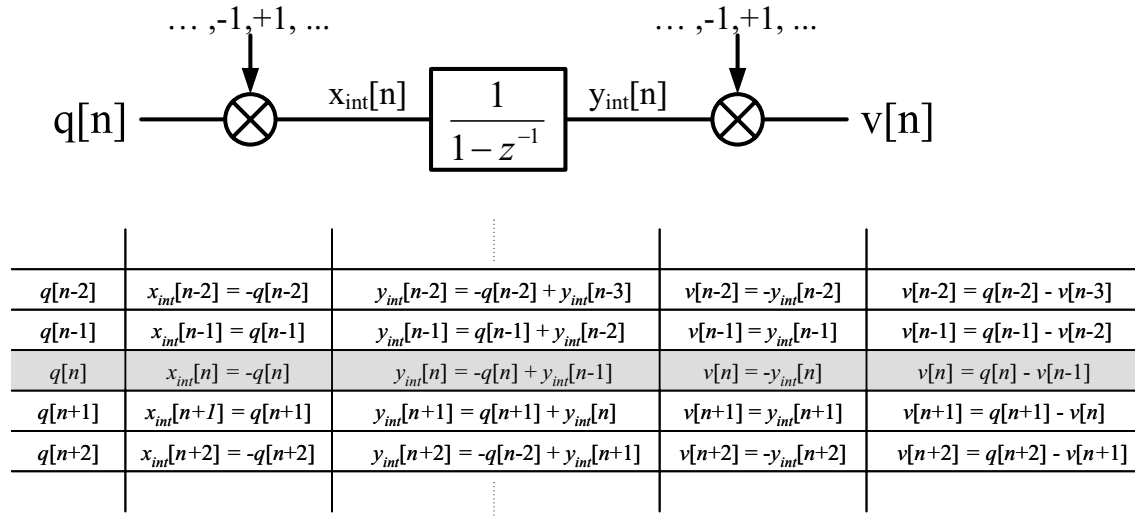
The first filter we would like to design is a discrete-time resonator. The transfer function is given below:

$$H_2(z) = \frac{1}{1 + z^{-2}} \quad (5.1)$$

The resonator has poles at  $\pm j$ , which realizes a bandpass filter with a center frequency at  $f_s/4$ .

When the filter is put inside a  $\Sigma\Delta$  modulator loop, the resulting STF and NTF is given below:

$$\begin{aligned} STF &= 1 \\ NTF &= 1 + z^{-2} \end{aligned} \quad (5.2)$$



**Figure 5-6.** Two-path filter using integrators

We can time-interleave the above transfer function using two identical paths. The resulting transfer function of each path is therefore:

$$H_{p2}(z) = \frac{1}{1 + z^{-1}} \quad (5.3)$$

We can write the difference equation for the same filter:

$$v[n] = q[n] - v[n - 1] \quad (5.4)$$

where  $q[n]$  and  $v[n]$  are the input and the output of the filter respectively. Recall that we wish to implement this transfer function using discrete-time integrators as building blocks. As a reference, the difference equation for a discrete-time integrator is given below:

$$y_{int}[n] = x_{int}[n] + y_{int}[n - 1] \quad (5.5)$$

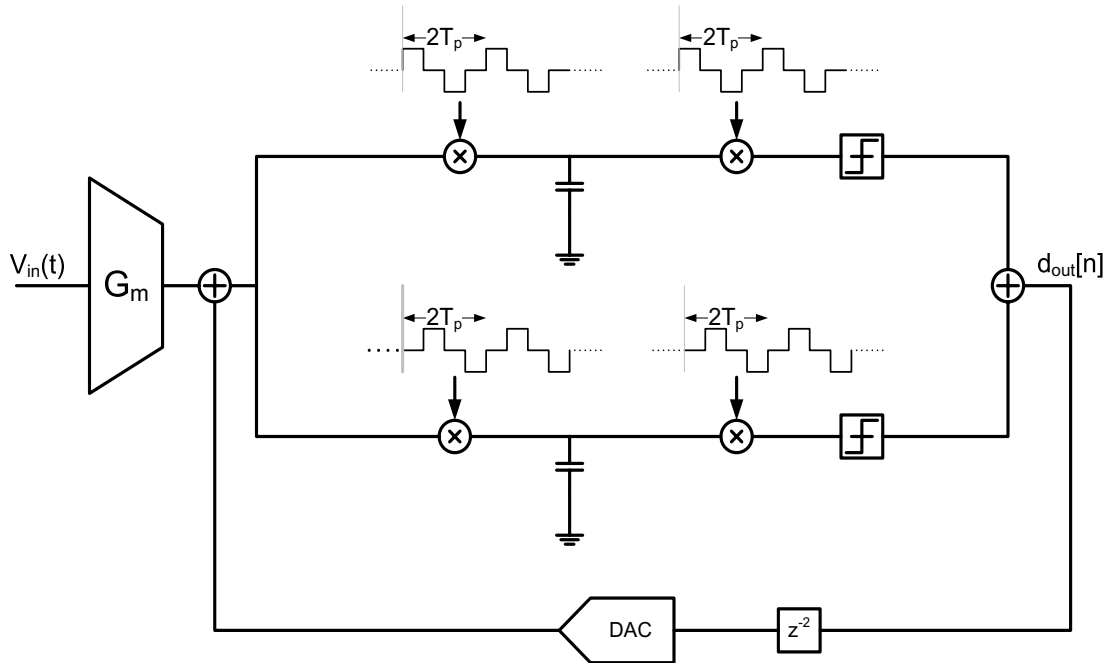
where  $x_{int}[n]$  is the input to the discrete-time integrator, and  $y_{int}[n]$  is the output. The only difference between the two difference equation is the sign in front of the previous output/memory term.

To obtain the desired transfer function from a discrete-time integrator, we start by re-writing eq. 5.4 as:

$$-v[n] = -q[n] + v[n-1] \quad (5.6)$$

Let  $-q[n]$  to be the input to a discrete-time integrator, i.e.  $x_{int}[n] = -q[n]$ . Then the output of the integrator is the negative of the desired response, i.e.  $y_{int}[n] = -v[n]$ . In the next sample period, we would like to form  $v[n+1] = q[n+1] - v[n]$ . If we let  $x_{int}[n+1] = q[n+1]$ , then  $v[n+1] = y_{int}[n+1]$ , since  $-v[n] = y_{int}[n]$ . In other words, in sample period  $n$ , we can obtain the desired output by multiplying the input and output of the integrator by a factor of -1. However at sample period  $n+1$ , we can input the new sample and read from the integrator as is. This argument suggest that we can realize the desired transfer function simply by multiplying the input and output of a discrete time integrator by a periodic sequence of -1 and +1. Figure 5-6 shows a few time iterations of using this process to show that modulating by a -1, +1 sequence does produce the correct output.

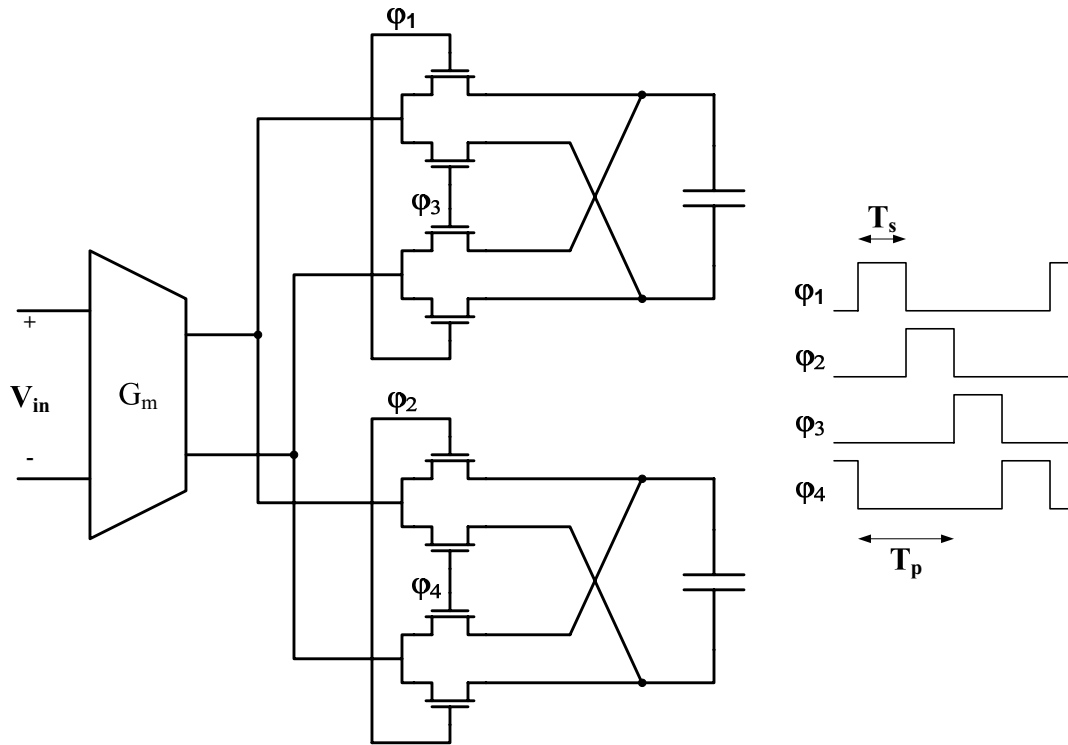
Intuitively, the above operation combines frequency modulation/demodulation and the frequency response of an integrator to synthesize the desired filter. Both filters are single-pole IIR filters, with very similar frequency responses. The only difference between the two filters, are the location of the single pole. An integrator has a pole at  $z = 1$ , while the desired filter has a pole at



**Figure 5-7.** Bandpass  $\Sigma\Delta$  A/D with a two-path filter

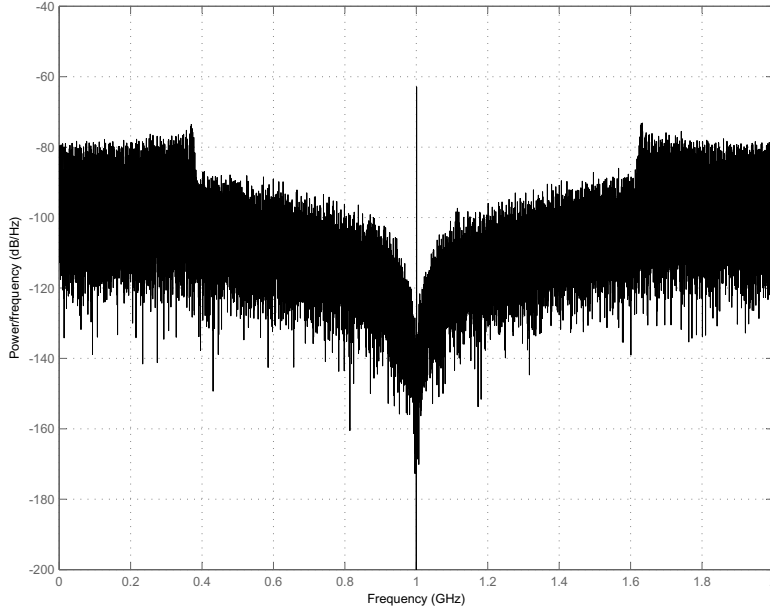
$z = -1$ . In this implementation, instead of shifting the filter's pole location, we shift the input signal's frequency. One can easily show that both operations are in fact mathematically identical.

We can put this filter inside a  $\Sigma\Delta$  loop, as shown in figure 5-7. The sampling time of the A/D is denoted  $T_s$ . Since the two paths are time-interleaved, the sampling rate of each of the path is denoted  $T_p$ , where  $T_p = 2T_s$ . The time-interleaving function between the two-path is implemented using the multipliers shown in front of each of the capacitors. This multipliers also modulates each path's input by a  $-1,+1$  sequence. The two operations, time-interleaving and modulation, result in the sine-like modulation signal shown in the figure. The transconductor, multipliers, and capacitors can be implemented as shown in figure 5-8. Depending on the timing signal, the input current can be routed to the top or bottom capacitor, and each can be routed as is, or in inverted form using two cross-coupled differential pairs.



**Figure 5-8.** Front-end for a two-path bandpass  $\Sigma\Delta$  A/D

Recall that a demodulation by an identical  $-1,+1$  sequence is necessary to fully synthesize the desired filter's response. When the filter is put in a  $\Sigma\Delta$  loop, the output of the filter would be quantized with a single-bit quantizer. As such, there's some freedom as to how the demodulation operation would be implemented. Figure 5-7 shows one possibility. In this case, one quantizer is used on each path; in order to lower the quantizer's operating frequency. The demodulation process, and the signal recombination from the two paths can then be implemented in the digital domain.



**Figure 5-9.** Simulation result of a bandpass  $\Sigma\Delta$  A/D with 2-path filter (Sampling frequency  $f_s$  is set to 4 GHz, with signal at 1.001 GHz)

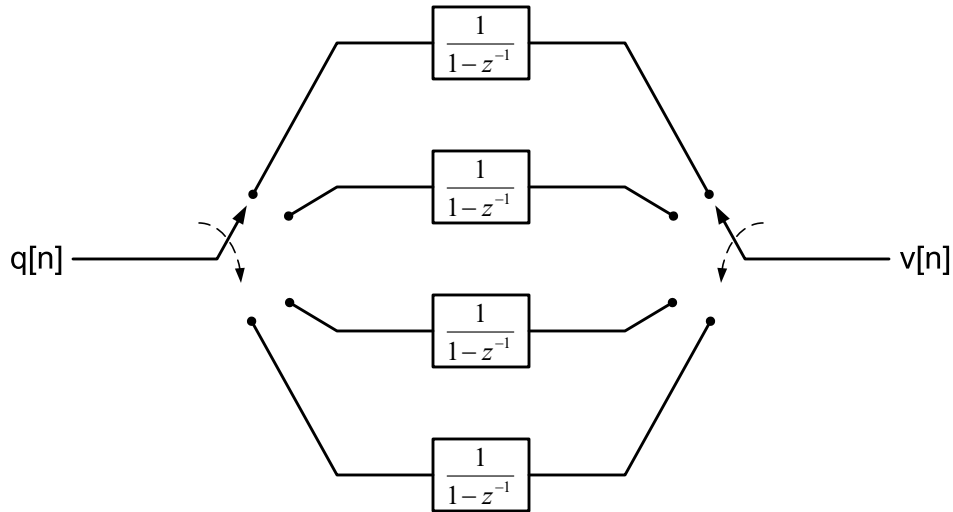
### 5.2.2. Four-path Bandpass Filter

In order to achieve a bandpass-type frequency response with center frequency at  $f_s/4$ , we needed two poles located at  $z = \pm j$ . The structure proposed in the last subsection generates those two poles exactly. As an alternative, we can also realize the following transfer function:

$$H_4(z) = \frac{1}{1 - z^{-4}} \quad (5.7)$$

which has poles located at  $z = \pm j$  and  $z = \pm 1$ . The advantage of using this transfer function, is that it can simply be implemented using 4 time-interleaved integrators, without the need of any modulators. Using a  $z^4$  to  $z$  transformation, the resulting filter for each path is simply

$$H_{p4}(z) = \frac{1}{1 - z^{-1}}, \text{ which is exactly the transfer function of a discrete-time integrator.}$$



**Figure 5-10.** Four-path bandpass filter

When this filter is put inside a  $\Sigma\Delta$  loop, the resulting STF and NTF is shown below:

$$\begin{aligned}
 STF &= 1 \\
 NTF &= 1 - z^{-4}
 \end{aligned}
 \tag{5.8}$$

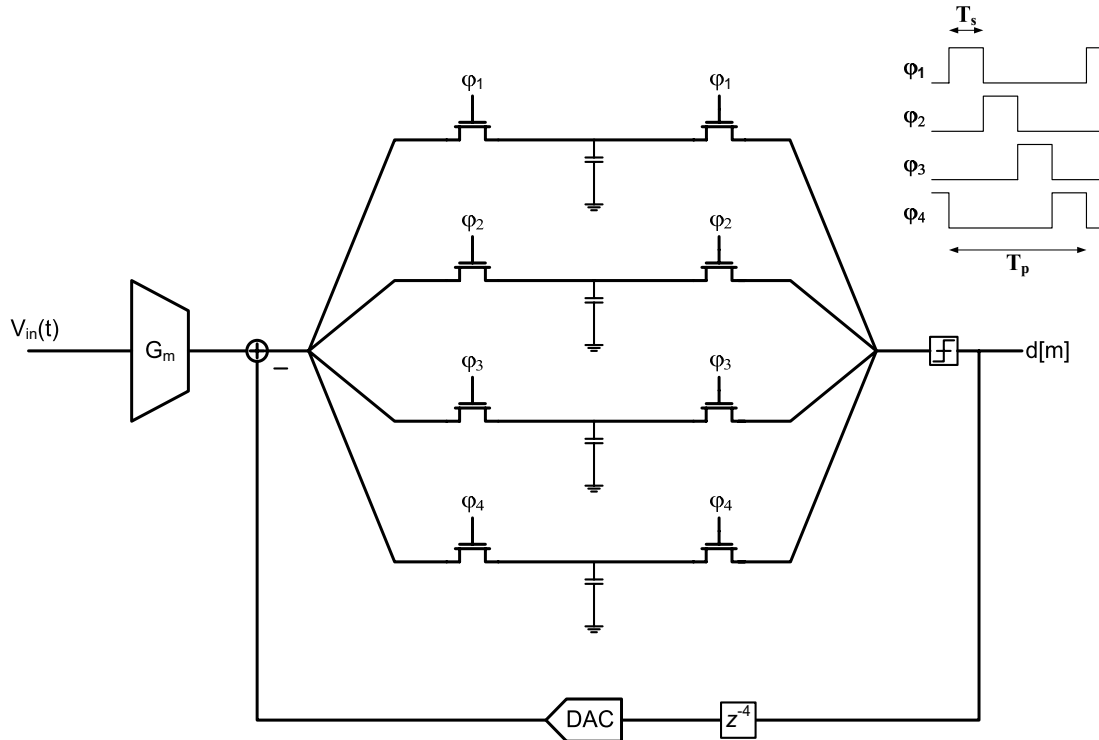
The noise transfer function has zeros exactly at the four pole locations of the original filter; e.g. at  $z = \pm j$  and  $z = \pm 1$ . Thus the desired quantization noise notch at  $f_s/4$  is achieved.

Figure 5-11 displays the four-path bandpass filter inside a bandpass  $\Sigma\Delta$  A/D loop.

The sampling period of the A/D is  $T_s$ . Since the filter is time-interleaved into four paths, then the sampling period of each path is  $T_p = 4T_s$ . On each path, the input current is integrated for a period of  $T_s = T_p/4$ , therefore the duty-cycle of the windowed-charge-integrator sampler is 25%.

The output of the filter is quantized after the signal is de-interleaved; thus it has to run with a period of  $T_s$ .

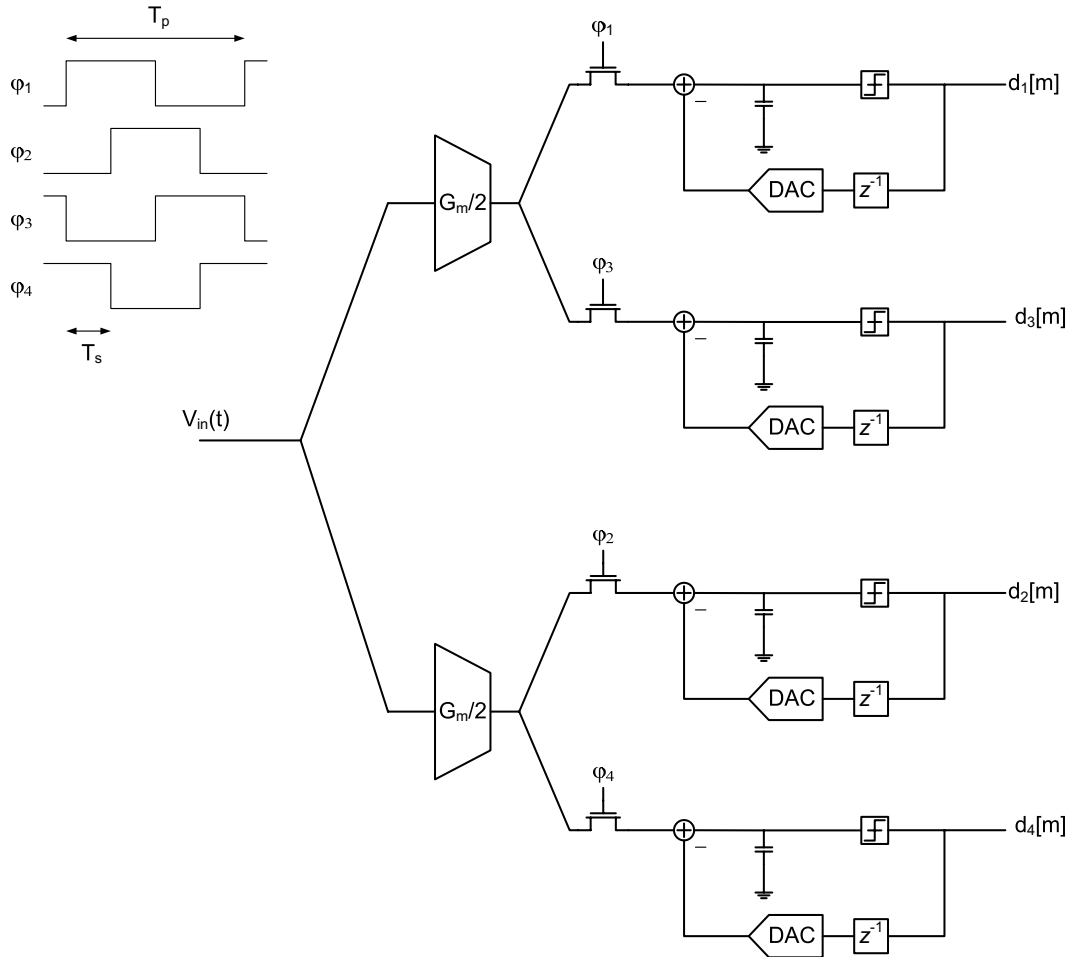
There are a number of variations or modifications that can be made to the realization structure shown in figure 5-11; all done while maintaining correct circuit function. Most of the modifica-



**Figure 5-11.** Bandpass  $\Sigma\Delta$  A/D with a four-path filter

tions relies on time-multiplexing or time-interleaving between the different paths of the filter. The goal of the modifications is usually to lower the sampling rate, or to reduce the circuit area.

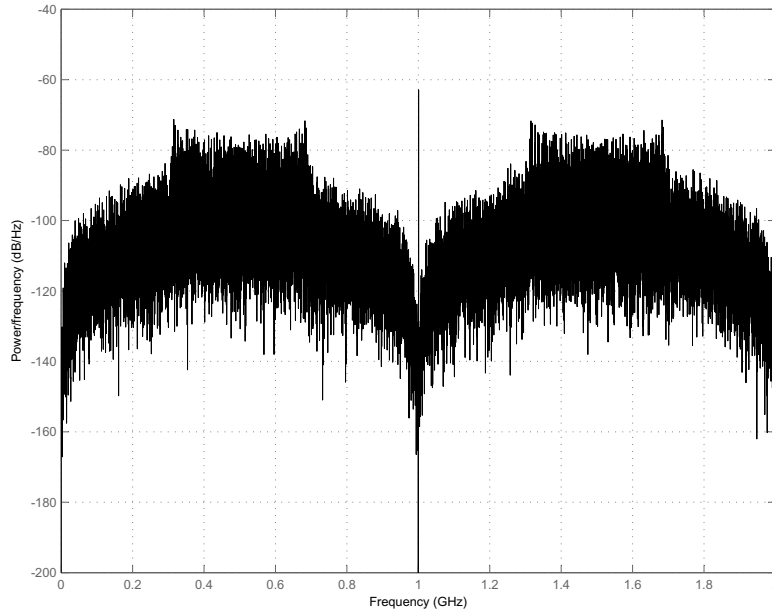
Figure 5-12 shows an alternative realization structure for the four-path bandpass  $\Sigma\Delta$  A/D. There are three main modifications made in this realization. First the locations of the de-interleaver and the quantizer are switched. Four quantizers are used to sample the output of the four paths. The signal de-interleaving can then be done digitally (not shown). Second, the  $\Sigma\Delta$  feedback signal is also split into four paths. This is possible since the delay on the original feedback path is exactly four, and therefore the feedback signal from each path can be locally generated on each path. Third, we split the transconductor into two, and modified the timing of the input transconductor. This modifications accommodate a 50% duty cycle in the sampler circuit. Note that the sampling



**Figure 5-12.** Modified bandpass  $\Sigma\Delta$  A/D with four-path filter

gain on each of the path remain constant,  $G_m T_s$ , and furthermore each transconductor is supplying current to one and only one capacitor at all time.

There are several advantages of the implementation in figure 5-12. First, by time-interleaving the quantizer and the feedback DAC, we can lower the operating frequencies of these two blocks. Since the quantizer and the DAC comprises of a comparator, and a single-bit DAC, the penalties of this parallelization scheme is relatively small. The 50% duty cycle on the sampler circuit is desired since it provides a more comprehensive anti-aliasing filter with little cost (Chapter 4). The third advantage is not as obvious, but is equally important. By separating each of the path as much as possible, we minimized the number of common nodes in the circuit. This is very important to



**Figure 5-13.** Simulation result of a bandpass  $\Sigma\Delta$  A/D with 4-path filter (Sampling frequency  $f_s$  is set to 4 GHz, with signal at 1.001 GHz)

minimize cross-talk between the paths. Charge stored in parasitic capacitances at the common nodes creates a mechanism for signal from one path to leak to another. For example, in the realization in figure 5-11, the output of the transconductor and the input of the quantizer are common nodes for all four paths. The disadvantage of this parallelization is that all the four quantizers and DAC has to be matched reasonably well to avoid impairing the performance of the overall system.

### 5.3. General Discussions on Bandpass $\Sigma\Delta$ A/D Based on N-path Filters

In the last two sections we introduced two possible implementations for a bandpass filter with a center frequency at  $f_s/4$  using N-path filters. Ultimately, in order to implement a filter with this type of response, we need to generate two poles at  $z = \pm j$ .

We can generalize an N-path filter built using integrators as the path filter. For an N-path filter built using integrators, the composite filter will have a transfer function in the form of:

$$H_N(z) = \frac{1}{1 - z^{-N}} \quad (5.9)$$

The resulting filter has N radially equispaced roots on the unit circle starting at  $z = 1$ .

Using two paths, we can generate poles at  $z = \pm 1$ . The modulator and de-modulator in the two-path filter effectively rotates the location of the two poles to the desired location.

On the other hand, a four-path filter generates four poles at  $z = \pm 1$  and  $z = \pm j$ . Unnecessary poles are usually undesired, since extra poles typically result in extra power consumption and also larger silicon area. While the former is true in this realization structure, the power consumption between the two-path and four-path circuit is quite comparable. First, the number of switching per period between the two circuits are exactly the same; one high-to-low and low-to-high switching per period, per path. Second the total transconductance of the two circuits is also the same.

We will show in later chapters that, the extra poles in a four-path loop filter can actually be utilized to calibrate for path mismatches in the filter. More discussion on the effect of mismatches between paths will be given in the same chapter.

We can make some interesting remarks in comparing the four-path bandpass  $\Sigma\Delta$  A/D realization given in figure 5-11 and figure 5-12. One can show that both are mathematically identical; if we did not take into account the different responses of the two windowed-charge-sampler. However,

the later reveals some insight into the structure of bandpass  $\Sigma\Delta$  modulators built using N-path filters. The realization in figure 5-12 essentially comprises of four identical and independent low-pass  $\Sigma\Delta$  modulators. Thus, one could view this A/D as a time-interleaved A/D with four paths, where the sub-A/D's are simply made of lowpass  $\Sigma\Delta$  A/D's. It is important to note that the sub-A/D's are the one responsible in suppressing the quantization noise and generating the signal and noise transfer functions. Through time-interleaving, or equivalently through the N-path structure, we are able to replicate these frequency response N times around the z-plane unit circle. Thus in the case of the A/D in figure 5-12, since the sub-A/D is made out of single integrator, the A/D exhibits a first-order type noise shaping, e.g. 20 dB/decade roll-off. This is an important point, since it says that in order to alter the shape, not the location, of the noise transfer function, one would only need to alter the sub-A/D's loop filter.

This view point of the N-path bandpass  $\Sigma\Delta$  A/D as a time-interleaved A/D is correct and generalizable to most N-path filter structures. This viewpoint provides an alternative description of the system, and would actually assist us in understanding the effects of mismatches between paths of the time-interleaved A/D in later chapters.

For the remaining of this report, we will concentrate on the structure shown in figure 5-12. We chose this implementation structure because of all the advantages explained in this and the previous sections.

# Chapter 6

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## *Passive High-order Filters*

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In the previous chapter we discussed the challenges in implementing a high-frequency filter for use in an RF bandpass  $\Sigma\Delta$  A/D. We argued that the difficulty in implementing a high-frequency filter, originated from the necessity of having a linear amplifier that can operate at a high frequency.

We then introduced a discrete-time N-path filter that can partially circumvent the above limitation. By using time-interleaving and a discrete-time integrator built into the front-end windowed-charge-sampler circuit, we were able to implement a bandpass filter without requiring additional active amplifier elements. This technique essentially allowed us to put several equi-spaced poles around the unit circle in the z-domain. We accomplish this by using only discrete-time integrators as a building block.

In this chapter we would introduce another technique, which we would use to generate higher-order filters. In other words, this technique would allow us to put a number of poles **at the same location**. By using a higher-order filter, we can achieve better in-band quantization noise rejection, and therefore better achievable dynamic range. We can accomplish this without requiring any additional active amplifiers. The method presented is similar to the one used in [1].

From the last chapter, we have asserted that a bandpass  $\Sigma\Delta$  A/D can be realized by time-interleaving four lowpass  $\Sigma\Delta$  A/D's. In fact the lowpass A/D is what generates the noise shaping in the

architecture. Thus, in order to improve the in-band quantization noise shaping, it is sufficient to improve the design of the lowpass  $\Sigma\Delta$  A/D's.

In this chapter, we will focus on developing a second-order lowpass  $\Sigma\Delta$  A/D. The starting point would be the lowpass  $\Sigma\Delta$  A/D formed by the windowed-charge-sampling circuit as explained in the last chapter. Keep in mind that, at the end, the resulting filter structure will be used in a time-interleaved fashion, in order to generate a bandpass type response.

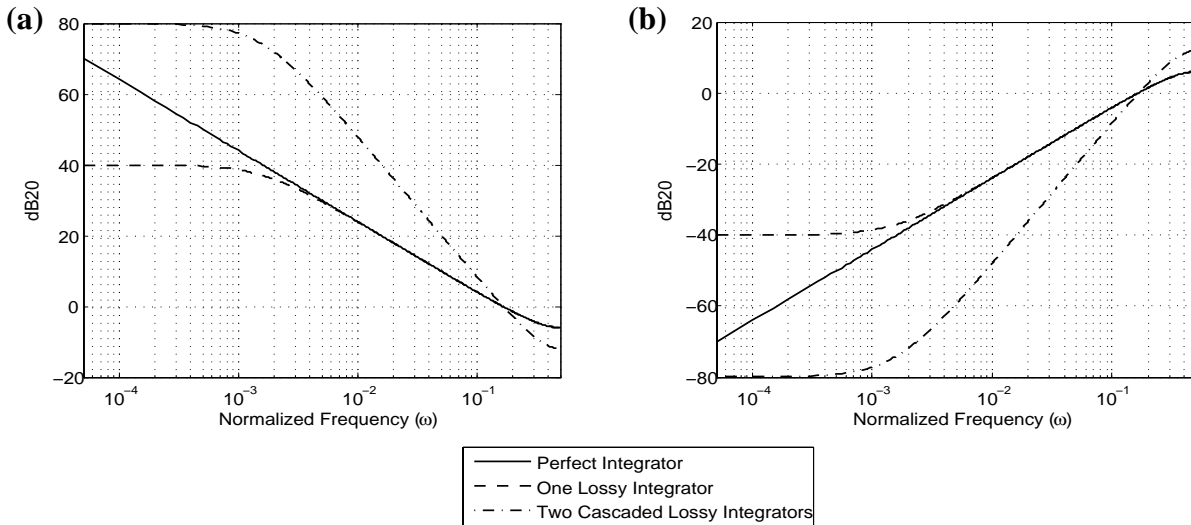
## 6.1. Motivation for High-order Filters

An ideal integrator has a pole exactly at  $z = 1$ , and therefore the gain at DC is infinite. However, when the integrator is lossy, then the pole location shifts and the resulting transfer function becomes:

$$H(z) = \frac{1}{1 - \alpha z^{-1}} \quad (6.1)$$

where  $\alpha < 1$ . The resulting DC gain is no longer infinite; it is simply  $\frac{1}{1 - \alpha}$ . When this integrator is used to implement a  $\Sigma\Delta$  modulator, the finite DC gain limits the attenuation of the in-band quantization noise. Thus, the finite DC gain of the integrator effectively limits the achievable dynamic range of a  $\Sigma\Delta$  A/D [6, 22, 23].

Unfortunately, limited DC gain is inevitable in any circuit implementation. In our circuit implementation, the loss factor resulted from the finite output resistance of the transconductor of the sampler circuit (section 4.2.1). In the numerical example given in the section 4.2.1, a 10 pF integrating capacitor, and a 5 k $\Omega$  output resistance, resulted in an integrator DC gain of only 40 dB.



**Figure 6-1.** Ideal, lossy and cascade of two lossy integrators  
**(a)** Loop filter response, **(b)** Noise transfer function

Figure 6-1(a) displays the frequency response of three different structures, an ideal integrator, a lossy integrator, and a cascade of two lossy integrators. The factor  $\alpha$  of the lossy integrators is set to 0.99, which corresponds to an integrator DC gain of 40 dB. In figure 6-1(b), we showed the noise transfer function of a  $\Sigma\Delta$  modulator when one of the three structures mentioned before is used as a loop filter.

We can draw several conclusions from figure 6-1. First, a loss factor in integrators are always detrimental in the suppression of quantization noise, especially if the input is narrowband. Because of the integrator's finite DC gain, the quantization noise notch flattens out near DC. Second, by cascading two or more integrators together, we can regain some of the in-band quantization noise suppression given by an ideal integrator. Third, one can further argue that for a wide bandwidth signal, two lossy integrators can actually suppress more in-band quantization noise than a single ideal integrator.

The analysis above suggest that in order to improve the dynamic range of the A/D, a second-order loop filter is the way to go. When the available integrators are lossy by nature, then the only way to increase the quality of the loop filter is to cascade a couple of them together.

To return to the big picture, a lossy integrator degrades the response of the N-path filter, the resulting quantization noise transfer function becomes:

$$STF(z) = 1 - \alpha z^{-N} \quad (6.2)$$

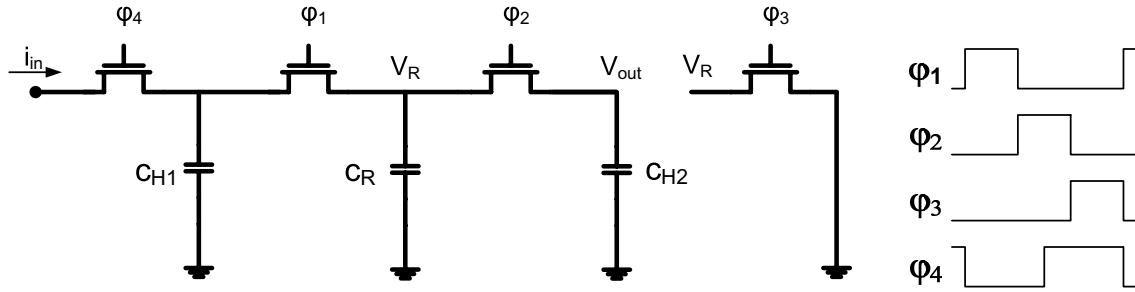
By cascading M lossy integrators and using them to replace a single integrator as the building block for our N-path filter, we can achieve the following noise transfer function

$$STF(z) = (1 - \alpha z^{-N})^M \quad (6.3)$$

## 6.2. Second Order Filter with Passive Circuits

In section 5.1, we have asserted that an amplifier is typically needed to interface two integrators together. These amplifiers are needed to relay the output of one integrator to the input of the next one. Recall that the output of the integrator, specifically in our implementation, is in the form of charge inside a capacitor, or equivalently a voltage across a capacitor. To achieve the goal of cascading two integrators, an active amplifier is typically used to perform a voltage-to-current conversion, or simply to act as a voltage buffer. We further argued that the performance of this amplifier is what typically limits the achievable operating frequency of a filter.

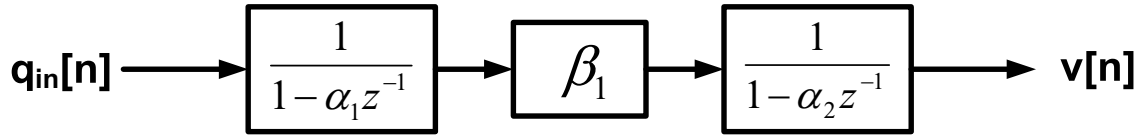
Figure 6-2 shows the proposed method of cascading two integrators. The basic idea is to physically move a fixed fraction of the charge stored in the first integrating capacitor ( $C_{H1}$ ), to the second integrating capacitor ( $C_{H2}$ ). This is accomplished by physically disconnecting a small rotating capacitor ( $C_R$ ) from  $C_{H1}$  and reconnecting it to  $C_{H2}$ .



**Figure 6-2.** Cascade of two integrators with a rotating capacitor

To analyze the circuit, we start at phase  $\phi_3$ . At the end of  $\phi_3$ , the capacitor  $C_R$  is fully reset and therefore it contains no charge. At the same time, capacitor  $C_{HI}$  just finished integrating the input current  $i_{in}$ . Note that the  $\phi_4$  MOS switch and  $C_{HI}$  are part of the front-end windowed-charge-sampling circuit. When  $\phi_1$  is active, charge sharing occurs between  $C_{HI}$  and  $C_R$ . As a result a fixed fraction of the charge from  $C_{HI}$ , denoted  $\frac{C_R}{C_{HI} + C_R}$ , is transferred to  $C_R$ . The rest of the charge stays in  $C_{HI}$ . During  $\phi_2$ , capacitor  $C_R$  is then disconnected from  $C_{HI}$  and reconnected to  $C_{H2}$ . Through charge sharing, the charge inside  $C_R$  and  $C_{H2}$  are combined to equalize the voltages across the two capacitors. At the end of  $\phi_2$ ,  $\frac{C_R}{C_{H2} + C_R}$  fraction of the total charge between the two capacitors resides in  $C_R$ , and the rest resides in  $C_{H2}$ . On  $\phi_3$ ,  $C_R$  is disconnected from  $C_{H2}$  and is reset once again.

Capacitor  $C_{HI}$  forms the first integrator in the cascade. The input of this integrator is the charge packet delivered through the integration of current  $i_{in}$  over the phase  $\phi_4$ . Capacitor  $C_{H2}$  forms the second integrator in the cascade. The input of this integrator is the charge packet delivered through charge sharing with  $C_R$ . Recall that the charge residing in  $C_R$  originates from the capaci-



**Figure 6-3.** Discrete-time model for passive second order filter

tor  $C_{H1}$ . Therefore charge sharing through  $C_R$  effectively relays (a fraction of) the output of the first integrator ( $C_{H1}$ ) to the input of the second one ( $C_{H2}$ ).

Since a fraction of charge residing in  $C_R$  is taken out from both integrators at the end of each corresponding phase, both integrators in the cascade become lossy.

Figure 6-3 shows a discrete-time model of the circuit. In the figure,  $\alpha_1 = \frac{C_{H1}}{C_{H1} + C_R}$  and

$\beta_1 = \frac{C_R}{C_{H1} + C_R}$ . The factors  $\alpha_2$  and  $\beta_2$  are similarly defined. The output of the cascade,

denoted  $v[n]$ , is the voltage across  $C_{H2}$ . Note that the loss factor resulting from the finite output resistance of the transconductor inside the sampler circuit (section 4.2.1) can be assimilated into  $\alpha_1$  and therefore included in the model.

The output voltage of the cascade of integrators is read during either  $\phi_1$  or  $\phi_3$ , i.e., when  $C_{H2}$  is not connected to  $C_R$ . Similarly, at the input current is only integrated when  $C_{H1}$  is not connected to  $C_R$ .

The circuit proposed above achieves the task of cascading two integrators to form a second-order filter without using any active amplifiers. This approach is also generalizable to a cascade of more than two integrators, using the same concept of physically moving charge from one integrating capacitor to the next one.

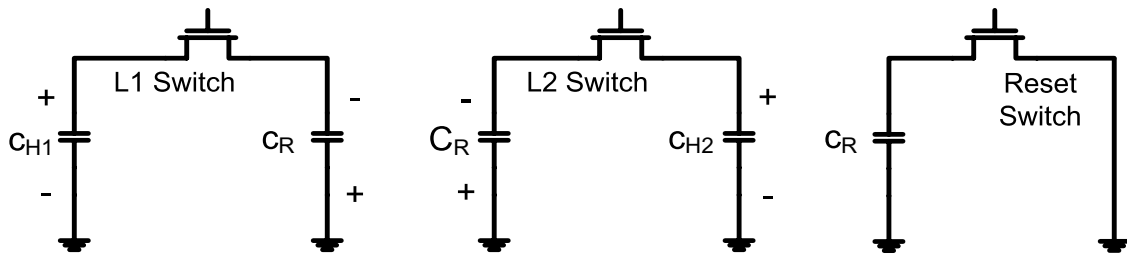
The downside of this approach is two folds. First, the two integrators becomes inherently lossy, due to the need of physically moving charge from one integrating capacitor to the other. Second, the inter-stage gain between the two integrators is relatively small. The loss factor of the integrator is represented by  $\alpha_1$  and  $\alpha_2$ , while the inter-stage gain between integrators is denoted  $\beta_1$ . These factors are determined by the relative sizes between  $C_R$ ,  $C_{H1}$  and  $C_{H2}$ . As such, there is an intrinsic trade-off between the quality of the integrators and the value of the inter-stage gain. The less lossy the integrators is, the smaller the inter-stage gain becomes.

We can easily show that the inter-stage gain is always less than one. In fact to maintain a reasonably useful integrator this gain is usually very small. Having a very small inter-stage gain is undesirable in the presence of circuit noise. Since the inter-stage gain is less than one, the signal is attenuated, and therefore the signal-to-noise ratio is reduced. In the following section we will provide a thorough analysis on the noise generated within the circuit.

### **6.3. Noise Analysis of Second Order Filter.**

Since the circuit consists of only MOS switches and capacitors, the noise generated by the circuit comes only from switching noise. The noise analysis of the second order filter circuit is primarily derived from noise analysis of a sample-and-hold circuit [24]. There are three separate noise sources corresponding to the three non-overlapping switching phases needed to form the output of the filter for each sampling period. Figure 6-4 decomposes the filter circuit into three different sub-circuits corresponding to each of the three phases of the sampling period. We labelled the three different switches as L1, L2 and Reset switch to ease the ensuing discussion.

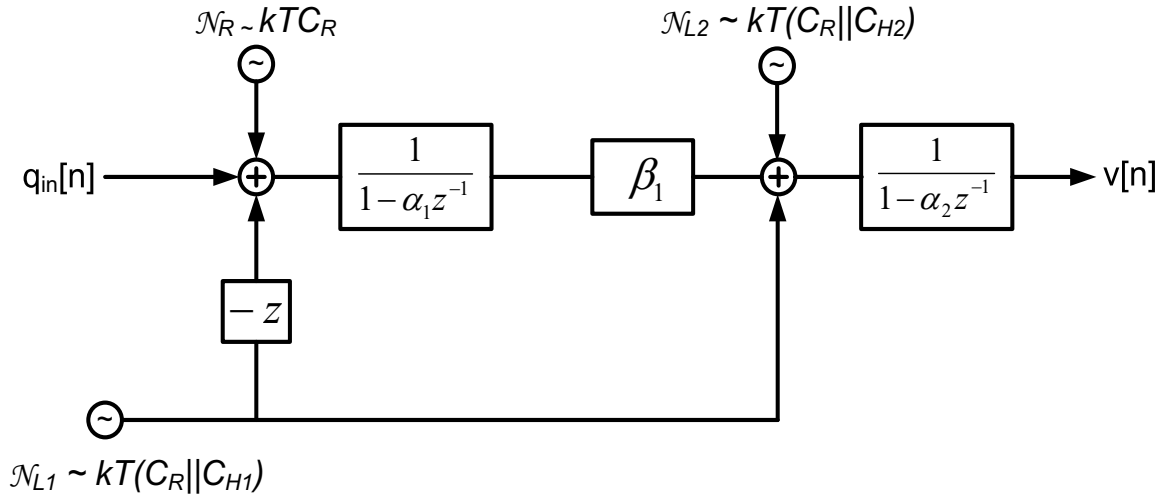
We start the analysis from the Reset switch. When the MOS switch is turned on, the channel within the transistor forms a connection between the two plates of the capacitor. Ideally this con-



**Figure 6-4.** Decomposition of second order filter for noise analysis

nection would short the two capacitor plates, and therefore depleting the charge stored in the capacitor. However, thermal noise generated within the transistor's channel prevents this from happening perfectly. Noise generated inside the transistor would effectively modulate the voltage across the capacitor  $C_R$ . At the instant when the switch is turned off, the connection between the two plates and the noise source is cut off. The instantaneous noise charge stored within the capacitor remains in the capacitor  $C_R$  after the switch is turned off. Thus, a noise charge of power  $kTC_R$  is put into  $C_R$  on each sampling period; where  $k$  is the Boltzman's constant, and  $T$  is the temperature. The exact same argument can be made using voltage instead of charge as the quantity for discussion. To maintain consistency with the rest of the report, we will retain the discussion in the charge domain.

The sub-circuits formed by switch L1 (and similarly L2) is actually topologically identical to the previous sub-circuit, if we consider the two capacitor  $C_{H1}$  and  $C_R$  are in series with each other. At each sampling period a noise charge of power  $kT(C_R \parallel C_{H1})$  is generated and stored in *each* of capacitors  $C_R$  and  $C_{H1}$ . Since the capacitors  $C_R$  and  $C_{H1}$  are in series with each other, both would store the same amount of noise charge; albeit with different polarity as shown in figure 6-4



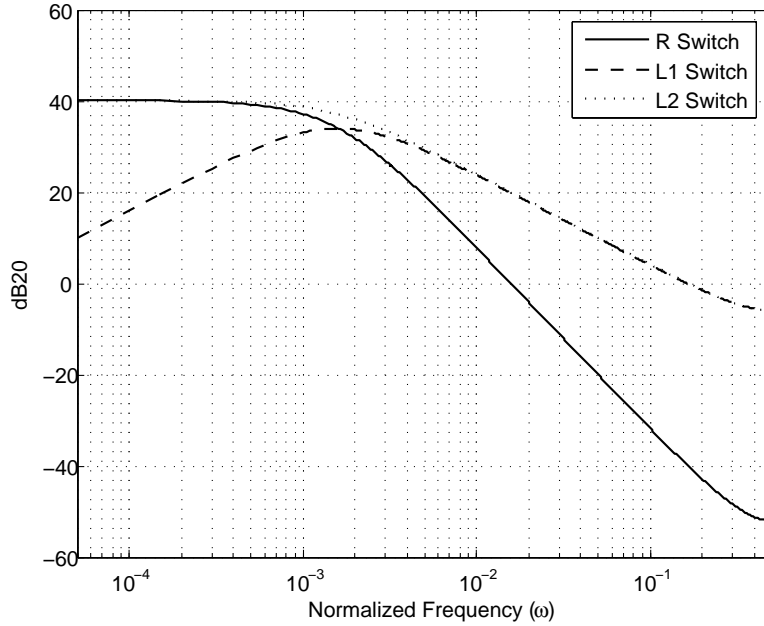
**Figure 6-5.** Noise transfer function for second-order filter

Having identified the three noise sources, we would now proceed to identifying the transfer function between each noise sources to the output to the filter.

The noise generated by the Reset switch is stored inside  $C_R$ . On  $\phi_1$ , this noise charge is transferred to  $C_{H1}$  through charge-sharing. Thus, we can view that the noise charge from the Reset switch actually acts as an input charge packet to the first integrator.

The noise generated by the L2 switch is distributed between  $C_R$  and  $C_{H2}$ . The noise charge located in  $C_R$  is irrelevant because at the next phase,  $C_R$  will be reset and therefore the noise will not be propagated. The noise charge residing in  $C_{H2}$ , on the other hand, is never reset; instead it will be added to the total charge already residing within the capacitor  $C_{H2}$ . Thus, we can consider this part of the noise generated by the L2 switch acts as an input charge packet to the second integrator.

The noise generated by the L1 switch is similarly distributed between  $C_R$  and  $C_{H1}$ . During  $\phi_2$ , the noise charge residing in  $C_R$  would be fully transferred to the second integrating capacitor  $C_{H2}$ .



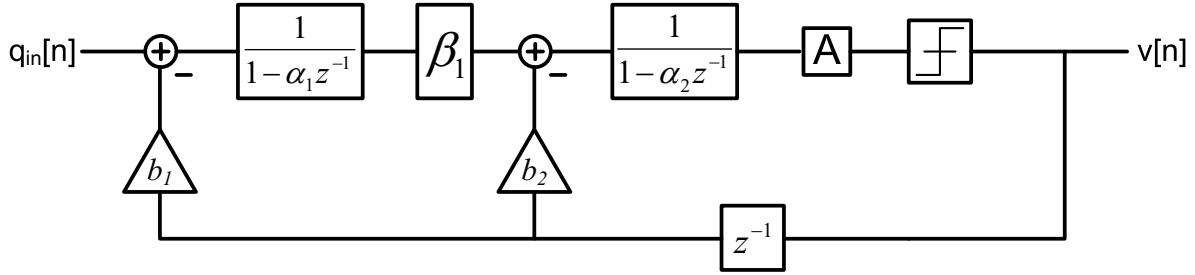
**Figure 6-6.** Frequency response of noise sources for a second-order filter

Therefore we can consider this noise as an input charge packet to the second integrator. The noise residing on  $C_{HI}$ , on the other hand, is retained within  $C_{HI}$ , and would be added to an existing charge already within  $C_{HI}$ . Therefore, with similar argument as in the above paragraph, this part of the noise charge resulting from L1 switch acts as an input to the first integrator. However, this noise charge would only act as an input to the first integrator on the next sampling period. This is because the capacitor  $C_{HI}$  has already been sampled in this period.

It is important to remember that the same noise source, e.g. the L1 switch noise, generates two identical and perfectly correlated noise charge packets that enters the circuit in two different locations. It is therefore crucial to factor in the polarity and the phase relationship between the two noise charge packets in deriving the correct transfer function for this particular noise source.

Figure 6-6 displays the frequency response of the three noise sources at the output. In this figure,

$\alpha_1 = \alpha_2 = \frac{100}{101}$ ,  $\beta_1 = \frac{1}{101}$ . As a reference, the input signal's response is identical to that of the



**Figure 6-7.** Second-order  $\Sigma\Delta$  modulator loop

noise response from the Reset switch. Note that at low frequency, the noise from the L1 switch is highly attenuated. This is due to the existence of a zero near DC in its frequency response.

This result has been confirmed through circuit simulation with SpectreRF.

#### 6.4. Second-Order $\Sigma\Delta$ Modulator

In our system, a distributed feedback architecture is chosen for the same reason of avoiding the need for additional amplifiers. A feed-forward architecture would require additional amplifiers to sum the values of the various integrators in the modulator.

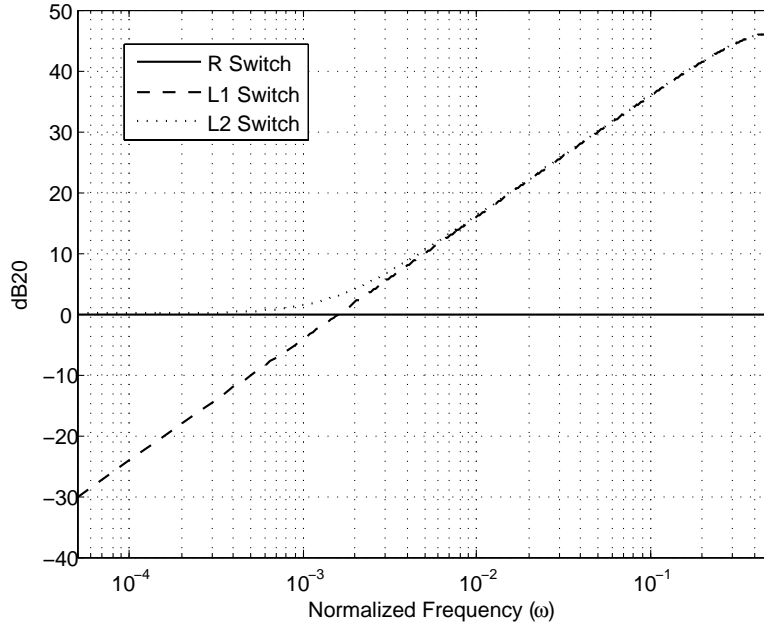
Figure 6-7 displays the second-order  $\Sigma\Delta$  modulator architecture. We can derive the signal and noise transfer functions as:

$$STF(z) = \frac{\beta_1 A}{D(z)} \quad (6.4)$$

$$NTF(z) = \frac{(1 - \alpha_1 z^{-1})(1 - \alpha_2 z^{-1})}{D(z)} \quad (6.5)$$

where the common denominator  $D(z)$  is given by:

$$D(z) = 1 - (\alpha_1 + \alpha_2 - b_1 \beta_1 A - b_2 A)z^{-1} + b_1 \alpha_1 A z^{-2} \quad (6.6)$$



**Figure 6-8.** Frequency response of noise sources for a second-order  $\Sigma\Delta$  modulator

To simplify the analysis, we set  $A\beta_1 = 1$ . This assumption can be removed without much impact.

There are two important points from the above three equations. First, a second-order noise shaping does happen; where we have two zeros close to  $z = 1$ . The quality of these zeros depends on the loss factors  $\alpha_i$ . Second, through choice of coefficients  $b_1$  and  $b_2$ , we could essentially form two arbitrary poles simultaneously in both the STF and NTF.

For the purpose of the ensuing discussion, we will set  $b_1$  and  $b_2$  such that  $D(z) = 1$ . This requirement results in  $b_1 = \alpha_1$  and  $b_2 = \beta_1\alpha_2$ .

Figure 6-8 displays the transfer functions of the three switching noise sources when put inside a second order  $\Sigma\Delta$  modulator. The value for  $\alpha_1$ ,  $\alpha_2$ , and  $\beta_1$  are identical to that of figure 6-7. The important point in this figure is that for low frequencies, noise from the Reset and L2 switches are

the ones that matter. Furthermore both noise sources are transferred to the output with a gain of around one for low frequencies.

We can proceed to calculate the necessary capacitor sizes to obtain the desired dynamic range. An oversampling ratio (*OSR*) of one thousand is typical for an RF signal; where oversampling in this case simply reflect the bandwidth of the signal compared to the sampling rate of the modulator. From figure 6-8, we found that for that amount of oversampling, the total noise at the output of the modulator is the sum of noise contribution from the Reset and the L2 switch. Furthermore, we know that the signal has a transfer function equals to unity from the input to the output of the modulator. We can therefore calculate the achievable dynamic range, given a size of capacitor, as:

$$DR = 10\log_{10}\left(\frac{OSR(G_m T_s V_{DD})^2}{16 kTC_R}\right) - 10\log_{10}(|H_W(f_c)|^2) \quad (6.7)$$

The second term in the equation is included to factor in the input signal attenuation due to the windowed-charge-sampler frequency response.

For example, for  $C_R = 100fF$ ,  $C_{H1} = C_{H2} = 10pF$ ,  $G_m = 1mS$ , with a 1 GHz sampling frequency and a 1 MHz signal bandwidth, the resulting dynamic range would be around 100 dB. Although the noise power depends on the size of a relatively small capacitor  $C_R$ , the large oversampling ratio means that the switching noise is spread over a large bandwidth. Therefore the in-band portion of the total noise is relatively small.



# Chapter 7

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## *Digital Background Calibration*

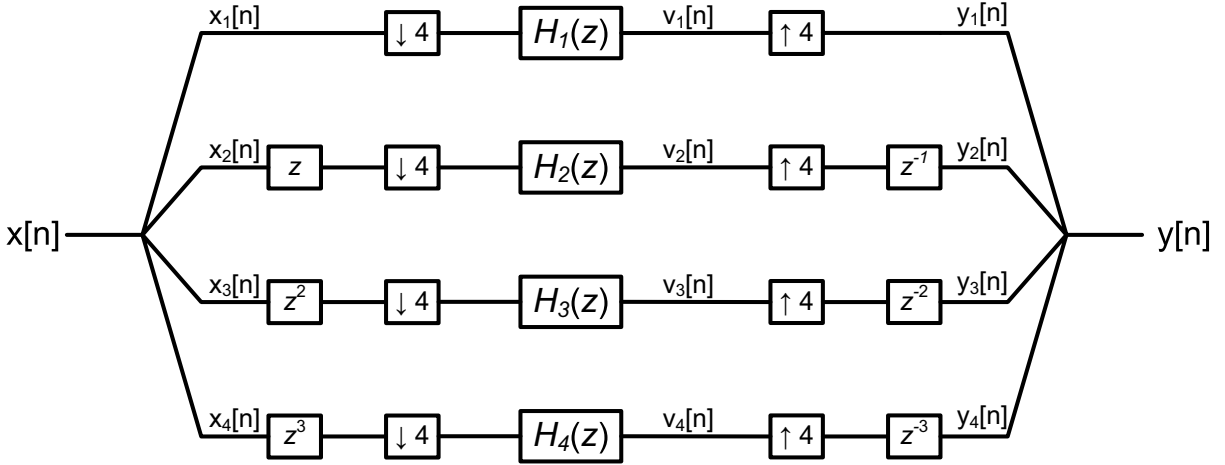
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A bandpass  $\Sigma\Delta$  A/D built using an N-path filter is an inherently time-interleaved system. As such, component and timing mismatch between the different paths can potentially limit the performance of the A/D. The various impairments resulting from path mismatches in a general time-interleaved A/D have been discussed elsewhere [30, 31]. The focus of this chapter would be to analyze the specific impairments and performance limitations that arise in the case of a four-path bandpass  $\Sigma\Delta$  A/D. The primary sources of mismatches will be identified. Furthermore, due to the narrow-band nature of the desired signal, we will also identify and isolate the potentially harmful images that might overlap with the desired signal in the presence of path mismatches.

We will then proceed to propose an online digital background calibration routine that would mitigate the effect of path mismatches in the system. The primary goal of this discussion is to illustrate the tools and mechanisms for calibration made available by this architecture; and not on the specific realization of the calibration algorithm.

### **7.1. Impact of Path Mismatches in a Four-Path Bandpass $\Sigma\Delta$ A/D**

In order to analyze the impact of path mismatches in a time-interleaved system, figure 7-1 shows a discrete-time model of a four-path time-interleaved system. In time-domain, the system simply time-interleaves the input signal into the four paths and de-interleaves it to form the output signal.



**Figure 7-1.** Model for mismatch analysis in a time-interleaved system

The four different filters denoted  $H_i(z)$  are used to model the mismatches among the four paths. These filters can be as simple as a constant factor for all frequencies, to model gain mismatches; but it can also model more complicated frequency-dependent mismatches.

In the frequency domain, we can write the output of each path before de-interleaving as:

$$V_i(z) = \frac{1}{4} H_i(z) \sum_{p=1}^4 \left( e^{-j\frac{2\pi}{4}i} z^{1/4} \right)^p X \left( e^{-j\frac{2\pi}{4}p} z^{1/4} \right) \quad (7.1)$$

De-interleaving essentially reconstructs the signal from the four paths as:

$$Y(z) = V_1(z^4) + z^{-1} V_2(z^4) + z^{-2} V_3(z^4) + z^{-3} V_4(z^4) \quad (7.2)$$

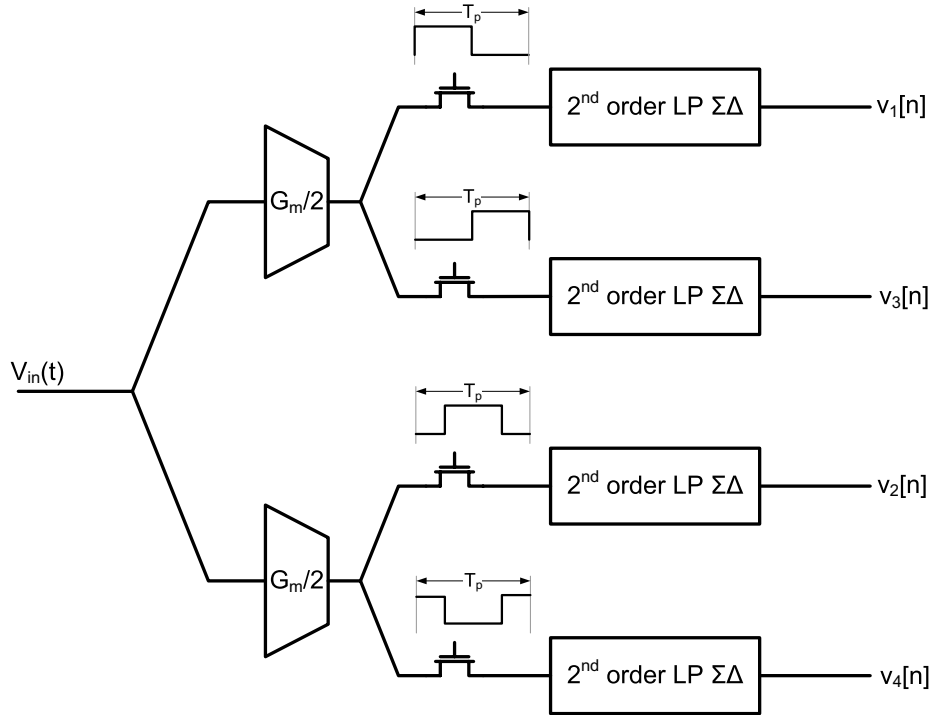
In order to get an intuitive understanding on the impact of path mismatches, it is worthwhile to expand the output of the time-interleaved system and write it as a frequency response, e.g. at

$z = e^{-j\omega}$ :

$$\begin{aligned}
Y(\omega) = & \frac{1}{4}H_1(4\omega)\left[X(\omega) + X\left(\omega - \frac{\pi}{2}\right) + X(\omega - \pi) + X\left(\omega - \frac{3\pi}{2}\right)\right] \\
& + \frac{1}{4}H_2(4\omega)\left[X(\omega) - jX\left(\omega - \frac{\pi}{2}\right) - X(\omega - \pi) + jX\left(\omega - \frac{3\pi}{2}\right)\right] \\
& + \frac{1}{4}H_3(4\omega)\left[X(\omega) - X\left(\omega - \frac{\pi}{2}\right) + X(\omega - \pi) - X\left(\omega - \frac{3\pi}{2}\right)\right] \\
& + \frac{1}{4}H_4(4\omega)\left[X(\omega) + jX\left(\omega - \frac{\pi}{2}\right) - X(\omega - \pi) - jX\left(\omega - \frac{3\pi}{2}\right)\right]
\end{aligned} \tag{7.3}$$

In eq. 7.3, each line corresponds to the output of each path after the upsampling process, but before the four signals are recombined, i.e. at  $y_i[n]$ . Due to the inherent downsampling operation in a time-interleaved system, the signal on each path is cluttered with three of its own images, at  $\frac{\pi}{2}$ ,  $\pi$ , and  $\frac{3\pi}{2}$  shifts in the normalized frequency axis. If each of the path is perfectly matched to each other for all frequencies, e.g.  $H_1(\omega) = H_2(\omega) = H_3(\omega) = H_4(\omega)$ , then the recombination of the four paths will enable the system to suppress the three undesired images perfectly. The resulting output will be the original signal, frequency shaped by one of the four (identical) paths' filter; i.e.,  $Y(\omega) = H_1(4\omega)X(\omega)$ . If the four paths is not matched perfectly for all frequencies, then the images would not be cancelled perfectly. This results in undesired images overlapping with the signal of interest.

We can analyze our proposed four-path bandpass  $\Sigma\Delta$  A/D, shown in figure 7-2, for possible cause of mismatches. In the windowed-charge-sampling circuit, mismatches in the transconductor as well as the duration of current integration contribute to a path gain mismatch. After the sampling operation, the signal is converted into a digital representation using a second-order lowpass  $\Sigma\Delta$  modulator. Inside the  $\Sigma\Delta$  modulator, capacitor mismatches as well as mismatches in the feedback DAC can cause further mismatches between the four paths.



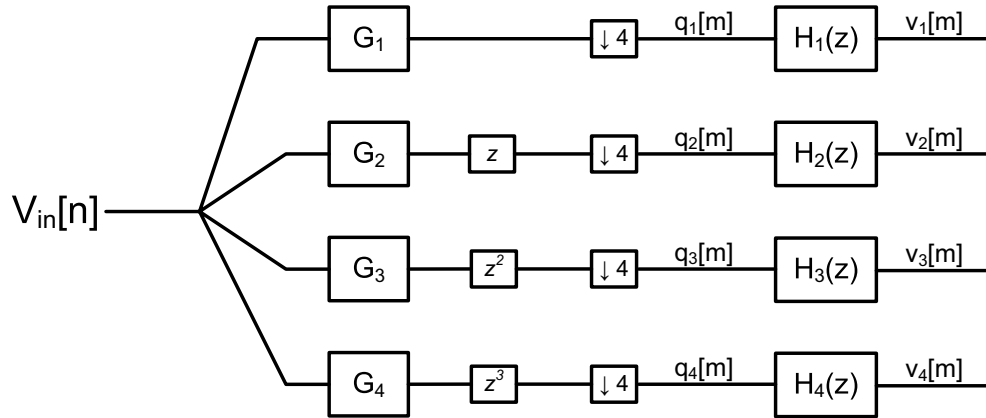
**Figure 7-2.** Four-path Bandpass  $\Sigma\Delta$  A/D

We can model the four-path bandpass  $\Sigma\Delta$  A/D as in figure 7-3 for the purpose of modelling path mismatches. The mismatches between the four  $\Sigma\Delta$  modulators are represented by the four filters denoted  $H_i(z)$ . It is easy to show that the filter  $H_i(z)$  is simply the signal transfer function for each of the four  $\Sigma\Delta$  modulators. Although the topology of the four  $\Sigma\Delta$  modulators are identical, the signal transfer functions can be slightly different in the presence of circuit mismatches.

Furthermore, we can also pinpoint the locations of the signal images that can potentially fold back to the desired band of interest, based on eq. 7.3. The desired RF signal is located in a small band

around  $\frac{f_s}{4}$ . Thus, the potentially harmful images are located at around DC, at  $-\frac{f_s}{4}$ , and at  $\pm\frac{f_s}{2}$ .

These bands corresponds to the  $\frac{\pi}{2}$ ,  $\pi$ , and  $\frac{3\pi}{2}$  (left) shifts in the normalized frequency axis, from the location the desired signal.



**Figure 7-3.** Discrete-time mismatch model for four-path bandpass  $\Sigma\Delta$  A/D

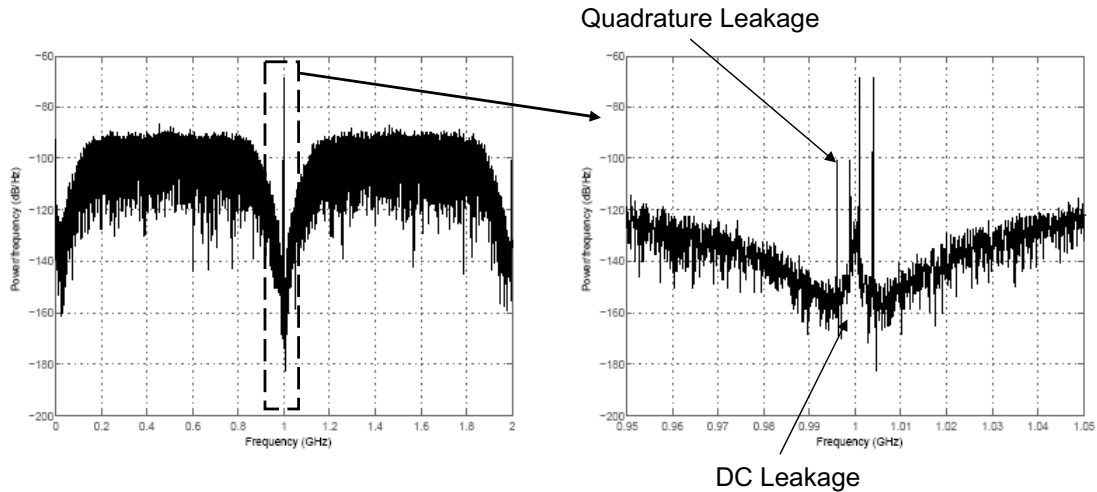
The band around  $\pm \frac{f_s}{2}$  will be occupied by signals at the second harmonic of the desired RF carrier.

This signal will be partly attenuated by the frequency response of the windowed-charge-sampling circuit. The band around DC will be cluttered by  $1/f$  noise, low frequency  $IM_2$  products as well as static DC offsets resulting from charge injection and clock feed-through. If the RF signal is

quadrature modulated, then the band at  $-\frac{f_s}{4}$  would contain the complex conjugate of the desired

signal. Overlap with images at  $-\frac{f_s}{4}$  results in an impairment similar to an I/Q imbalance in a direct conversion receiver.

Figure 7-4 shows a spectrum plot of the four-path bandpass  $\Sigma\Delta$  A/D with path mismatch. One of the feedback DAC is set to have a 5% deviation from the nominal value. The A/D is run at 4 GHz, with the RF signal to be located around 1 GHz. We input two tones at 1.001GHz and 1.004 GHz at -14 dBFS. At DC we also input a slowly varying random sequence to mimic signals arising from second-order intermodulation as well as other sources of DC offsets. We exaggerated these DC signals for the purpose of illustration; in reality these signals would have a smaller magnitude.



**Figure 7-4.** PSD plot of mismatched four-path bandpass  $\Sigma\Delta$  A/D

Because of the path mismatch, images of both the DC signal as well as the quadrature of the desired signal appear in the band of interest.

If the desired RF signal is to be sampled with a high dynamic range, then provisions have to be made so that the levels of the undesired signal are less than the quantization noise floor. Otherwise, the undesired images would be indistinguishable from the desired RF signal. Achievable component matching usually dictates the amount of rejection available towards these undesired images. Typically the amount of rejection degrades dB-by-dB as the relative matching between components is reduced.

In current CMOS technologies, achievable relative matching between components ranges from 0.1% to as much as 10%, depending on the available process option. Trimming can further enhance the achievable relative matching, albeit at a very high cost.

This argument sets the stage for the need of a calibration routine. It turns out, a simple FIR filter can suppress most of the undesired images by matching the frequency responses of the four paths. This would enable the bandpass  $\Sigma\Delta$  A/D to maintain a better signal fidelity and immunity towards

1/f noise, low frequency  $IM_2$  products, charge injection, as well as improving the quadrature matching.

In the above discussion we neglected the impact of mismatches towards the shaping of the quantization noise. In the presence of circuit mismatches, quantization noise would also overlap with its own images. Because of this, the in-band quantization noise level will be determined by the path with least in-band quantization noise rejection. Therefore, in light of mismatches, one can argue that the in-band quantization noise floor would be increased somewhat. However, this impairment is not as severe as the case with signal images, since signal images will appear as spurious tones in the spectrum.

## 7.2. Digital Background Calibration for a Four-path Bandpass $\Sigma\Delta$ A/D

As mentioned in the previous section, the mismatch on each of the four paths can be modeled by a constant gain factor followed by the signal transfer function of the each path's  $\Sigma\Delta$  A/D. We can then write the transfer function for each path  $i$  as (eq. 6.4):

$$H_i(z) = \frac{G_i}{1 + b_{1i}z^{-1} + b_{2i}z^{-2}} \quad (7.4)$$

where the parameters  $G_i$ ,  $b_{1i}$  and  $b_{2i}$  are determined by component parameters, such as capacitor size and DAC current.

Suppose the ideal transfer function is given as:

$$H(z) = \frac{1}{1 + b_1z^{-1} + b_2z^{-2}} \quad (7.5)$$

then, clearly the following filter is sufficient to cancel the mismatches:

$$C_i(z) = \frac{1}{G_i} \left[ \frac{1 + b_{1i}z^{-1} + b_{2i}z^{-2}}{1 + b_1z^{-1} + b_2z^{-2}} \right] \quad (7.6)$$

In other words, for a second-order  $\Sigma\Delta$  modulator built using a feedback structure, a digital filter with two poles and two zeros are sufficient to correct for the path mismatches.

If the desired signal transfer function is a constant, e.g.  $H(z) = 1$ , then clearly a two-tap FIR filter is a sufficient correction filter.

The next step in developing the calibration routine is on how to estimate the three coefficients  $G_i$ ,  $b_{1i}$  and  $b_{2i}$  for each of the four paths. We would like to do this without interrupting the operation of the filter; while at the same time being able to continuously monitor changes in the mismatches due to voltage and temperature variation.

We would like to use a training sequence in order to perform the system identification. The idea is to input a common, known training sequence to each of the four paths. Based on the digital output, one can estimate the three coefficients  $G_i$ ,  $b_{1i}$  and  $b_{2i}$  for each of the path. A greedy gradient-descent type approach, such as LMS, can be used to estimate the coefficients for each path.

We can generate this training sequence by inputting a narrow-band signal located around DC. If the maximum frequency of the signal is much less than each path's sampling frequency, then each of the four paths would see an almost identical signal, which is the training sequence itself. There will be slight phase shifts between the four paths due to the time-interleaving process. However, if the bandwidth of the training signal is small enough, then the error due to the phase shifts can be kept very small.

Since mismatch is unavoidable, images of this training sequence will corrupt the signal of interest at around  $\frac{f_s}{4}$  initially. However, as the system is able to converge to the right correction filters, the mismatch between paths will be greatly reduced. In the ideal case when the path is perfectly matched, then images of the training sequence should be completely eliminated from the band of interest. This fact is important, because when the system is fully calibrated, then the presence of a training signal around DC would not affect the normal operation of the A/D. However, this training signal can be used to detect if any deviation on the parameters occurs, possibly due to voltage or temperature variation

Therefore, this training signal can be input to the system continuously without much of an impact to the normal operation of the A/D. This is very important in achieving an online digital calibration capability.

Recall that due to the four-path loop filter structure, quantization noise will be nulled around DC. Thus, the training sequence around DC would actually be converted to digital with a high level of fidelity. This is important, since the quality of the parameter estimation will only be as good as observation of the output of the system. Averaging can further enhance the quality of the estimate, at the cost of acquisition time.

In short, we utilized the extra quantization noise nulls around DC in order to accommodate a training sequence. Based on each path's response to this training signal, we can estimate and form a digital correction filter which would mitigate the effect of circuit mismatches. Being able to fully calibrate the time-interleaved system for path mismatch would enable better rejection towards  $1/f$  noise,  $IM_2$  products and other DC offsets, as well as quadrature leakage.



# Chapter 8

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## *Conclusion*

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In this project we propose the use of a bandpass  $\Sigma\Delta$  A/D to directly capture RF signals. We identified challenges and technology limitations that have so far prevented the successful implementation of such system. We then proceed to propose several techniques to circumvent these limitations.

Most of the system and circuit techniques presented in this project have been separately presented elsewhere in the literature. The main contribution of this project is in combining several of these previously known techniques in solving the problem at hand. Furthermore, some detailed analysis is provided in this report that has previously been unavailable in the literature.

In summary, the proposed solution comprises of four enabling techniques. A windowed-charge-sampling circuit to pre-condition and sample the radio signal. A discrete-time N-path filter structure is used to synthesize a bandpass type frequency response using integrators as building block. The noise-shaping afforded by a single integrator is further enhanced by replacing it with a cascade of two lossy integrators, which is built entirely using passive elements. Finally, an online digital calibration routine is introduced to mitigate the impact of circuit mismatches to the performance of the overall architecture.

## 8.1. Future Work

The immediate continuation of this project is to move this system level description into circuit level implementation.

The two biggest challenge that we can foresee at the moment is the design of the front-end transconductor and in maintaining good linearity in the passive switched capacitor network.

There are two analyses that are still missing in this report; a noise analysis on the front-end transconductor, and a comprehensive analysis on the impact of clock jitter in the architecture.

Noise analysis in the front-end transconductor turns out to be quite challenging due to the many nonlinear interactions that are happening at the output of the transconductor. A closed-form analytical solution to this problem might not be easily obtained, and we may resort to performing optimization using a circuit simulator.

We feel that the jitter analysis through time-to-voltage error conversion is not completely appropriate, when this architecture is used as a radio receiver. This type of analysis originates from baseband A/D's and can not be applied blindly to derive specifications for a bandpass  $\Sigma\Delta$  A/D used as a radio receiver. Most modulation are designed to be have some resiliency towards jitter; or, in this case, phase noise. Simple comparison to the phase noise performance achieved by commercial receivers does not provide good correlation to the jitter requirement derived in this report. Therefore, a more comprehensive, system level evaluation must be made to properly asses the impact of clock jitter in this system.

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