

A 1.5-V 0.7–2.5-GHz CMOS Quadrature Demodulator for Multiband Direct-Conversion Receivers

Nuntachai Poobuapheun, *Student Member, IEEE*, Wei-Hung Chen, *Student Member, IEEE*, Zdravko Boos, and Ali M. Niknejad, *Member, IEEE*

Abstract—An integrated quadrature demodulator with an on-chip frequency divider is reported. The mixer consists of a transconductance stage, a passive current switching stage, and an operational amplifier output stage. A complementary input architecture has been used to increase the transconductance for a given bias current. The circuit is inductorless and is capable of operating over a broad frequency range. The chip was implemented in a 0.13- μm CMOS technology. From 700 MHz to 2.5 GHz, the demodulator achieves 35 dB of conversion voltage gain with 250-kHz IF bandwidth, a double-sideband NF of 10 dB with 9–33 kHz $1/f$ -noise corner. The measured IIP3 is +4 dBm for a 0.1-MHz IF frequency and +10 dBm for a 1-MHz IF frequency. The total chip draws 20 to 24 mA from a single 1.5-V supply.

Index Terms—CMOS RF, passive current switching mixer, quadrature demodulator, wireless communications.

I. INTRODUCTION

WITH the proliferation of wireless standards and frequency bands of operation, there is an urgent need to design a single transceiver that is compatible with multiple standards. Direct conversion (zero-IF) is attractive for the transceiver due to its high level of integration and the simplicity of the baseband circuitry. Despite the attractiveness, designing a mixer for multi-band operations in deep-submicron CMOS technology is nontrivial. The main challenge lies in maintaining moderate gain, noise figure, and linearity at minimum current consumption across a wide frequency spectrum with the abating supply voltage.

This paper presents the design of a wideband CMOS quadrature demodulator based on the passive current switching mixer with active first-order RC filtering at its output [1]–[3]. Complementary folded inputs [4], [5] are employed to achieve higher transconductance efficiency. No inductor has been utilized in order to realize a wideband demodulator. The elimination of inductors also leads to substantial die area reduction and reduced substrate coupling due to the inevitably large inductor dimensions especially at low gigahertz frequencies. The circuit operates over a wide range of frequencies from 700 MHz to 2.5 GHz.

Manuscript received December 1, 2006; revised March 28, 2007.

N. Poobuapheun, W.-H. Chen, and A. M. Niknejad are with the Berkeley Wireless Research Center, Department of Electrical Engineering and Computer Sciences, University of California, Berkeley, CA 94704-1302 USA (e-mail: nuntachp@eecs.berkeley.edu).

Z. Boos is with Infineon Technologies, Munich D-81739, Germany.

Digital Object Identifier 10.1109/JSSC.2007.900294

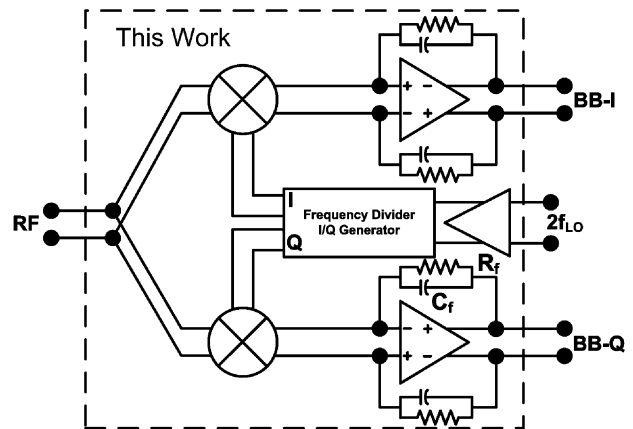


Fig. 1. Demodulator architecture overview.

This paper is organized as follows. In Section II, the architecture of the demodulator and the mixer is discussed. The circuit design details for the mixer and the frequency divider are presented in Section III, followed by measurement results in Section IV, with the conclusion in Section V.

II. ARCHITECTURE

A. Demodulator Architecture

The demodulator block diagram is shown in Fig. 1. It consists of two separate mixers for in-phase (I) and quadrature-phase (Q) paths and a local oscillator (LO) generation circuit. The divide-by-two circuit is implemented to generate on-chip quadrature LO signals from the external $2f_{LO}$ source. The on-chip frequency division effectively isolates the signal coupling between LO and RF ports via bondwires and reduces the reciprocal mixing considerably. This is important in direct-conversion systems where the desired signal is located at f_{LO} . Nonetheless, residual signal coupling occurs between LO and RF ports due to ground and supply bounce internally on chip. All the RF and signal paths are implemented in fully differential style in order to enhance common-mode noise rejection. Since the demodulator is designed to be integrated with an on-chip LNA, its input impedance is not matched to 50Ω and an off-chip resistor was used for input matching in measurements. Quadrature phase matching between I and Q paths in this architecture depends strongly on the duty cycle of the external $2f_{LO}$ source, as will be discussed later in the paper.

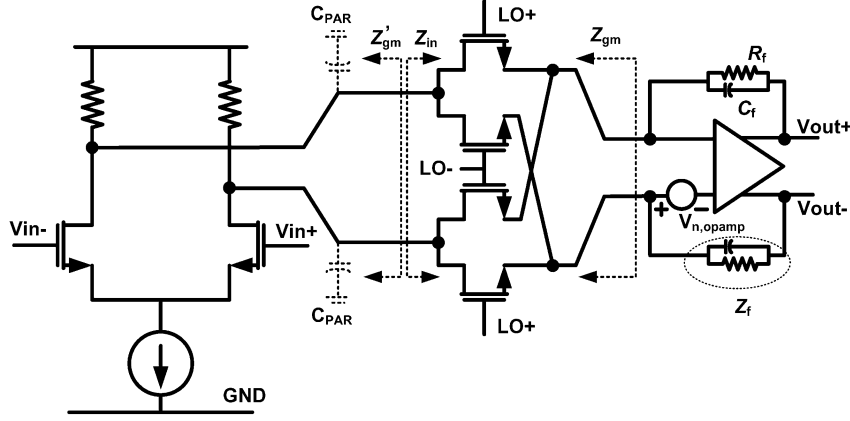


Fig. 2. Mixer conceptual diagram.

B. Mixer Architecture

A conceptual diagram of the mixer core is shown in Fig. 2. It consists of an RF transconductance stage followed by a double balanced switching quad. An RF current from the transconductor commutates through the time-varying switching quad, experiences frequency-translation, and flows into the transimpedance load. The baseband voltages are established at the amplifier output after the switching current passes through the first-order RC low-pass network. The overall voltage conversion gain of the mixer due to fundamental tone mixing can thus be approximated as

$$\frac{V_{out}(f_{out})}{V_{in}(f_{in})} \approx \frac{2}{\pi} g_m \left(\frac{R_f}{1 + j2\pi f_{out} R_f C_f} \right) \quad (1)$$

where f_{out} is the output frequency at IF, f_{in} is the input RF frequency, g_m is the total transconductance of input stage, and the factor $2/\pi$ is related to the first harmonic amplitude of the periodically time-varying transfer function [6]. The operational amplifier provides a virtual ground at its input and appears as a low impedance (Z_{in}) at the mixer core output. Low Z_{in} retains the current mode operation at the output of the transconductor and hence relieves the linearity degradation imposed by the limited voltage headroom [2], [3]. Another advantage of this architecture is that the signal experiences first-order low-pass filtering before reaching the first high voltage-swing node at the amplifier output. This results in a higher 1-dB compression point for the mixer as well as lowered linearity requirements on subsequent blocks in the receiver chain.

Major noise sources in this architecture are the input transistors, the transimpedance amplifier, the feedback resistors, and the transistors in the switching quad. $1/f$ noise in the switching quad depends on the amount of current flowing through the switches [7]. Since there is a very small DC bias current flowing through the switches, $1/f$ noise from the switching quad can be made negligibly small. Noise at the output of the mixer from each of the major noise sources are

$$\bar{V}_{n,out}^2(f_{out}, f_{in})_{g_m} = (4kT\gamma g_{ds0})\beta^2 |Z_f(f_{out})|^2 \Delta f \quad (2)$$

$$\begin{aligned} \bar{V}_{n,out}^2(f_{out}, f_{in})_{switches} \\ = \frac{4kT}{R_{ON}} \left| \frac{R_{ON}}{R_{ON} + Z'_{gm}(f_{in})} \right|^2 \beta^2 |Z_f(f_{out})|^2 \Delta f \quad (3) \end{aligned}$$

$$\bar{V}_{n,out}^2(f_{out}, f_{in})_{opamp} = \bar{V}_{n,amp}^2 \left| 1 + \frac{2Z_f(f_{out})}{Z_{gm}(f_{in})} \right|^2 \quad (4)$$

$$\bar{V}_{n,out}^2(f_{out}, f_{in})_{R_f} = \frac{4kTR_f \Delta f}{|1 + j2\pi f_{out} R_f C_f|^2} \quad (5)$$

where γ is process-dependent [6], β^2 is a constant representing a switching activities including noise folding effects and equals $\pi^2/8$ under the assumption of perfect square wave switching [6]. $\bar{V}_{n,amp}^2$ is the operational amplifier's input-referred voltage noise, R_{ON} is the average on resistance of the switches, and Z_{gm} is the effective impedance looking into the switches from the transimpedance amplifier as shown in Fig. 2. If the current is small and the transistor is biased to have low average on-resistance, noise contribution from the switches to overall noise performance is then negligible. If we exclude the noise from the source and the switching quad, the total added output spot noise in the mixer can be estimated as

$$\begin{aligned} \bar{V}_{n,out}^2(f_{out}, f_{in}) &= (4kT\gamma g_{ds0})\beta^2 |Z_f(f_{out})|^2 \Delta f \\ &+ \bar{V}_{n,amp}^2 \left| 1 + \frac{2Z_f(f_{out})}{Z_{gm}(f_{in})} \right|^2 + \frac{4kTR_f \Delta f}{|1 + j2\pi f_{out} R_f C_f|^2}. \quad (6) \end{aligned}$$

Dividing the output noise by the voltage gain of the mixer, the input-referred voltage noise is

$$\begin{aligned} \bar{V}_{n,in}^2(f_{out}, f_{in}) \\ = \frac{(4kT\gamma g_{ds0})\beta^2 |Z_f(f_{out})|^2 \Delta f}{g_m^2 \left(\frac{2}{\pi}\right)^2 |Z_f(f_{out})|^2} \\ + \frac{\bar{V}_{n,amp}^2 \left| 1 + \frac{2Z_f(f_{out})}{Z_{gm}(f_{in})} \right|^2}{g_m^2 \left(\frac{2}{\pi}\right)^2 |Z_f(f_{out})|^2} \\ + \frac{4kTR_f \Delta f}{g_m^2 \left(\frac{2}{\pi}\right)^2 |Z_f(f_{out})|^2 |1 + j2\pi f_{out} R_f C_f|^2}. \quad (7) \end{aligned}$$

If $Z_f \gg Z_{gm}$ and defining $\alpha = g_m/g_{ds0}$, the equation above simplifies to

$$\begin{aligned} \bar{V}_{n,in}^2(f_{out}, f_{in}) &= \frac{4kT\gamma}{\alpha g_m} \left(\frac{\beta\pi}{2} \right)^2 \Delta f \\ &+ \frac{\pi^2}{g_m^2} \left(\frac{\bar{V}_{n,amp}^2}{|Z_{gm}(f_{in})|^2} + \frac{kT}{R_f} \Delta f \right). \quad (8) \end{aligned}$$

One interesting observation from (8) is that the input-referred noise increases when Z_{gm} decreases [3]. If Z_{gm} is dominated by the parasitic capacitance C_{par} as shown in Fig. 2, then

$$Z_{gm}(f_{in}) = \frac{1}{4f_{in}C_{par}} \quad (9)$$

and (8) becomes

$$\bar{V}_{n,in}^2(f_{out}, f_{in}) = \frac{4kT\gamma}{\alpha g_m} \left(\frac{\beta\pi}{2}\right)^2 \Delta f + \left(\frac{4\pi f_{in}C_{par}}{g_m}\right)^2 \bar{V}_{n,amp}^2 + \frac{\pi^2}{g_m^2} \left(\frac{kT}{R_f}\right) \Delta f. \quad (10)$$

As suggested by the equation above, noise contributions from the transimpedance amplifier become significant at higher input frequency and increase with C_{par} . In a narrowband design, we can employ an inductor to tune out C_{par} , whereas in this broadband design it is important to reduce this capacitor as much as possible.

Linearity performance in the mixer depends on the linearity of the voltage-to-current conversion in the transconductance stage, effects from the switching stage, and the linearity of the transimpedance amplifier stage. The linearity of a transconductance stage has been extensively analyzed in [8] and [9], and can be designed to have higher than +10 dBm IIP₃ with careful sizing and moderate current consumption. In wideband designs, the linearity of this stage will be relatively flat as a function of operating and offset frequencies. The linearity of the transimpedance amplifier, however, depends strongly on the frequency offsets of the blocking signal from the carrier, explained as follows. As depicted in Fig. 2, the transimpedance amplifier can be viewed as a current-feedback amplifier with feedback impedance Z_f and driven by a current source with effective impedance Z_{gm} . Assuming an amplifier has a forward voltage transfer function of $A(f)$, the total loop gain of this amplifier can be written as

$$T(f) = A(f) \frac{Z_{gm}(f)}{Z_{gm}(f) + Z_f(f)} \quad (11)$$

$$T(f) = A(f) \frac{Z_{gm}(f)}{Z_{gm}(f) + \left[\frac{R_f}{1+j2\pi f R_f C_f}\right]}. \quad (12)$$

To get higher loop gain and higher input-referred input intercept point, we need to maximize the open-loop linearity of $A(f)$ as well as the loop gain $T(f)$ [10]. Due to frequency conversion in the switches, impedance $Z_{gm}(f)$ at low frequency (near DC) will be proportional to the impedance $Z'_{gm}(f)$ near the LO frequency. Since $Z'_{gm}(f)$ is relatively flat near the LO frequency, $Z_{gm}(f)$ is then approximately constant as a function of baseband frequency. $Z_f(f)$, however, follows 20 dB/dec decrease with baseband frequency since it is an RC network. If the magnitude and linearity of $A(f)$ are relatively constant, $T(f)$ increases with the frequency and results in better input-referred linearity intercept point of the circuits. Once the frequency increases up to a point where the open-loop gain of the amplifier decreases, the loop gain, as well as the linearity performance of the circuit, does not increase further. It is worth mentioning that the linearity of $A(f)$ is not constant

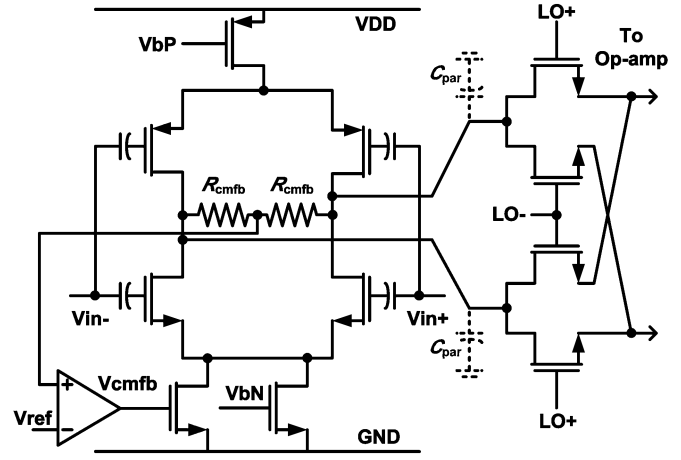


Fig. 3. Transconductance and switching stages.

as a function of frequency and affects the overall linearity of the circuit as well. Analysis specifically concerning IIP₂ of a mixer has been extensively performed in [11] and many of the considerations can be applied to the presented mixer. Since a passive mixer requires a high level of LO drives at the switches, one major concern in this architecture is the LO-RF leakage in the circuit that can degrade the IIP₂ of the system due to finite IIP₃ of the front-end blocks [12].

III. BUILDING BLOCK DESIGNS

We have described the architecture in the previous section with emphasis on system-level tradeoffs in gain, noise, and linearity. In this section, we will focus on implementation of a quadrature demodulator by discussing each of the demodulator building blocks including transconductance stage, switching quad, transimpedance amplifier, and the LO generation circuits.

A. Transconductance

The transconductance stage of the mixer is shown in Fig. 3. It consists of a differential complementary pair and a common-mode feedback circuit. The RF and the LO signals are AC-coupled into the mixer core through several linear metal-insulator-metal (MIM) capacitors. AC-coupling increases biasing flexibility and suppresses low-frequency distortion interaction between stages. The current from the transconductance stage, however, is DC-coupled to the switching pairs. With no capacitor between the stages (used for DC blocking), we realize minimum parasitic capacitance at the transconductance stage output, C_{par} , by reducing the signal routing. It was shown earlier in [3] and in (10) that SNR degradations of the signal due to op-amp noise will increase when the value of C_{par} increases.

Unlike narrowband designs, C_{par} cannot be easily tuned out by using an inductor for all the possible operating frequencies. Since the op-amp is required to have low power consumption, it also constitutes a nontrivial portion of the mixer noise, especially in the $1/f$ region. Minimizing C_{par} allows for a less stringent noise specification upon the op-amp, which favorably translates into lower power-consumption circuit design. On the other hand, absence of DC-blocking capacitors results in

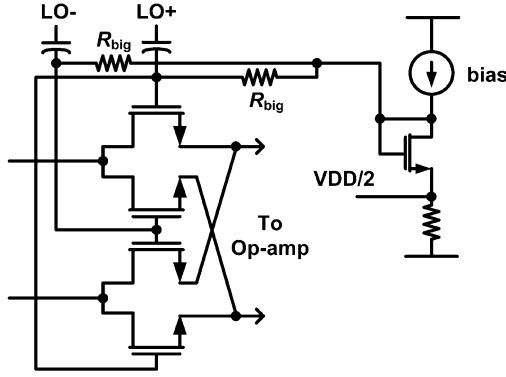


Fig. 4. Replica bias configuration for the switches.

non-zero DC bias current flowing through the switches. This amount of current should be minimized in order to reduce $1/f$ noise contributions from the switches, and was done by careful design of common-mode feedback circuits in both the op-amp and the transconductor.

Since there is no AC-coupling capacitor between this stage and the switches, low-frequency intermodulation tones created by second-order nonlinearity (due to mismatches) will transfer to the next stages downstream. Thus, it is important to reduce the second-order nonlinearity in this stage by using a fully differential topology. Although using the fully differential topology requires extra headroom for the pair due to current-source biasing, the RF voltage swing at this stage is low due to the virtual ground set by an operational amplifier. The nMOS and pMOS devices are biased at high overdrive $V_{gs} - V_{th}$ region in order to achieve high linearity [8]. The common-mode voltages at the mixer and the operational amplifier outputs are set at $V_{dd}/2$ in order to obtain the highest possible headroom for voltage swing. The I/Q mixer altogether with all the bias circuits consume 10 mA.

B. Switches

The switches consist of four transistors forming a double-balanced structure. The DC bias level at the gate of the switches is set where they are operating near threshold of conduction in order to achieve the lowest on-resistance while preventing overlapping on-periods. The overlapping on-periods of the switches result in lowered conversion gain and increased flicker noise from the LO port, while an overlapping off-period will result in linearity degradation [13]. To ensure that the bias voltage tracks with process variation, it is generated by a replica bias circuit as shown in Fig. 4. As mentioned in the previous section, the common-mode voltage level at the drains and sources of the switches is chosen to be $V_{dd}/2$ in order to obtain the highest voltage headroom at the output of the transconductance stage. Assuming the highest allowable gate voltage is V_{dd} , the highest overdrive voltages of the switches will be $V_{dd} - V_{dd}/2 - V_{th}$. If the voltage headroom is not a constraint, the common-mode voltage level can be reduced to allow higher LO voltage swing and higher overdrive voltage of the switches (up to as high as $V_{dd}/2$ for the overdrive). Higher overdrive voltage results in lower average on-resistance of the switches and increases the linearity, gain, and noise performance of the mixer.

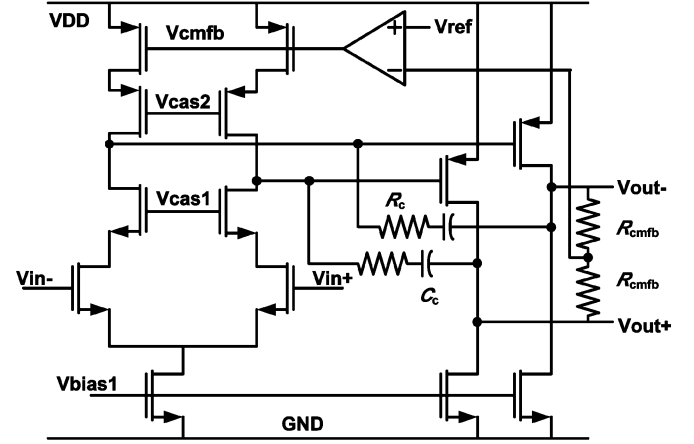


Fig. 5. Simplified operational amplifier schematic.

The switches are sized large enough in order to minimize the on-resistance. However, LO power consumption as well as noise contributions from the operational amplifier determine an upper limit on the size due to associated parasitic capacitances.

C. Operational Amplifier and the Feedback Network

The schematic of the op-amp, shown in Fig. 5, shows a two-stage topology chosen for the op-amp design in order to obtain both high output voltage swing and low input-referred noise. The input-referred spot noise of the op-amp is given by [14]

$$\bar{v}_{n,amp}^2 = 8kT\gamma \frac{1}{g_{mN}^2} \left(\frac{g_{mN}}{\alpha_N} + \frac{g_{mP}}{\alpha_P} \right) \Delta f + \frac{2}{fC_{ox}} \left(\frac{K_N}{(WL)_N} + \frac{K_P}{(WL)_P} \frac{g_{mP}^2}{g_{mN}^2} \right) \Delta f \quad (13)$$

where K_P and K_N are process-dependent constants, α is the ratio g_m/g_{ds0} , and C_{ox} is the gate oxide capacitance per unit area. In order to reduce the op-amp noise contribution, the input nMOS transistors were sized to have a high W/L ratio with a long channel length, while the pMOS have a low W/L ratio with a long channel length. The output stage of the amplifier is simply a common-source stage and provides almost rail-rail output swing. The feedback resistors were chosen to be large in order to reduce the associated thermal noise as shown in (5) and (10). The upper limit of the resistor value was set by the linearity of the circuits. The feedback capacitors are large in order to attenuate the out-of-band blockers [15]. Although using large feedback capacitors creates a low-frequency gain roll-off at the baseband output, this can be characterized and corrected in later stages as long as the noise figure is low and the gain is high enough for the baseband frequency of interest. In practice, available chip area and gain of the circuit determine the upper limit of the capacitor value. The two op-amps (I/Q) draw a total of 3.5 mA from the supply.

D. Frequency Divider and LO Buffers

The LO generation path of the mixer is shown in Fig. 6(a). The first two inverters in parallel act as the input buffer to reshape the high-frequency waveform that is distorted by the packaged pin, bond wire, and pad parasitics. A symmetric LO waveform is critical in ensuring the balanced switch operation

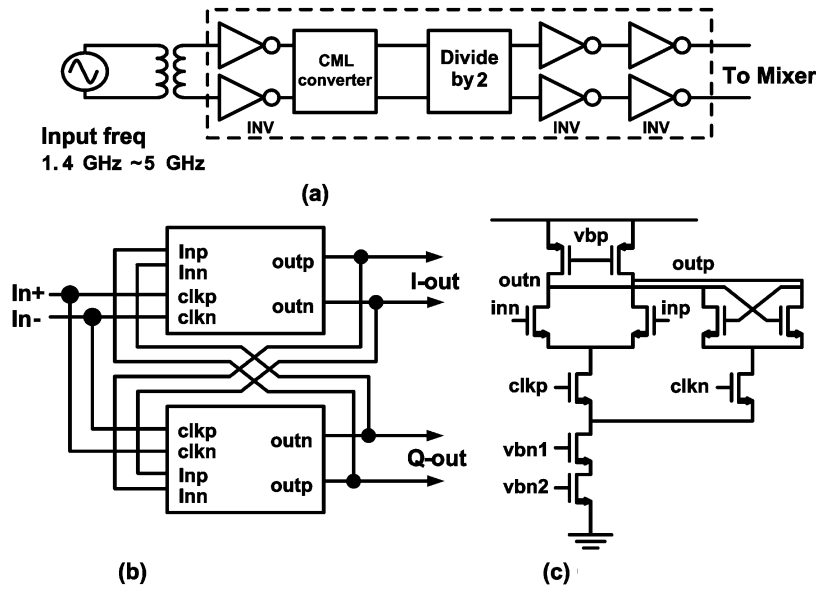


Fig. 6. LO generation circuitry. (a) LO generation path. (b) Frequency divider. (c) CML latch.

so that the switching quad itself does not degrade the mixer noise figure, as well as creating second-order intermodulation products [7], [11]. A divide-by-two frequency scheme is employed to produce 50% LO duty cycle so as to minimize LO asymmetries. The internal LO frequency ranges from 700 MHz to 2.5 GHz, while the divider operates between 1.4 GHz and 5 GHz. This translates into higher power consumption and the need for a larger balun bandwidth. For testing purposes, multiple baluns were used to accommodate the entire frequency range.

The divide-by-two was implemented in current-mode logic (CML) style. The core of the divider block, shown in Fig. 6(b), consists of two CML latches with the output cross toggled back to their inputs. The CML latch circuit diagram is shown in Fig. 6(c). The CML divider draws constant current and has the advantage of generating less current spikes during its dynamic operation which may propagate and appear as noise to other sensitive RF nodes. Because differential signaling is utilized in the CML divider, both I and Q LO outputs with good matching are available. A level converter, placed between the input inverter and CML divider, brings signal from CMOS logic to the CML domain. It consists of two CML stages cascaded as in Fig. 6(c) but without the clocked gate.

Larger LO swing expedites the switching quad transition and helps improve the mixer noise figure and second-order intermodulation product [7], [11]. The mixer core design requires the LO differential swing of at least $1.5 V_{pk-pk}$ from a supply of 1.5 V. Two scaled inverters are cascaded in each path to provide sufficient drive capability. The CML circuits (I/Q) consume a total of 1.43 mA.

IV. EXPERIMENTAL RESULTS

A. Measurement Setup

The prototype chip was fabricated in a 0.13- μm CMOS technology and occupies a total area of 0.8 mm by 1 mm. All the

signal and bias pads were ESD protected. 60% of the chip area was allocated to the feedback capacitors of the op-amps. The packaged chip was mounted on the PCB board for testing and on-board baluns were used to perform single-ended-to-differential conversion at the mixer and LO inputs. An external 100- Ω resistor was placed at the mixer RF input to provide the input matching for measurement purposes. At the output of the chip, buffers were used to convert the differential outputs to a single ended output and to drive low-impedance measurement cables. Noise contributions from the buffers were significant at base-band frequencies higher than 2 MHz due to mixer gain roll-off and were de-embedded by estimating the total noise contribution of the buffer from equivalent circuit models obtained from the component provider and then subtracting it out from the output noise. Detailed measurements were done at 900 MHz and 2.1 GHz, near the two ends of the intended operating frequency range. The results can be interpolated into other operating frequencies due to the wideband nature of the circuit.

B. Measurement Results

The conversion gain plot for 900 MHz and 2.1 GHz is shown in Fig. 7. Conversion gain at 1 kHz and the -3 dB bandwidth of the mixer for inputs from 700 MHz to 2.5 GHz are plotted in Fig. 8. The measured conversion voltage gain is close to 38.5 dB and the internal voltage gain of the mixer is approximately 3 dB below the measured gain due to 3 dB voltage gain of the balun.

Since the baluns were glued on the same PCB board with the mixer chip, leaving no probing space in between for characterizing the balun loss at different frequencies, the measured mixer gain, noise, and linearity values reported here reflect the combined effect and show a variation of roughly 1 dB. This effect is clearly depicted in Figs. 8 and 10. The simulated gain increases with the LO frequency due to high-pass characteristics of the AC-coupling networks. Measured gain stays within 1 dB of the simulation values and shows variation that is expected to come from balun mismatches as mentioned earlier. The gain drops

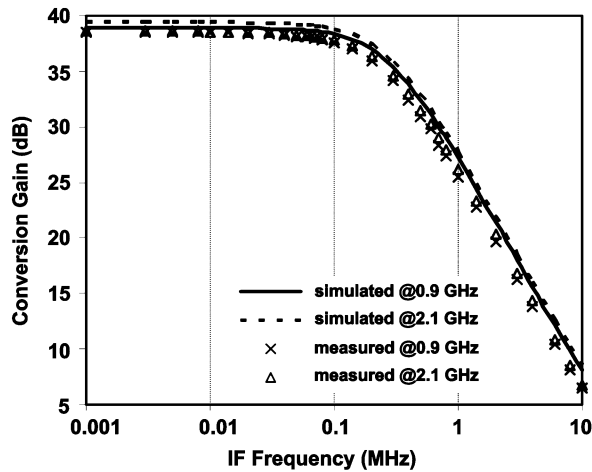
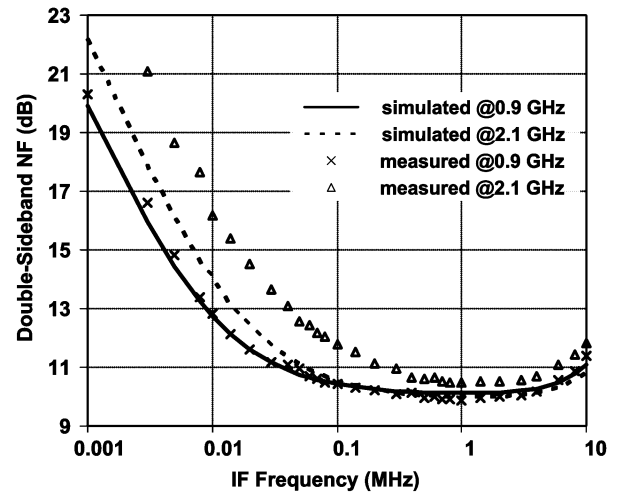
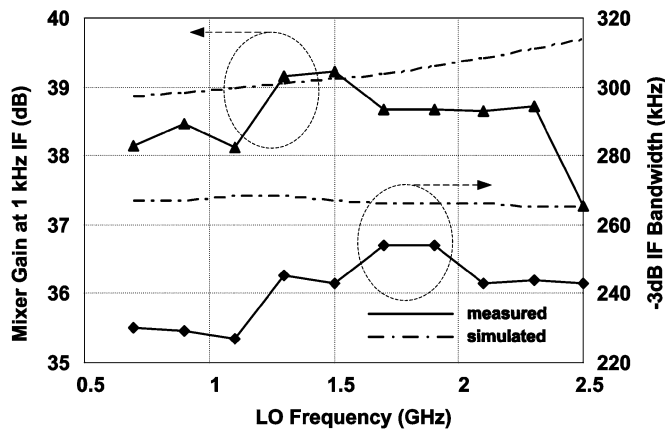
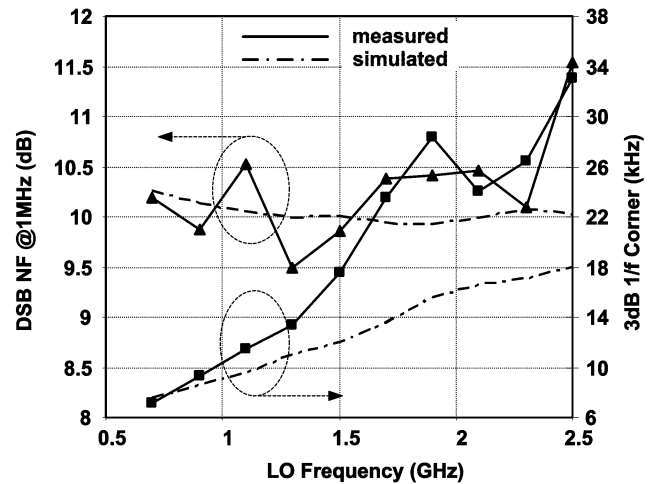
Fig. 7. Gain plots at 900 MHz and 2.1 GHz f_{LO} .Fig. 9. Measured double-sideband noise figure at 900 MHz and 2.1 GHz f_{LO} .

Fig. 8. Measured conversion gain and bandwidth.

Fig. 10. Noise characteristics at different f_{LO} .

significantly at 2.5 GHz and is due to the effect of balun loss and the resulting lower LO drives into the switches.

The measured double-sideband noise figure (DSB NF) at 900 MHz and 2.1 GHz are shown in Fig. 9. In addition, the DSB NF at 1-MHz baseband frequency and 1/f noise corner at different LO frequencies are shown in Fig. 10. Variations in noise figure across LO frequencies is due to effects from different balun losses across the frequency range. The measured noise figure floor is near 10 dB or 2.89 nV/sqrt(Hz) and the 1/f noise corner is lower than 35 kHz across the LO frequency range. Taking into account the effect of single-ended to differential conversion, the on-chip input-referred voltage noise floor would be 4.07 nV/sqrt(Hz) assuming perfect a balun were used. The 1/f noise increases with higher LO frequency because of higher 1/f noise contribution from the operational amplifier as predicted from (10). However, the 1/f noise corner increases faster than expected as a function of LO frequency and the potential cause is due to parasitic capacitances at the transconductance output. Although not experimentally verified, the amount of 1/f noise is expected to rise with the presence of a blocking signal due to higher RMS currents flowing through

the switches [16]. Measured noise figure increases significantly at 2.5 GHz.

The two-tone linearity test results are shown in Fig. 11 for 900 MHz and 2.1 GHz LO frequencies. The intermodulation (IM) products are located in-band at 30 kHz for all cases. For example, the 1-MHz frequency offset means the input signals are located at 1-MHz and 1.03-MHz offsets for IIP₂ tests while the inputs tones for IIP₃ tests are located at 1-MHz and 2.03-MHz offsets. All the input-referred intercept points were calculated from the input-referred powers of the IM products. At very low IF frequency, IIP₃ and IIP₂ increase as the gain decrease as suggested by (12). Above 2-MHz IF, IIP₃ and IIP₂ flatten out or start to decrease due to limitations from the transconductance and the switches nonlinearity as well as lowered op-amp loop gain. The op-amp loop gain reduces at high frequency due to gain roll-off in the op-amp open-loop transfer function. At 1-MHz offset, the achieved IIP₃ is +11 dBm and average IIP₂ is +64 dBm. IIP₂ is measured with five samples and the minimum is higher than +60 dBm at this frequency. In Fig. 11, one observes an abrupt IIP₃ and IIP₂ dip at baseband offset around 5 MHz. This is attributed to an unintended peaking in the op-amp's common-mode transfer function. The problem can

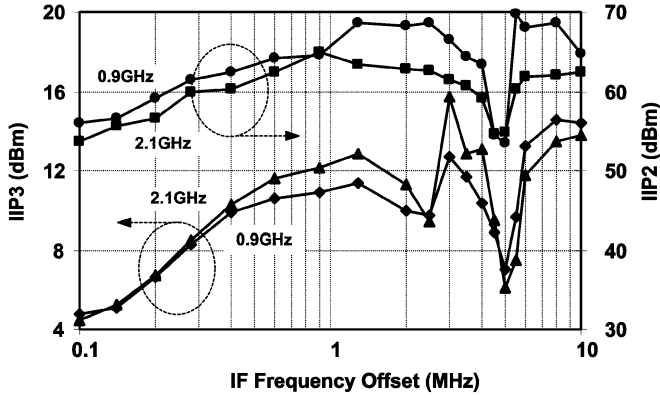
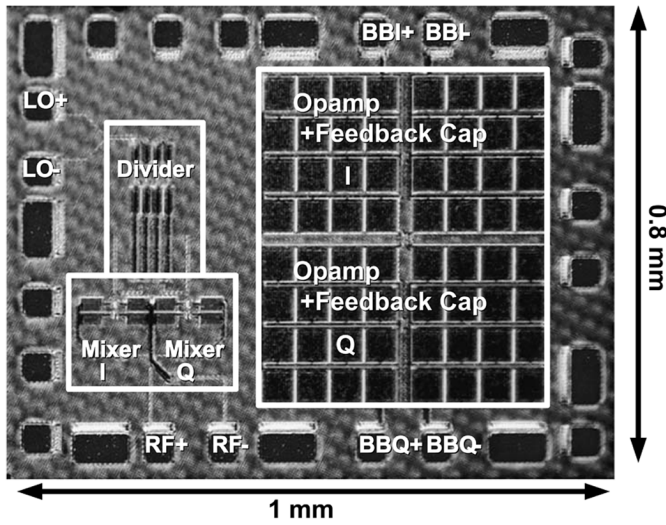

 Fig. 11. Measured IIP_2 and IIP_3 at 900 MHz and 2.1 GHz.


Fig. 12. Microphotograph of the chip.

be prevented in the future designs by carefully modifying the common-mode circuit.

The 1-dB compression point (P_{-1dB}) of the circuit is limited by the output swing and varies with the frequency offset of the blocking signals. For 900-MHz f_{LO} , the measured input-referred P_{-1dB} at 100-kHz, 1-MHz, and 10-MHz offsets are -25.8 dBm, -13.5 dBm, and -5.6 dBm, respectively. For the input power of -26 dBm at 100-kHz offset, the output voltage is approximately 0.7 V_{p-p} on each side of the differential outputs. At this condition, the gain of the transimpedance amplifier drops rapidly as a function of V_{out} amplitude and the compression is caused by higher order distortions as well as rapidly decreasing loop gain at the same time. In other words, feedback does not help linearize the circuit at very high output voltage level due to significant gain compression in the “feed-forward” path. As the blocker offset moves from 0.1 MHz to 1 MHz, IIP_3 increases by 7 dB while P_{-1dB} increases by 12 dB. Similarly, IIP_3 increases by less than 3 dB but P_{-1dB} increases by 8 dB when the offset moves from 1 MHz to 10 MHz. The compression point can be increased either by decreasing Z_f or decreasing the transconductance of the input stage. Both methods have negative effects on the noise figure,

 TABLE I
 DEMODULATOR PERFORMANCE SUMMARY

Specification	Value	
Process Technology	0.13 μ m CMOS	
Supply Voltage	1.5 V	
Total Bias Current	20 mA – 24 mA	
Voltage conversion gain	35.5 dB	
Output -3 dB Bandwidth	250 kHz	
Operating Frequency	0.7 GHz - 2.56 GHz	
IIP_3 @ 1 MHz Offset	0.9 GHz	11 dBm
	2.1 GHz	12 dBm
IIP_2 @ 1 MHz Offset	0.9 GHz	60 dBm minimum
	2.1 GHz	
DSB NF@ 1 MHz Offset	0.9 GHz	10 dB
	2.1 GHz	10.5 dB
1/f 3 dB Corner	0.9 GHz	10 kHz
	2.1 GHz	26 kHz
LO Leakage at the RF Port	-74 dBm rms	

but the effect can be low depending on how much noise is contributed by Z_f and by the op-amp. The measured LO leakage at the RF port was -74 dBm on average with the maximum value of -62 dBm. The measured output offset is 19.5 mV_{rms}. The measured I-Q gain imbalance at 100-kHz offset varies from 0.03 dB to 0.1 dB with different LO frequencies. The phase imbalance, however, varies strongly from 0.3° to 10° with different baluns, LO frequencies, and external LO power at $2f_{LO}$. The variation in phase matching comes from duty cycle error of the signal hitting the on-chip LO divider and can be solved by using an on-chip divide-by-four circuit to generate I-Q LO drives. The measured performance is summarized in Table I. The total chip including bias circuitry consumes 20 mA at 700 MHz and 24 mA at 2.5 GHz from a 1.5-V supply. The highest operating frequency is up to 2.56 GHz and is limited by the frequency divider. A microphotograph of the prototype is shown in Fig. 12. Table II shows the comparison of this work to other published wideband inductorless mixer designs operating in similar frequency bands. The comparisons show that this design achieves very high conversion gain and competitive linearity, noise figure, and power consumption compared to the other recently published inductorless mixer works.

V. CONCLUSION

A low 1/f noise inductorless quadrature demodulator is presented. A fully differential complementary pair was used to increase the efficiency of the transconductance. The circuit operates over a wide range of frequencies including the 0.7–2.5-GHz frequency bands.

To get an estimate on overall receiver performance if this mixer is integrated as a part of an RF front-end, we can assume that a wideband differential low-noise amplifier (LNA) with a conversion gain of 14 dB, noise figure (NF) of 2.4 dB, and

TABLE II
COMPARISONS WITH PREVIOUS WORKS

Parameters	[4]	[5]	[18]	[20]	This Work
Frequency	2.4 GHz	900 MHz	0.8 – 2.1 GHz	0.1 – 3.85 GHz	0.9 GHz - 2.3 GHz
Voltage Conversion Gain	15.7 dB	18 dB	9.0 dB – 11.7 dB	20 dB	34.5 dB – 35.5 dB
IF Bandwidth	Not Reported	Not Reported	600 kHz – 1.2 MHz	70 MHz (For Low-IF)	250 kHz
Noise Figure	9.9 dB DSB	10 dB SSB	8.8 dB – 9.4 dB DSB	8.4 dB - 11.5 dB SSB	9.5 dB - 11.5 dB DSB
1/f Noise Corner	Not Given	5 kHz	Not Given	Not Given	9 kHz – 33 kHz (No Blocker)
IIP ₃	1 dBm	- 4 dBm	7.8 dBm - 10.7 dBm	Not Reported	4 dBm @ 0.1 MHz IF 11 dBm @ 1 MHz IF
IIP ₂	Not Reported	30 dBm	54.6 dBm - 56.4 dBm	Not Reported	52 dBm @ 0.1 MHz IF 60 dBm @ 1 MHz IF
Technology	0.18- μ m CMOS	0.35- μ m CMOS	90-nm CMOS	90-nm CMOS	0.13- μ m CMOS
Vdd	1.8 V	2.7 V	Not Reported	1.2 V	1.5 V
Total Bias Current	4.5 mA	6 mA	7.55 mA - 12.46 mA	8.15 mA	20 mA – 24 mA
Note	One Mixer	One Mixer	Bias with Off-Chip Chokes I/Q Mixers + Divider	LNA + Mixer (Not I/Q)	I/Q Mixers + Divider

IIP₃ of 0 dBm can be achieved [17]. The combined front-end would have 49 dB of voltage gain, 3.2 dB noise figure, IIP₃ of -4.5 dBm, and IIP₂ of +46 dBm. Lower mixer gain and higher linearity can be obtained by reducing the feedback impedance of the transimpedance stage at the mixer output, at the cost of higher noise figure of the system. The feedback resistors and capacitors can be made programmable using MOS switches as well to increase design flexibility. A mechanism when integrating with the LNA is the IIP₂ degradations of the front-end due to LO leakage and finite IIP₃ of the circuits should be considered as well in the design [12].

Another consideration when implementing a front-end using this mixer architecture is that the LO generations will be implemented with an integrated voltage-controlled oscillator (VCO). This VCO has to be properly design to minimize LO leakages into other parts of the circuits. This issue can be alleviated by choosing a VCO running frequency that is not an integer multiple of f_{LO} as being used in [18].

ACKNOWLEDGMENT

The authors would like to thank Infineon Technologies for providing chip fabrication and BWRC industrial members for their support. The authors would also like to thank Henry Jen, Luns Tee, and Gang Liu for their help and insights during measurements.

REFERENCES

- [1] S. Zhou and M. F. Chang, "A CMOS passive mixer with low flicker noise for low-power direct-conversion receiver," *IEEE J. Solid-State Circuits*, vol. 40, no. 5, pp. 1084–1093, May 2005.
- [2] M. Valla, G. Montagna, R. Castello, R. Tonietto, and I. Bietti, "A 72-mW CMOS 802.11a direct-conversion front-end with 3.5-dB NF and 200-kHz 1/f noise corner," *IEEE J. Solid-State Circuits*, vol. 40, no. 4, pp. 970–977, Apr. 2005.
- [3] E. Sacchi, I. Bietti, S. Erba, L. Tee, P. Vilmercati, and R. Castello, "A 15 mW, 70 kHz 1/f corner direct conversion CMOS receiver," in *Proc. IEEE Custom Integrated Circuits Conf.*, San Jose, CA, Sep. 2003, pp. 459–462.
- [4] V. Vidojkovic, J. Tang, A. Leeuwenburgh, and A. H. M. Roermund, "A low voltage folded-switching mixer in 0.18- μ m CMOS," *IEEE J. Solid-State Circuits*, vol. 40, no. 6, pp. 1259–1264, Jun. 2005.
- [5] D. Manstretta, R. Castello, and F. Svelto, "Low 1/f noise CMOS active mixers for direct conversion," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 48, no. 9, pp. 846–850, Sep. 2001.
- [6] T. H. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*, 1st ed. Cambridge, U.K.: Cambridge Univ. Press, 1998.
- [7] H. Darabi and A. A. Abidi, "Noise in RF-CMOS mixers: A simple physical model," *IEEE J. Solid-State Circuits*, vol. 35, no. 1, pp. 15–25, Jan. 2000.
- [8] M. Brandolini, P. Rossi, D. Sanzogni, and F. Svelto, "A +78 dBm IIP2 CMOS direct conversion mixer for fully integrated UMTS receivers," *IEEE J. Solid-State Circuits*, vol. 41, no. 3, pp. 552–559, Mar. 2006.
- [9] M. T. Terrovitis and R. G. Meyer, "Intermodulation distortion in current-commutating CMOS mixers," *IEEE J. Solid-State Circuits*, vol. 35, no. 10, pp. 1461–1473, Oct. 2000.
- [10] P. Gray, P. Hurst, S. Lewis, and R. Meyer, *Analysis and Design of Analog Integrated Circuits*, 4th ed. New York: Wiley, 2001.
- [11] D. Manstretta, M. Brandolini, and F. Svelto, "Second-order inter-modulation mechanisms in CMOS downconverters," *IEEE J. Solid-State Circuits*, vol. 38, no. 3, pp. 394–406, Mar. 2003.
- [12] I. Elahi, K. Muhammad, and P. T. Balsara, "IIP2 and DC offsets in the presence of leakage at LO frequency," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 53, no. 8, pp. 647–651, Aug. 2006.
- [13] A. Shahani, D. K. Shaeffer, and T. H. Lee, "A 12-mW wide dynamic range CMOS front-end for a portable GPS receiver," *IEEE J. Solid-State Circuits*, vol. 32, no. 12, pp. 2061–2070, Dec. 1997.
- [14] B. Razavi, *Design of Analog CMOS Integrated Circuits*. New York: McGraw-Hill, 2001.

- [15] V. Aparin *et al.*, "A fully-integrated highly linear zero-IF CMOS cellular CDMA receiver," in *IEEE Int. Solid-State Circuits Conf. 2005 Dig. Tech. Papers*, San Francisco, CA, Feb. 2005, pp. 324–325.
- [16] D. Leenaerts and W. Redman-White, "1/f noise in passive CMOS mixers for low and zero IF integrated receivers," in *Proc. 27th Eur. Solid-State Circuits Conf.*, Villach, Austria, 2001, pp. 103–107.
- [17] F. Bruccoleri, E. Klumperink, and B. Nauta, "Wide-band CMOS low-noise amplifier exploiting thermal-noise canceling," *IEEE J. Solid-State Circuits*, vol. 39, no. 2, pp. 275–282, Feb. 2004.
- [18] A. Behzad *et al.*, "Direct-conversion CMOS transceiver with automatic frequency control for 802.11a wireless LANs," in *IEEE Int. Solid-State Circuits Conf. 2003 Dig. Tech. Papers*, San Francisco, CA, Feb. 2003, pp. 356–499.
- [19] S. Peng, C. Chen, and A. Bellaouar, "A wideband mixer for WCDMA/CDMA2000 in 90 nm CMOS digital CMOS process," in *Proc. IEEE Radio Frequency Integrated Circuits (RFIC) Symp.*, 2005, pp. 179–182.
- [20] A. Amer, E. Hegazi, and H. F. Ragaie, "A 90-nm wideband merged CMOS LNA and mixer exploiting noise cancellation," *IEEE J. Solid-State Circuits*, vol. 42, no. 2, pp. 323–328, Feb. 2007.



in CMOS technologies.

Nuntachai Poobupheun (S'01) received the B.Eng. degree in electrical engineering from Chulalongkorn University, Bangkok, Thailand, in 2002, and the M.S. degree in electrical engineering from the University of California, Berkeley, in 2005, where he is currently working toward the Ph.D. degree.

In summer 2006, he held an internship position at Rambus Inc., Los Altos, CA, where he worked on high-speed analog front-end for serial links. His research has been on analog and RF circuits, with an emphasis on wideband receiver front-end designs



Wei-Hung Chen (S'03) received the B.S. and M.S. degrees in electrical engineering from National Taiwan University, Taipei, Taiwan, R.O.C., in 1998 and 2000, respectively.

Between 2000 and 2002, he served as IT Second Lieutenant in the Army of R.O.C. In 2003, he was with the Industrial Technology and Research Institute, Hsin-Chu, Taiwan, for six months, developing a clock synchronizer for a tri-mode WCDMA/GSM/DCS receiver. Since fall 2003, he has been with the Department of Electrical Engineering and Computer Science at the University of California, Berkeley, where he is currently working toward the Ph.D. degree. During the summers of 2005 and 2006, he interned in the wireless group at Maxim Integrated Products, Sunnyvale, CA, where he worked on various blocks of two high data-rate WAN chips. His current research focuses on linearization schemes of frond-end circuits and architecture for enabling cognizant universal radios. His research interest includes accurate distortion modeling for advanced CMOS devices.

Mr. Chen received the Outstanding Student Design Award from Analog Device Inc. and the IEEE MTT-S Graduate Student Fellowship, both in 2007.



Zdravko Boos received the B.S.E.E. degree from the University of Zagreb, Croatia, in 1982, and the M.S.E.E. degree from the Eindhoven International Institute, Eindhoven, The Netherlands, in 1991.

From 1983 to 1989, he was with Institute for Electronics in Zagreb, where he was involved in the development of UHF frequency synthesizers. From 1991 to 1998, he was with Philips Consumer Electronics in Eindhoven, where he developed DAB front-ends for DAB 452 and DAB 752 receivers. In 1989, he joined Siemens Semiconductors/Infineon Technologies, where he was developing RF concepts for advanced multimode transceivers. He is currently a Senior Principal Wireless Communications RF Engineer with Infineon Technologies, Munich, Germany. His technical interests are in the digital transmitter and receiver concepts in deep-submicron CMOS technology. He holds several EU and U.S. patents.



Ali M. Niknejad (S'93–M'00) received the B.S.E.E. degree from the University of California, Los Angeles, in 1994, and the Master's and Ph.D. degrees in electrical engineering from the University of California, Berkeley, in 1997 and 2000. During his graduate studies, he authored *ASITIC*, a CAD tool that aids in the simulation and design of passive circuit elements such as inductors into silicon integrated circuits. *ASITIC* is actively used by industry and academic research and development centers.

After graduation from Berkeley, he worked in industry, focusing on the design and research of analog RF integrated circuits and devices for wireless communication applications. He is currently an Associate Professor in the EECS Department at the University of California, Berkeley, and co-director of the Berkeley Wireless Research Center and the BSIM Research Group. His research interests lie in the area of wireless and broadband communications, including the implementation of integrated communication systems in silicon using CMOS, SiGe, and BiCMOS processes. Focus areas of his research include analog and RF circuits, device physics and modeling, and numerical techniques in electromagnetics, with an emphasis on the analysis and modeling of active and passive devices at microwave frequencies for IC applications.

Prof. Niknejad was a co-recipient of the Outstanding Technology Directions Paper at ISSCC 2004 for co-developing a modeling approach for devices up to 65 GHz. He has served as an associate editor of the *IEEE JOURNAL OF SOLID-STATE CIRCUITS* and is now serving on the Technical Program Committees for CICC and ISSCC.