

A Highly Linear Broadband CMOS LNA Employing Noise and Distortion Cancellation

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Abstract—This paper presents a broadband very low 3^{rd} -order intermodulation inductor-less low-noise amplifier (LNA) implemented in $0.13\ \mu\text{m}$ CMOS technology. The LNA consists of a common-gate input stage for wideband impedance matching, followed by two parallel common source amplifiers which perform noise and distortion cancellation. Third-order distortion due to amplifier's second-order interaction is further minimized by employing a low second-order distortion PMOS/NMOS input pair. This LNA achieves $+16\ \text{dBm}$ IIP_3 in both the 900 MHz and 2 GHz bands. The LNA maintains minimum internal gain $14.5\ \text{dB}$, noise figure below $2.6\ \text{dB}$ from 800 MHz-2.1 GHz while drawing $11.6\ \text{mA}$ from a supply of 1.5V .

I. INTRODUCTION

The design of a multi-standard multi-band front-end requires a high linearity and low-noise over a wide frequency range. Even in a “digital” receiver application, employing discrete-time signal processing, requires a linear front-end amplifier to reject the noise and relax the performance of the samplers. Conventional solutions employ parallel narrowband receiving paths at cost of die and board area, high pin count, and lack of reconfigurability. Much research activity has focused on the design of a tunable or wideband front-end amplifier. For instance [1] uses multi-band feedback in conjunction with a common-gate input stage to realize a tunable narrowband amplifier, so that the input pin can be shared. Recently, feasibility of deep sub-micron CMOS technology for ultra-wideband systems has been demonstrated up to 10 GHz [2][3]. Exploiting high f_T/f_{max} transistors available from nano-scale CMOS, an inductor-less ultra-wideband LNA with performances comparable to a narrowband counterpart has been reported [4]. While the noise and bandwidth of nano-scale CMOS improve with scaling, unfortunately on the linearity deteriorates with low supply voltage and high-field mobility effects. High V_t transistor or elevated supply voltage are used in [3] and [4] to achieve the reported IIP_3 .

Prior-art MOSFET LNA linearization schemes manipulated the different polarity of the 2^{nd} -order g_m derivative from weak to strong inversion region and have achieved high IIP_3 in narrowband application [5]. Noise cancellation LNAs with wideband matching and low noise figure [6] have been demonstrated. In this work we demonstrate that if we incorporate the intrinsic device properties together with noise and distortion cancellation, an LNA with wideband input matching, low noise and high linearity can be realized. Since a cascade amplifier is used to subtract the noise of input transistor in the noise cancellation LNA, another source of 3^{rd} -order distortion is

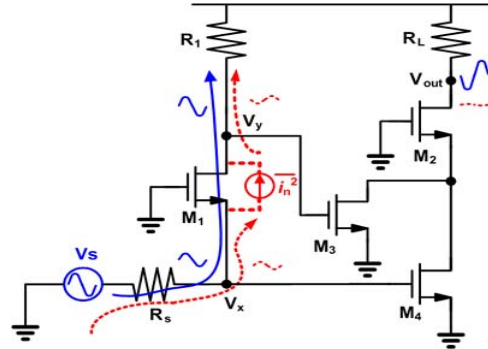


Fig. 1. Simplified small-signal schematic.

created by amplifier's 2^{nd} -order interaction. We will demonstrate that in a noise/distortion cancellation topology, this source of distortion dominates the overall distortion of the amplifier. By proper care in the design of the transconductance amplifier, we present an amplifier that achieves both noise and distortion cancellation. The target application for this design is for multi-mode 3GPP systems, while the techniques are generally applicable to many wireless communication systems.

II. WIDEBAND AMPLIFIER NOISE CANCELLATION DESIGN

Fig. 1 shows the simplified small-signal schematic of the noise cancellation LNA. A similar amplifier was presented by [7] but does not incorporate distortion cancellation. The input signal (solid line) undergoes feedforward amplification whereas the channel thermal noise (dotted line) of transistor M1 undergoes subtraction at output node due to two correlated but out-of-phase noise voltages at V_x and V_y . At low frequencies, the input impedance Z_{in} , voltage gain A_v and noise factor F are given by

$$Z_{in} = \frac{R_1 + r_{o1}}{1 + g_{m1}r_{o1}} \quad (1)$$

$$A_v = \left[g_{m4} + g_{m3} \left(\frac{1 + g_{m1}r_{o1}}{1 + \frac{r_{o1}}{R_1}} \right) \right] \times R_L \quad (2)$$

$$F = 1 + \frac{g_{m3}^2 R_1 + \frac{\gamma}{\alpha} \left(g_{m3} + g_{m4} + g_{m1} R_T^2 \left(g_{m3} \frac{R_1}{R_s} - g_{m4} \right)^2 \right)}{R_L^{-2} R_s^{-1} \cdot (R_s \parallel Z_{in})^2 \cdot A_v^2} \quad (3)$$

where $R_T = R_s \parallel \frac{r_{o1}}{1 + \frac{r_{o1}}{R_1}} \parallel \frac{1}{g_{m1}}$. The first, second and third term in the numerator of Eq. 3 refer to noise contribution of R_1 , M_3 ,

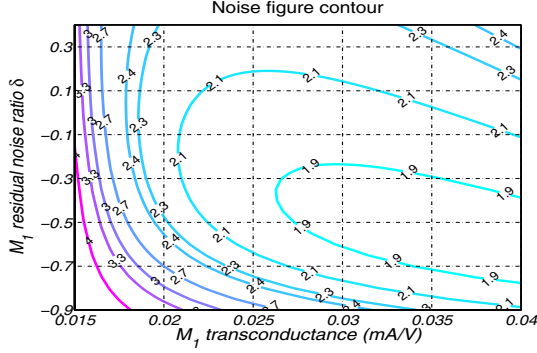


Fig. 2. NF contour with $S_{11}=-20$, $A_v=18$ dB, total $g_m=100$ mS.

and M_4 respectively. The residual M_1 noise after cancellation, the fourth term, can be formulated as a residual factor $g_{m3} \frac{R_1}{R_s} \delta$. By incorporating S_{11} and A_v constrains, a design equation for F is derived

$$F = 1 + \frac{R_1 + \frac{\gamma}{\alpha} \left(\frac{1}{g_{m3}} \left(1 + \frac{R_1}{R_s} (1 + \delta) \right) + g_{m1} \delta^2 R_T^2 \left(\frac{R_1}{R_s} \right)^2 \right)}{R_s \left(\frac{1 + \varepsilon_{rr}}{1 + \varepsilon_{rr}} \right)^2 A_v^2 g_{m3}^{-2} R_L^{-2}} \quad (4)$$

where $Z_{in} = R_s (1 + \varepsilon_{rr})$ represents the impedance matching criteria. A contour analysis based on Eq. 4 is shown in Fig. 2 indicating robust noise cancellation centered around the upper-middle of the contour.

III. WIDEBAND DISTORTION CANCELLATION DESIGN

Volterra series analysis is conducted to understand in detail the distortion characteristics of the common-gate stage in Fig. 1. By denoting

$$V_x = A_1(\omega) \circ V_s + A_2(\omega_1, \omega_2) \circ V_s^2 + A_3(\omega_1, \omega_2, \omega_3) \circ V_s^3 \quad (5)$$

$$V_y = B_1(\omega) \circ V_s + B_2(\omega_1, \omega_2) \circ V_s^2 + B_3(\omega_1, \omega_2, \omega_3) \circ V_s^3 \quad (6)$$

and nonlinear transconductance, $i_d = g_m \times V_s + \frac{g'_m}{2!} \times V_s^2 + \frac{g''_m}{3!} \times V_s^3$, the 1st, 2nd, and 3rd-order Volterra operators ($A_1, B_1, A_2, B_2, A_3, B_3$) are derived as

$$A_1(\omega) = \frac{Z_1 + r_{o1}}{H(\omega)} \quad (7)$$

$$A_2(\omega_1, \omega_2) = \frac{\frac{1}{2} g'_{m1} r_{o1} R_s A_1^2}{H(\omega_1 + \omega_2)} \quad (8)$$

$$A_3(\omega_1, \omega_2, \omega_3) = \frac{-R_s r_{o1} (-g'_{m1} \overline{A_1 A_2} + \frac{1}{6} g''_{m1} A_1^3)}{H(\omega_1 + \omega_2 + \omega_3)} \quad (9)$$

$$H(\omega) = j\omega(Z_1 + r_{o1})R_s C_1 + Z_1 + r_{o1} + R_s + g_{m1} r_{o1} R_s \quad (10)$$

and

$$B_1(\omega) = \frac{Z_1 \times (1 + g_{m1} r_{o1})}{Z_1 + r_{o1}} A_1(\omega) = \frac{Z_1}{R_{in}} A_1(\omega) \quad (11)$$

$$B_2(\omega_1, \omega_2) = \frac{-Z_1 \times (1 + j(\omega_1 + \omega_2) C_1 R_s)}{R_s} A_2(\omega_1, \omega_2) \quad (12)$$

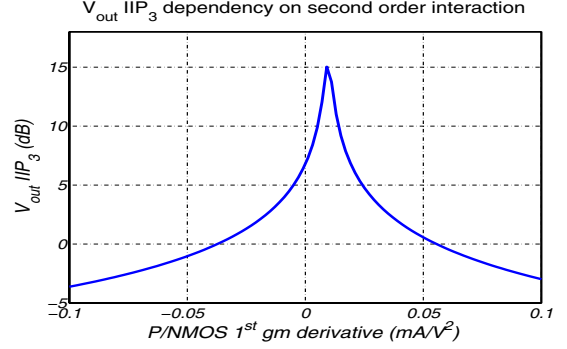


Fig. 3. V_{out} IIP₃ versus g'_m , nominal $g_{m'_{p,n}} = \pm 42$ (mA/V²).

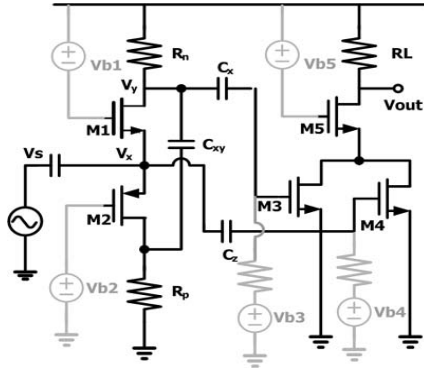
$$B_3(\omega_1, \omega_2, \omega_3) = \frac{Z_1 (1 + j(\omega_1 + \omega_2 + \omega_3) C_1 R_s)}{-R_s} A_3(\omega_1, \omega_2, \omega_3) \quad (13)$$

where Z_1, C_1 are the load impedance/source capacitance at M_1 drain and source respectively, $\overline{A_1 A_2}$ represents the 2nd-order interaction operator. V_x, V_y are then amplified by transistors M_3 and M_4 with corresponding g_m and its derivatives. A memoryless polynomial distortion representation is applied to M_3 and M_4 since the simple common source plus cascode topology is wideband due to the high device f_T . The fundamental and 3rd-order V_{out} expressions are given by

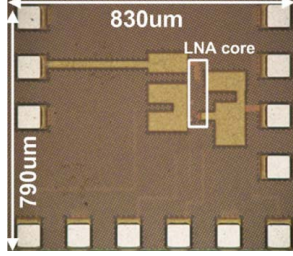
$$\begin{aligned} V_{out, fund} &= ((A_1 \circ V_s) \times g_{m4} + (B_1 \circ V_s) \times g_{m3}) \times R_L \\ V_{out, 3rd} &= [((A_3 \circ V_s^3) \times g_{m4} + (B_3 \circ V_s^3) \times g_{m3}) \\ &\quad + \left((A_1 \circ V_s)^3 \times \frac{g''_{m4}}{6} + (B_1 \circ V_s)^3 \times \frac{g''_{m3}}{6} \right) \\ &\quad + ((\overline{A_1 A_2} \circ V_s^3) \times g'_{m4} + (\overline{B_1 B_2} \circ V_s^3) \times g'_{m3})] \times R_L \end{aligned} \quad (15)$$

In order to deconvolve Eq. 15, first consider low frequencies and assume an impedance match, so the ratio of $\frac{A_1}{B_1}, \frac{A_2}{B_2}, \frac{A_3}{B_3}$ reduces to $\frac{R_s}{R_1}, \frac{R_s}{-R_1}$ and $\frac{-R_s}{R_1}$ respectively. All of them contribute to the 3rd-order intermodulation at V_{out} . The first term in Eq. 15 is due to M_1 's 3rd-order distortion and cancels out in the same vein as the mechanism that cancels M_1 's channel noise. The second term is due to M_3 and M_4 's 3rd-order distortion and is canceled by properly biasing M_3/M_4 at weak and strong inversion region to create a different polarity of g''_{m3} and g''_{m4} . Up until this point, optimum size and bias of M_3/M_4 are set to allow the aforementioned noise and distortion cancellation to take effect.

The third contribution in Eq. 15 is the 2nd-order interaction which exists in any cascode and feedback system. Despite the reverse polarity of $\overline{A_1 A_2}$ and $\overline{B_1 B_2}$, and the same polarity of g'_{m3} and g'_{m4} , the residual IM_3 after subtraction can still be substantial because of the device size/bias chosen by the previous cancellation schemes. As mentioned in [8] and also independently found by the authors, a PMOS in an inverter-type configuration exhibits the same g_m and g'_m polarity as an NMOS while exhibiting different g'_m . This IM_2 property of an inverter pair is thus incorporated into the input common gate stage such that a new degree of freedom for



(a) Complete LNA schematic.



(b) Chip microphotograph.

Fig. 4. Full schematic and chip photo

adjusting $(\overline{A_1 A_2}, \overline{B_1 B_2})$ is obtained without affecting previous distortion/noise cancellations.

Since $Z_1 \cdot (j\omega R_s C_1 + 1)$, the ratio of transistors M_3/M_4 for distortion cancellation, is insensitive to frequency change, low IM_3 at V_{out} is obtained over a wide frequency range. Extracting device parameters from simulations with foundry's BSIM4 model and substituting the bias conditions used in this LNA, a calculation on IIP_3 versus 2^{nd} -order interaction is shown in Fig. 3. It is clear that given the real circuit parameter values, the 2^{nd} -order interaction reshapes the 3^{rd} -order distortion substantially.

IV. IMPLEMENTATION

A 0.8-2.1 GHz LNA based on the above noise/distortion cancellation schemes was designed and fabricated in $0.13\mu\text{m}$ CMOS technology with standard- V_t transistors. The full circuit schematic is shown in Fig. 4(a). In addition to a reduced g'_m , the complementary PMOS/NMOS pair reuses the DC current and simplifies the bias for the input stage. Capacitor C_{xy} is inserted between drain of M_1 and M_2 to equalize V_x and V_y at signal frequency. Because each transistor requires different voltage levels, AC coupling of signals between transistors are utilized with linear MIM capacitors for maximum tuning flexibility. Unlike in narrow-band design, the size of these capacitors are chosen large enough so that they do not redistribute IM_2 which adversely alters the circuit behavior on which the Volterra series analysis is based. Resistor R_L is sized close to 50Ω in order to eliminate the use of output buffer for measurement which potentially limits the observable LNA linearity. Due to a very low value of R_L , the simulated IIP_3 only shows a small difference when measured on-chip,

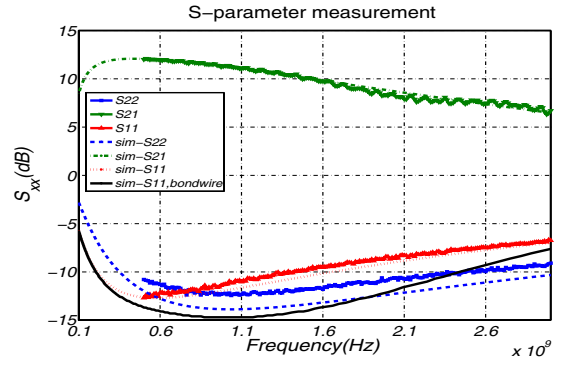


Fig. 5. Measured S parameters

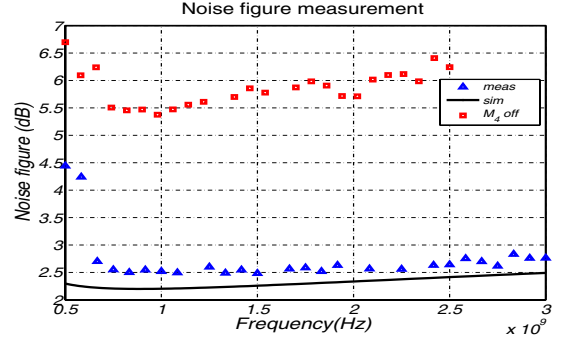


Fig. 6. Measured noise figure

with 6 dB increase of gain. The entire chip in Fig. 4(b) takes up $830 \times 790\mu\text{m}^2$ die area while the circuit core is only $320 \times 310\mu\text{m}^2$ including MIM capacitors.

V. MEASUREMENT RESULTS

The chip is measured by on-wafer probing. The S -parameter results in Fig. 5 shows good agreement with simulation. The S_{11} at 2.1 GHz is -8.5 dB and can be improved with the addition of a 1.5-2.5 nH bondwire inductor. In simulation this bondwire has only a minor impact on NF and IIP_3 .

The measured noise figure of the LNA remains less than 2.6 dB for frequencies below 2.1 GHz. Effective noise cancellation is verified in Fig. 6 by turning off one of the common source transistors. The IIP_3 of the LNA is measured with a WCDMA compliant blocker test. Two sinusoidal tones located at 1.76/1.95 GHz model the strong AM blocker and on-chip transmitter leakage. They result in an IM_3 product at 2.14 GHz, which falls in the receiver band. The same two-tone spacing is adopted for IIP_3 test at 900 MHz band in order to compare IM_3 cancellation over the frequency. The measured result in Fig. 7 shows very close IM_3 behavior in both bands which confirms the cancellation scheme is indeed effective over wide range of frequency. Both tests achieve a record wideband IIP_3 of +16 dBm. The IM_3 cancellation scheme holds for blocker power as large as -20 dBm, which relaxes the stringent isolation requirement imposed on the duplexer ahead of the LNA. The measured LNA P_{1dB} is -12dBm, as P_{1dB} does not benefit as much as in IIP_3 since higher order terms, e.g. IM_5 , IM_7 , are not canceled by this scheme and

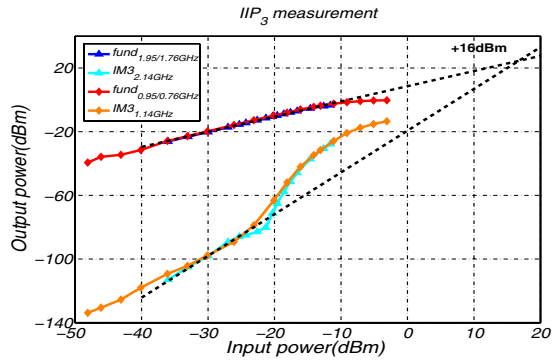


Fig. 7. IIP_3 measurement

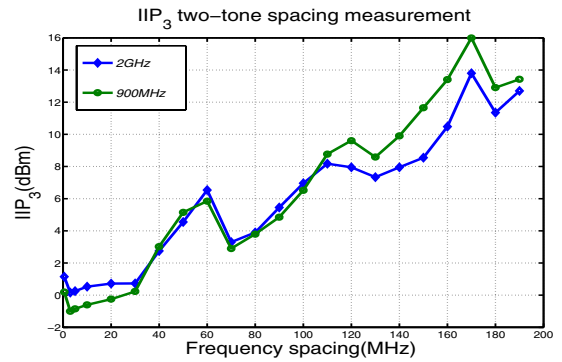


Fig. 9. IIP_3 two-tone spacing measurement

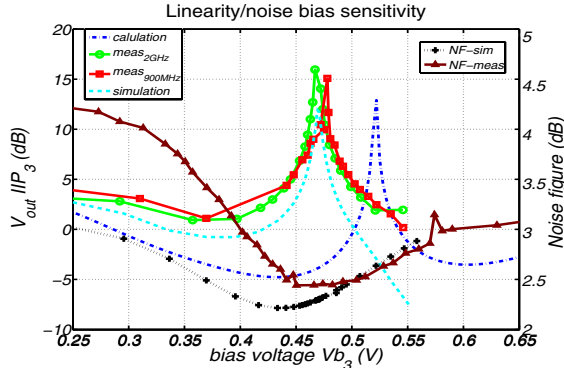


Fig. 8. IIP_3 and NF sensitivity measurement

play a role at higher power levels.

It is important to examine the sensitivity of the distortion/noise cancellation schemes. One way to emulate the effects of matching and threshold variation is to vary the bias point Vb_3 . Fig. 8 compares the measured IIP_3 sensitivity versus post-layout simulation and hand calculation. Good agreement is observed in both the noise and distortion. Discrepancy on the peak IIP_3 location in hand calculation is attributed to difficulties of extracting accurate high order i_d derivatives. As Vb_3 biases transistor M_3 into deep subthreshold region, the corresponding LNA NF moves toward the lower half in the contour in Fig. 2, making the measured NF more susceptible to parameter variations as well as modeling accuracy. As shown in Fig. 8, a 50 mV bias window for Vb_3 is sufficient to maintain IIP_3 greater than +5 dBm and NF below 2.5 dB. On the other hand, this LNA topology shows strong dependency on two-tone spacing when IM_3 test is conducted. This is because the MIM capacitors block low frequency IM_2 components which take part in the cancellation mechanism. Shown in Fig. 9, the benefit of cancellation decreases as two-tone spacing narrows. Since in most wideband systems it is out-of-band blockers that set the most stringent IM_3 requirement, the proposed LNA topology remains promising as a wideband low noise and highly linear solution. The LNA draws 11.6 mA from 1.5 V supply in high linearity low noise mode. The simple topology of this LNA makes it flexible for dynamically scaling the power consumption by turning off some of the unit transistors in the common source stage.

VI. CONCLUSION

A wideband very low IM_3 distortion LNA exploiting noise and distortion cancellation is presented. Volterra analysis indicates 2^{nd} -order interaction constitutes a substantial source of non-linearity after applying distortion cancellation in the LNA. An inverter-type PMOS/NMOS pair is utilized in the common-gate input stage to mitigate this source of distortion. Measured IIP_3 agrees well with simulation and hand calculation. This LNA achieves constant peak IIP_3 of +16 dBm over a wide bandwidth from 800-2100 MHz, while achieving a noise figure below 2.6 dB. A prototype fabricated in a $0.13\mu\text{m}$ CMOS technology without utilizing high- V_{dd} or thick-oxide transistors confirms the amplifier linearity and noise cancellation.

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