

# A 60 GHz Power Amplifier in 90nm CMOS Technology

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**Abstract**—A two-stage 60 GHz 90nm CMOS PA has been designed and fabricated. The amplifier has a measured power gain of 9.8 dB. The input is gain matched while the output is matched to maximize the output power. The measured  $P_{-1dB} = 6.7$  dBm with a corresponding power added efficiency of 20%. This amplifier can be used as a pre-driver or as the main PA for short range wireless communication. The output power can be boosted with on-chip or spatial power combining.

## I. INTRODUCTION

The utilization of the 60 GHz band for wireless communication has received a lot of attention in recent years, with many demonstrations of many CMOS building blocks [1] [2] [3] [4] [5] and even complete front-end receivers [6] [7]. The low supply voltage, thin gate oxide breakdown voltage, and lossy Si substrate of CMOS technology has led many to conclude that CMOS is inappropriate as a power amplifier. Many of these same arguments were also made in the lower GHz spectrum from 1-5 GHz and yet many CMOS power amplifiers have been demonstrated with relatively high efficiency and high levels of integration [8] [9] [10]. Many of the same techniques to realize high power levels in the low GHz regime do not apply to high frequencies since large CMOS transistors have high parasitics which reduce the power gain at mm-wave frequencies. In this work we demonstrate a medium power amplifier that is appropriate as a pre-driver for a PA or as a PA for short range wireless communication links.

We will show in the next section that there is a practical limit to how large we can make a CMOS transistor before the returns on the power gain of the device diminish. Given a fixed supply voltage of 1V in CMOS technology and a fixed device size, and hence fixed device current, the output power of the transistor is limited by  $P_o < V_{DD} \times I_Q$ . To deliver higher power levels therefore requires power combining, as shown in Fig. 1. On-chip power combiners incur additional loss which lowers the efficiency. For instance, a “corporate” 2-way power combiner using Wilkinson couplers introduces about  $\mathcal{L} \sim 1$  dB of loss when implemented onto the Si substrate. Given two amplifier with 5 mW of output power at 20% efficiency means that we can go to about 8 mW and 16% ( $\mathcal{L} \cdot \eta$ ) with a 2-way combiner or about 12.8 mW and 10% efficiency ( $\mathcal{L}^2 \cdot \eta$ ) in a 4-way combiner. Alternatively, we can utilize a multiple antenna transmitter where each amplifier drives a different antenna. The radiated fields of the amplifiers are combined in space with nearly 100% efficiency. Given the small wavelength of

5 mm at 60 GHz, a multi-antenna transmitter is a practical alternative for the realization of the transmitter [11].

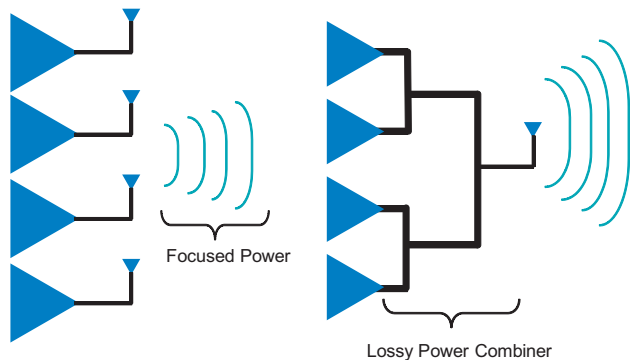


Fig. 1. Conventional on-chip lossy power combining versus spatial power combining.

## II. MM-WAVE POWER DEVICE

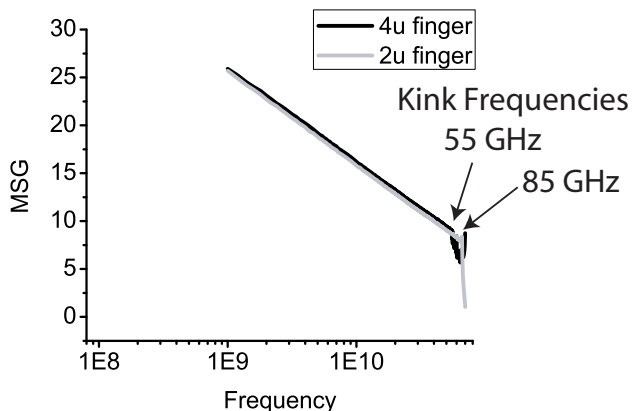


Fig. 2. A comparison of device power gain as a function of device layout (2  $\mu$  versus 4  $\mu$  finger width.)

The design of a power amplifier hinges around the selection of the appropriate power device. In this research we restricted the design to the standard digital transistors available in a 90nm CMOS technology process. While I/O or thick oxide devices are also available, their lower frequency performance limits their applicability at mm-wave frequencies. At this



Fig. 3. Load impedance contours of power gain for the  $2\ \mu$  (left) and  $4\ \mu$  (right) device.

technology node the unity gain current frequency  $f_T$  for the thin oxide NMOS is 100 GHz, and operation at 60 GHz is already close to the limits of activity.

One of the main degrees of freedom in the transistor layout is the selection of the number of fingers for a device of fixed width. Having more fingers helps to reduce the parasitic part of the gate resistance by providing parallel paths to the input signal. Reducing the gate resistance helps to increase the device maximum gain frequency  $f_{max}$ . So, it might appear that we should increase the number of fingers to the limits that process rules permit or until line edge roughness results in large variations in gate resistance. However, there are other issues to consider in making the decision about finger length. The primary considerations for the design of a power amplifier include sufficient power gain  $G_p$ , stability, output power  $P_o$ , and drain efficiency. A large number of fingers results in a very small gate resistance, smaller than that required to stabilize the device in the mm-wave band. For a conditionally stable device, the calculation of the maximum stable gain assumes that fictitious loss is added to the gate to stabilize the device, and therefore increasing the number of fingers does not help. This is true as long as the device is operated below the unconditional stability frequency. This frequency is associated with the kink of the maximum available power gain of the device and is a function of the total gate resistance. Fig. 2 shows a comparison of the maximum stable power gain for a  $2\ \mu$  versus  $4\ \mu$  finger width transistors. The maximum gain at frequencies before the kink where both devices are conditionally stable are similar and independent of the number of fingers. However the kink happens earlier for the  $4\ \mu$  finger width device and the available gain of the  $2\ \mu$  finger device is larger beyond this frequency. As an example, a power device for a 77 GHz PA prefers the smaller finger width device while this does not play a role in terms of gain at 50 GHz.

Increasing the number of fingers could even have some disadvantages. Fig. 5 shows the die photo of a 400 finger  $400\ \mu\text{m}$  width device. As clear in the figure, the aspect ratio of the devices (lengths/ width of the device layout) is very large when utilizing many fingers. Large tapers are usually employed in these devices to ensure a uniform current distribution among fingers. These tapers introduce large series inductance and shunt capacitance on the input and output of the device. Moreover these reactances are lossy due to the conductivity of the substrate and metal layers. The measured

MSG of this device is less than 5 dB, less than half of the optimal device width.

Despite the lower gain, the  $400\ \mu$  device should in theory be able to deliver twice the power of the  $200\ \mu$  device. The  $200\ \mu$  device is biased with 47 mA whereas the  $400\ \mu$  device is biased at 94 mA. However, the variation in gain is much more rapid for the larger device as we move away from the optimal point for the larger device, which means that process variations would lead to more variation of power gain (Fig. 3).

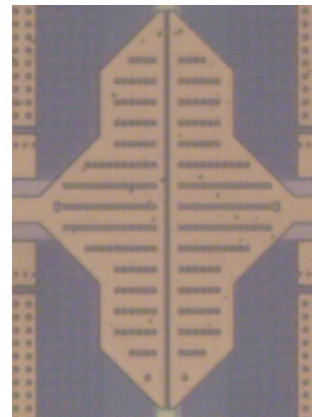


Fig. 5. A  $W = 400\ \mu$  device realized with 400 fingers.)

Given an accurate large signal model of the transistor, or extensive measurements, one can trade-off output power and power gain by plotting contours of constant power gain and constant efficiency on the Smith Chart and select a load impedance, as shown in Fig. 4. As expected both contours fall mostly in the inductive region where the capacitive parasitics of the transistor are tuned out. These plots in addition to the load stability plot can be used to select the optimum load impedance. Given the difficulty of doing extensive load-pull measurements at mm-wave frequencies, we used large signal BSIM models derived from DC I-V curve measurements and AC S-Parameter measurements. Previous experience indicated that this approach is reasonably accurate and simple when large signal power measurements were compared between measurements and simulations [12].

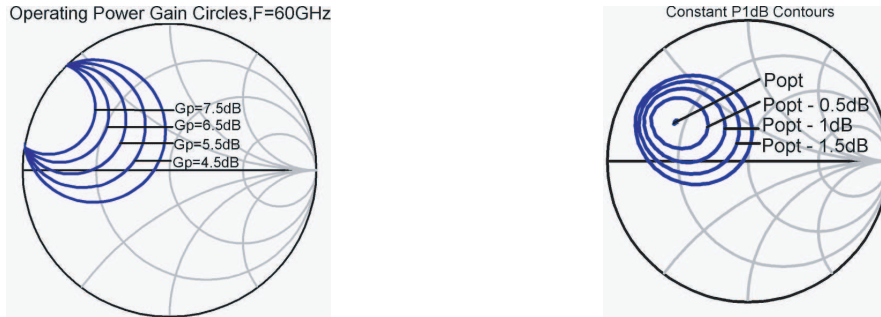


Fig. 4. Load impedance contours of constant device power gain and contours of constant output power.

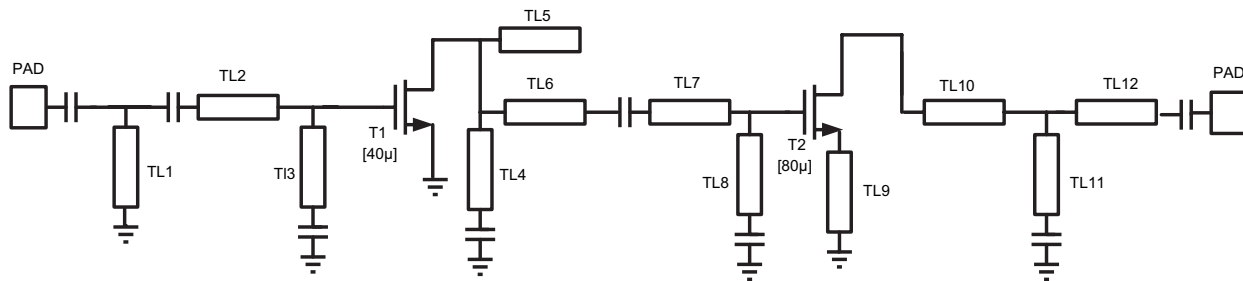


Fig. 6. Schematic of two-stage power amplifier.

### III. AMPLIFIER DESIGN

A two-stage amplifier was designed using “round table” layout transistors [4]. This structure shows an improved available gain compared to the regular multi-finger structure and is desirable for the first stage which is optimized for gain. The output device is  $80\mu$  and the input stage is  $40\mu$ . The width scaling of the second stage is to ensure that the output transistor enters compression first when the first stage has at least 3 dB of gain. The output stage is biased with 14 mA of current whereas the driver stage is biased with 7 mA of current. All matching networks have been realized using coplanar waveguide transmission lines with characteristic impedance of  $51\Omega$  and length varying between  $\lambda/20$  to  $\lambda/6$ . Bypass and coupling caps are custom designed finger capacitors and together with input and output pads have been modeled and incorporated as part of the matching networks. The shorted transmission line at the input, T1, helps to ensure the stability of the circuit at lower frequencies. The output transistor is also degenerated through a small transmission line to add a degree of freedom in the stability-power gain trade-off. To realize a higher power, in this design the output matching network converts the load to a lower impedance of  $15\Omega$  using a transmission line matching network. Note that the output cannot drive the  $50\Omega$  load directly since this would result in very poor gain. A compromise is made between gain and output power when selecting the optimum load impedance. An interstage matching network is also utilized between the driver stage and the output stage. A two-stage low Q matching network is utilized so that the frequency response is determined mainly by the output network. Finally an input

matching network is incorporated for a power match. The most important matching network is the output since this determines the output power capability. The input and interstage matching network should be broadband in order to make the design more robust. Extensive bypass capacitors are employed to decouple the bias and supply. The gate bias networks are de-Q’ed in order to suppress potential instability at lower frequencies.

### IV. EXPERIMENTAL RESULTS

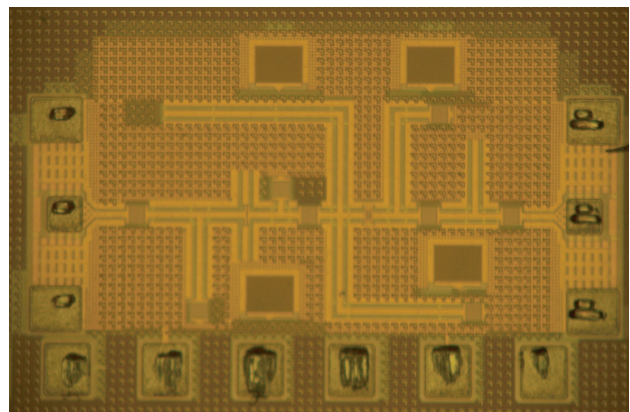


Fig. 7. Die photo of power amplifier.

The prototype PA was fabricated in a digital CMOS process. The chip die photo is shown in Fig. 7. Co-planar transmission lines, finger “comb” capacitors, and poly resistors are employed in the layout of the structure. The input and output

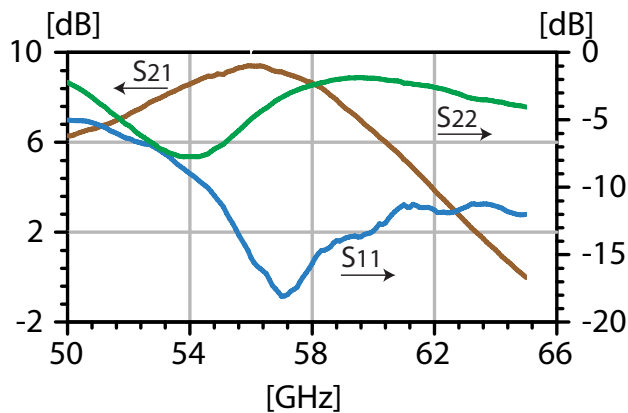


Fig. 8. Measured  $S$  Parameters of power amplifier.

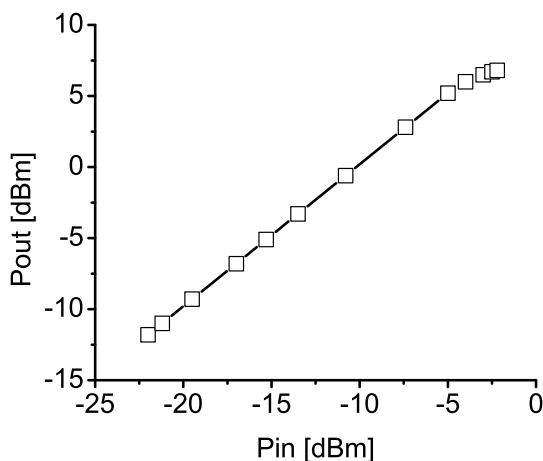


Fig. 9. Measured output power versus input power.

pads parasitics are also absorbed into the design and measured results include pad losses. The measured  $S$ -parameters are shown in Fig. 8. The input is matched at 57 GHz, slightly below the targeted frequency. The gain also peaks at 9.8 dB at 56 GHz and the gain is larger than 8 dB over a 6 GHz bandwidth. The output is matched for power (not gain), as evident in the figure. In simulations, the overall design is unconditionally stable, but the stability is marginal at 40 GHz in this particular design. In the actual measurements, potential instability is observed around this frequency but this did not cause any oscillations. The mismatch between measurement and simulations might be a result of the inaccuracy of the degenerated source of the second stage in addition to process variations which affects the value for input capacitances of the devices.

The amplifier power measurements are shown in Fig. 9. The input power is varied and the output power is measured using an Anritsu ML2437 power meter using the SC6230 65 GHz

power sensor. The linear behavior between input/output power indicates stability. In the measurement setup the output was not directly observable around 40 GHz but the power sensor was used to verify that the circuit is stable, despite the potential instability observed in the small-signal measurements. The output power has a  $P_{-1dB} = 6.7$  dBm, which corresponds to a PAE of nearly 20%. To date, few mm-Wave CMOS PAs have been reported; the only other previously reported CMOS 60 GHz PA demonstrated 7% power added efficiency with nearly similar  $P_{-1dB}$  [3].

## V. CONCLUSION

A fully integrated 90nm CMOS PA capable of delivering 6.7 dBm of linear power in the 60 GHz band has been demonstrated. The PA has a measured efficiency of 20% and is appropriate as a pre-driver or for short range mm-wave transmitter applications.

## VI. ACKNOWLEDGEMENT

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## REFERENCES

- [1] C. H. Doan, S. Emami, A. M. Niknejad, and R. W. Brodersen, "Design of CMOS for 60GHz applications," *ISSCC Digest of Technical Papers*, 2004, pp. 440-538.
- [2] C. H. Doan, S. Emami, A. M. Niknejad, and R. W. Brodersen, "A 60-GHz down-converting CMOS single-gate mixer," *RFIC Digest of Tech. Papers*, 2005, pp.163-166.
- [3] T. Yao, M. Gordon, K. Yau, M.T. Yang, S. Voinigescu, "60-GHz PA and LNA in 90-nm RF-CMOS," *RFIC Digest of Papers*, 2006.
- [4] B. Heydari, M. Bohsali, E. Adabi, A.M. Niknejad, "Low-Power mm-Wave Components up to 104GHz in 90nm CMOS," *ISSCC Digest of Technical Papers*, 2007, pp. 200-201, 597.
- [5] C.-M. Lo, C.-S. Lin, H. Wang, "A Miniature V-band 3-Stage Cascode LNA in 0.13m CMOS," *ISSCC Dig. Tech. Papers*, pp. 322-323, Feb. 2006.
- [6] B. Razavi, "A mm-Wave CMOS Heterodyne Receiver with On-Chip LO and Divider," *ISSCC Dig. Tech. Papers*, 2007, pp. 188-189.
- [7] C.H. Doan, S. Emami, A.M. Niknejad, R.W. Brodersen, "A 60GHz CMOS Front-End Receiver," *ISSCC Digest of Tech. Papers*, 2007, pp. 190-191.
- [8] K.-C. Tsai, P. R. Gray, "A 1.9-GHz, 1-W CMOS class-E power amplifier for wireless communications," *IEEE Journal of Solid-State Circuits*, vol. 34, July 1999, pp. 962-970.
- [9] I. Aoki, S.D. Kee, D. Rutledge, A. Hajimiri, "A 2.4-GHz, 2.2-W, 2-V fully-integrated CMOS circular-geometry active-transformer power amplifier," *Proceedings of CICC*, 2001, pp. 57-60.
- [10] G. Liu, T.-J. King, A. M. Niknejad, "A 1.2V, 2.4GHz Fully Integrated Linear CMOS Power Amplifier with Efficiency Enhancement," *Proceedings of CICC*, 2006, pp. 141-144.
- [11] A. M. Niknejad, C. H. Doan, S. Emami, D. Sobel, R. W. Brodersen, "60 GHz CMOS radio for Gb/s wireless LAN," *RFIC Digest of Papers*, 2004, pp. 225-228.
- [12] S. Emami, C. H. Doan, A. M. Niknejad, R. W. Brodersen, "Large-signal millimeter-wave CMOS modeling with BSIM3," *RFIC Digest of Papers*, 2004, pp. 163-166.