

# Low-Power Successive Approximation Converter With 0.5 V Supply in 90 nm CMOS

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**Abstract**—We report on the design and characterization of an ultralow-power converter, designed for use in baseband digitization in wireless sensor network radio receivers. The converter uses a successive approximation architecture and operates robustly with a supply voltage as low as 450 mV, overcoming charge leakage limitations. Implemented in a 90 nm CMOS process, this design achieves a figure of merit of 0.14 pJ/Conv.Step for the converter core and shows the integration of a complete data-conversion subsystem, including reference generation, from a 0.5 V supply.

**Index Terms**—Analog-to-digital conversion, charge leakage, CMOS, digital calibration, low power, low voltage, subthreshold, successive approximation.

## I. INTRODUCTION

THE massive deployment of wireless sensor networks requires complete radio receivers with power dissipation of a few hundred microwatts to be designed.

As an integral part of the radio receiver, a moderate resolution analog-to-digital (A/D) ( $\sim 6$  b) converter with power dissipation of a few microwatts and sample rate in excess of 500 KS/s is required [1]. The converter should also operate from a power supply as low as possible to facilitate its integration with low-power digital circuitry. In this paper, we present an analog-to-digital converter (ADC) that satisfies these requirements. It employs a successive approximation architecture, to minimize analog complexity and avoid the use of operational amplifiers, and sign-magnitude bit coding, combined with a three-level unit element digital-to-analog converter (DAC), to minimize input capacitance. An integrated mixed-signal calibration routine exploits the existing converter logic to perform digital offset cancellation by adjusting the capacitive load of the clocked comparator. The converter core achieves 5.15 ENOB at Nyquist input while sampling at 1.5 MS/s and dissipates 7  $\mu$ W total from a 0.5 V supply. A low-voltage reference generator, also operating from 0.5 V, is integrated with the converter and provides full-scale voltage variables between 65 and 260 mV, embedding an additional 12 dB of programmable gain to the system.

This paper is organized as follows. In Section II, the main factors determining the minimum operating voltage of successive approximation converters are reviewed. Section III describes the design of an integrated converter system at the architecture level, while the circuit details are reported in Section IV. The measured performance of the prototype is described in Section V, and conclusions are drawn in Section VI.

## II. ANALOG VOLTAGE SCALING

With the exception of [2], most studies on the effects of voltage scaling on the analog performance and power dissipation are restricted to a noise-limited scenario, where power efficiency is degraded by scaling. If a design is limited by capacitive mismatch, however,  $V_{\text{err}} = V_{\text{dd}}\Delta C/C$ , so that the capacitor sizes are independent of the supply voltage  $V_{\text{dd}}$ . Under these circumstances, power dissipation is reduced by decreasing the circuit operating supply. While the lower limit on the operating supply is set by thermal noise, for 6 bits of resolution and realistic capacitance values, this limit is of the order of 100 mV and cannot be achieved in practice. Power efficiency is instead degraded when the reduced headroom forces the designer to employ complex, power-inefficient circuit topologies. Architectures that rely on high-gain amplifiers, such as pipelined ADCs, are the first to fail. Conversely, a successive-approximation-register (SAR) converter presents almost ideal behavior with respect to voltage scaling. When using switched-capacitor techniques, the only analog blocks present are the sampling switches, the clocked comparator, and a charge/redistribution-based DAC. Since the latter is composed only of capacitors and switches connected to the fixed reference voltages, it can be operated from a very low-supply voltage. Similarly, the comparator does not have a stringent offset specification, and, hence, for moderate speeds, supplies almost as low as the metastable point of a CMOS latch, of the order of 100 mV, can be used.

The limiting factor to supply voltage scaling is finally introduced by the sampling network. First, to keep the on-resistance (and hence sampling linearity) constant at reduced  $V_{\text{dd}}$ , wider transistors have to be used, resulting in increased capacitive drive for the clock network. Due to the exponential dependence of channel resistance on  $V_{\text{dd}}$  in subthreshold, for the component values used in this design, reducing  $V_{\text{dd}}$  below 500 mV [6] results in drastic increase in clock power. Second, widening sampling switches decreases their off-resistance. As proved in the Appendix for B-bits of linearity, a worst case analysis requires from the sampling switches an  $R_{\text{off}}/R_{\text{on}}$  ratio better than

$$\frac{R_{\text{off}}}{R_{\text{on}}} > 2^B B^2 \log(2). \quad (1)$$

Overlaying the value predicted by (1) with the simulated  $R_{\text{off}}/R_{\text{on}}$  value of a commercial 90 nm CMOS process as done in Fig. 1 shows the performance limitations imposed by charge leakage: when the supply is lowered to 0.5 V, the resolution appears limited to 5 bits or less if specific countermeasures are not taken.

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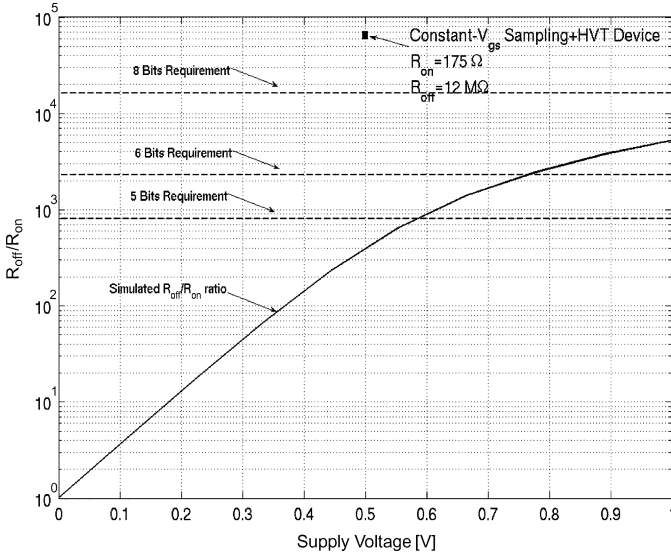


Fig. 1. Noise margin for a 90nm and chosen design point in [1].

Although the analysis leading to (1) makes worst case assumptions and therefore leads to conservative predictions, the high sensitivity of leakage currents to process and temperature variations requires careful design. For instance, over a 0 °C–85 °C temperature range, switches must have a sufficiently low  $R_{on}$  to ensure accurate sampling in the conditions where the process is on the slow corner and temperature is low (as at low supplies, threshold voltage variations dominate on-resistance temperature behavior over mobility variations), while still providing a sufficiently high  $R_{off}$  when the process is on the fast corner and the operating temperature is high. Since in this latter condition the leakage currents are increased by roughly 100 times over the nominal value, while in the former on-resistance is increased by as much as a factor of ten, a large margin is needed to meet (1).

### III. ARCHITECTURE DESIGN

The overall architecture of this integrated converter system is shown in Fig. 2. It is an improved version of the work presented in [1]. Only the differential input signal and a 16 MHz bit cycling clock need to be generated off-chip, while the full-scale reference as well as other control signals and biasing are generated on-chip and controlled by a three-wire SPI interface.

#### A. Conversion Algorithm

The converter performs quantization by operating on a sign-modulo number representation and performs sampling on the top plates of the capacitor array. Operating in sign-magnitude format enables the use of a tri-level unit element DAC, which, as will be explained below, provides good linearity and low input capacitance to the circuit. Furthermore, when operating in a sign-magnitude representation, sampling on the top plates enables the use of the sampling phase as the first phase of the conversion, leading to a faster algorithm or to a reduced clock frequency.

Therefore, the signal is sampled on the top plate of the capacitor array, and, at the end of the sampling phase, the comparator

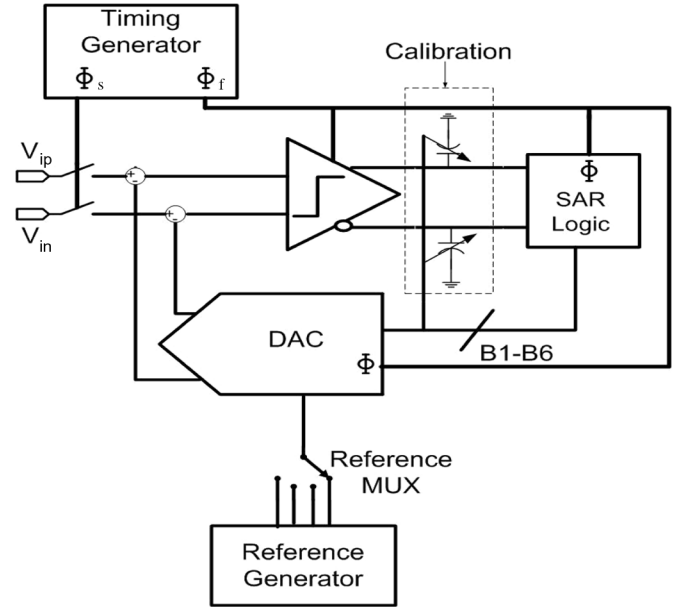


Fig. 2. Block diagram of a complete successive approximation conversion system.

decides on the sign of the current sample. In successive clock phases, depending on the first decision, the voltage on the positive side of the capacitor array is either incremented or decremented with respect to the voltage on the negative side, effectively performing the conversion of the absolute value of the input. Assuming, for instance, that the input sample was positive and the sign bit was resolved correctly to 1, the first guess in the absolute value search will be 10 000 and the overall output code will be 110 000. Therefore, the bottom plate of the MSB capacitor connected to the positive side is connected to  $V_{r1}$ , while the bottom plate of the negative-side MSB capacitor is connected to  $V_{rh}$ . All of the other capacitors have bottom plates tied to  $V_{cmRef}$ . The differential voltage on the comparator input nodes decreases by  $V_{ref}/2$  ( $V_{ref} = V_{rh} - V_{r1}$ ) and is thresholded by the comparator. Based on this decision, the second guess is calculated and the conversion process continues.

This algorithm maintains the properties of a conventional binary search and, in particular comparator offset, as long as it is lower than  $V_{ref}/2$  in absolute value, only results in overall converter offset and does not degrade linearity.

#### B. Embedded Variable Gain

Performance of the converter in [1] was limited by quantization noise rather than by thermal noise. In this design, we take advantage of the quantization-noise-limited nature of the core by making the reference generator output programmable between 65 and 260 mV through two control bits. The ability to reduce the ADC reference by a factor of up to four for low-input signals acts as an embedded 12 dB programmable gain amplifier, extending the circuit dynamic range. However, reference independent errors such as converter offset voltage are amplified along with the signal, so that special care must be taken in minimizing them. This leads to the introduction of the offset cancellation routine described in Section IV.

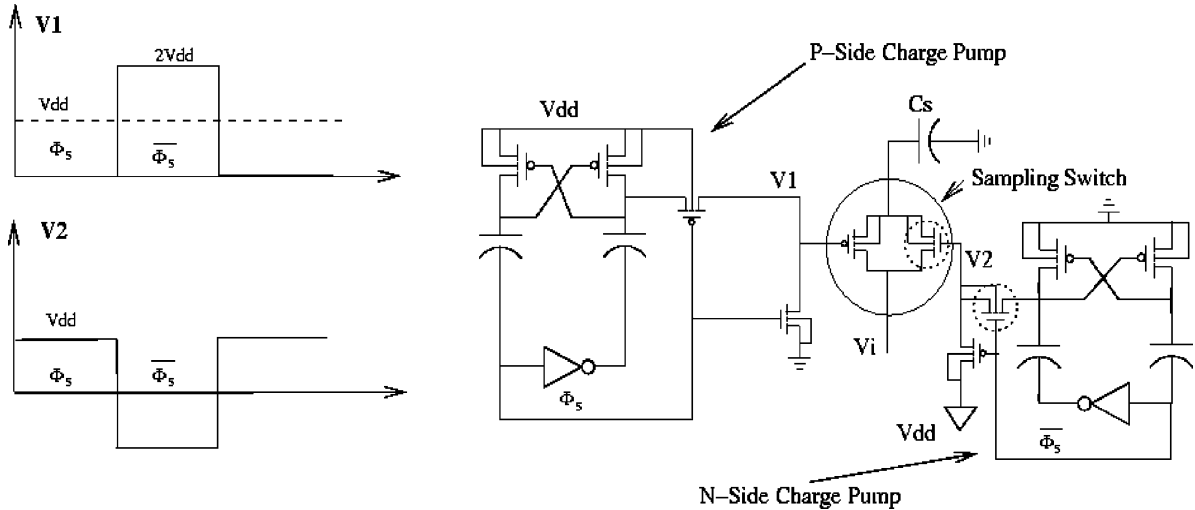


Fig. 3. Complementary sampling with boosted turn-off.

#### IV. CIRCUIT DESIGN

##### A. Sampling Network Design

As mentioned above, this design uses top-plate sampling. This raises concerns about nonlinearity of the parasitic capacitance on the top plates. Due to the small size of the active devices used, the parasitic capacitance on the top plate of the array is dominated by routing and is hence quite linear, so that no significant signal-dependent error is introduced at the 6 bits level. Sampling on the bottom plate could still improve the robustness of the converter with respect to charge leakage, as in this case the critical switch only connects the common-mode reference to initialize the top plates, resulting in a relaxed on-resistance requirement. However, this benefit is modest because the voltage to be switched is still around midrail and the required converter accuracy is small. Even when using bottom plate sampling, a boosted turn-off switch might have to be used for common-mode initialization, leading to no significant reduction in circuit complexity.

Avoiding the use of HVT devices poses challenges in the sampling network design, as a constant- $V_{gs}$  sampling scheme fails to provide adequate off-resistance during the bit-cycling phase [1]. T-switches cannot be employed due to the dynamic nature of the floating node and, hence, a complementary switch with boosted turn-off, where the pMOS and nMOS devices are turned off hard, is employed (see Fig. 3) to achieve linear sampling and good isolation [4]. Because the  $V_{dd}$  is only 0.5 V, the  $V_{gs}$  of the boosted devices is always lower than 1 V, so that no reliability concern is raised. Still, this circuit requires an nMOS pass transistor to tolerate a  $-V_{dd}$  source voltage (see the device with a dotted circle in Fig. 3), and it can only be employed in those technologies which allow nMOS devices to be fabricated in a separate well and isolated from the substrate, which is the case for the given 90 nm process.

##### B. Digital-to-Analog Converter

The core DAC is a capacitor array that was designed to obtain a moderate linearity of 6 bits while simultaneously minimizing the total capacitance to avoid excessively loading any preceding

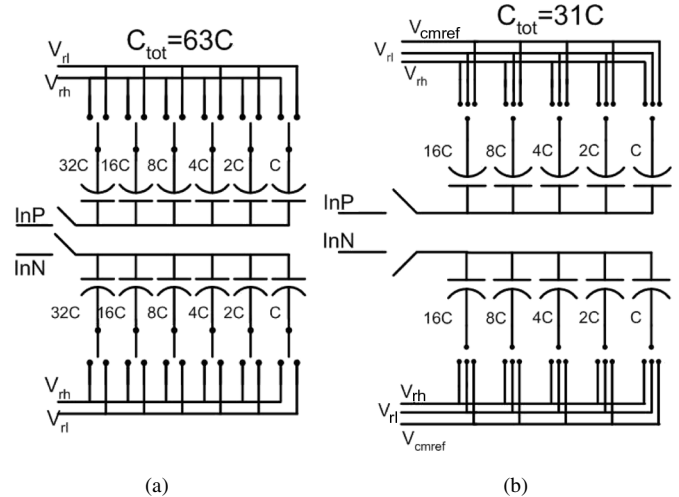


Fig. 4. Binary-weighted 6 bit DAC employing (a) conventional technique and (b) 1.5 b/element technique.

variable gain/filtering stage and increasing power consumption. To reduce capacitance, a binary-weighted 1.5 b/element design is used. In this design, the bottom of each capacitor can be tied to the positive reference  $V_{rh}$ , the negative reference  $V_{rl}$ , or the common-mode reference  $V_{cmref} = V_{dd}/2$ , so that each capacitor pair can encode +1, -1, and 0 (see Fig. 4). This technique solely relies on the top plate of the array being floating and on the use of sign-magnitude coding, and it could hence be used in conjunction with bottom-plate sampling as well.

The total capacitance of a binary-weighted 6 bit DAC employing this technique is  $31C_u$ , as opposed to  $63C_u$  of a conventional implementation. Furthermore, the gain from unit capacitance mismatch to peak INL standard deviation is also halved [1]. As a result, this technique enables the reduction of total capacitance of a matching-limited design by a factor of four.

The linearity of the converter depends now also on  $V_{cmref}$  being located exactly halfway between  $V_{rh}$  and  $V_{rl}$ . It is shown in [6] that this effect does not introduce any performance limitation for 6 bits of resolution, so it will be ignored in the following.



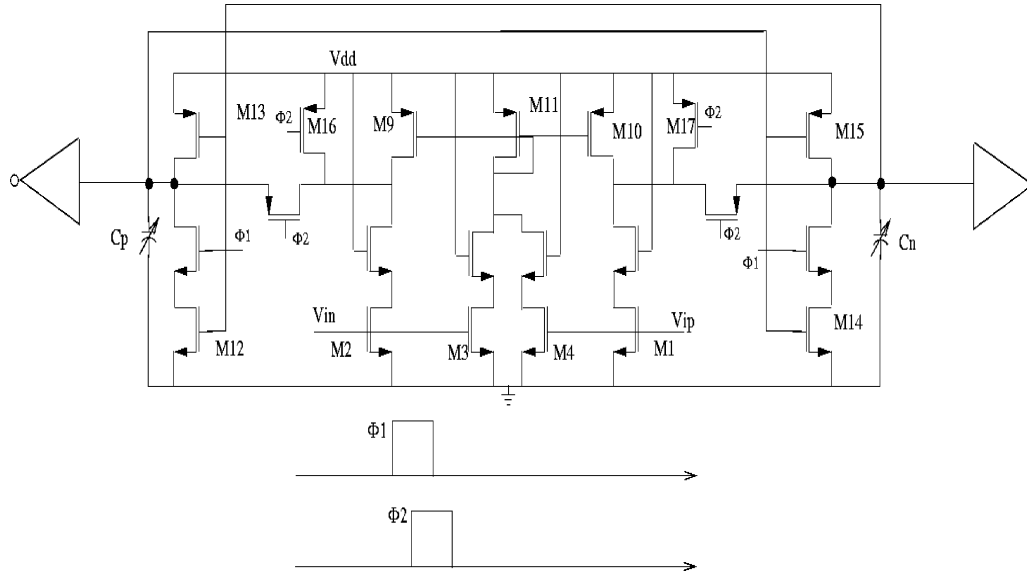


Fig. 6. Comparator schematic and timing diagram.

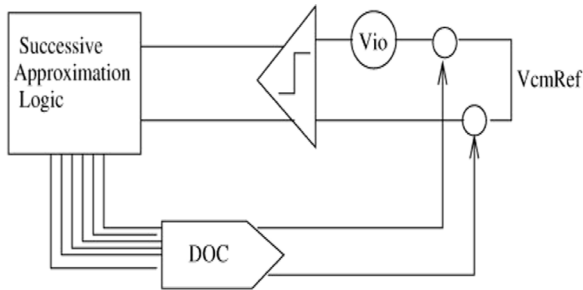


Fig. 7. Digital-offset calibration concept.

### F. Offset Cancellation

To maximize the effectiveness of the reference scaling technique, we use a mixed-signal offset cancellation scheme, where the comparator input referred offset is measured during a calibration phase and compensated by a digital-to-offset converter (DOC) (see Fig. 7) during normal operation. During the measurement phase, the same DOC together with the successive approximation logic and the clocked comparator are used to build a successive approximation offset-to-digital converter (ODC) by disconnecting the inputs of the clocked comparator from the main signal path and letting the DOC act as a DAC in a normal successive approximation routine. Because the comparator and digital logic are already required by the normal converter operation, the calibration requires very little overhead and is hence amenable to low-power design.

The DOC is realized by connecting two digitally controlled capacitor arrays to the regeneration nodes of the clocked comparator ( $C_p$  and  $C_n$  in Fig. 6). As proved in [6] and [10], a relative capacitive imbalance  $\Delta C/C$  on these nodes is translated into an input referred offset  $V_{io}$  given by

$$V_{io} = \frac{2(V_{cm} - V^*)}{A_v} \cdot \frac{\kappa - 1}{\kappa + 1}$$

$$\kappa = \sqrt{1 + \frac{\Delta C}{C}} \quad (3)$$

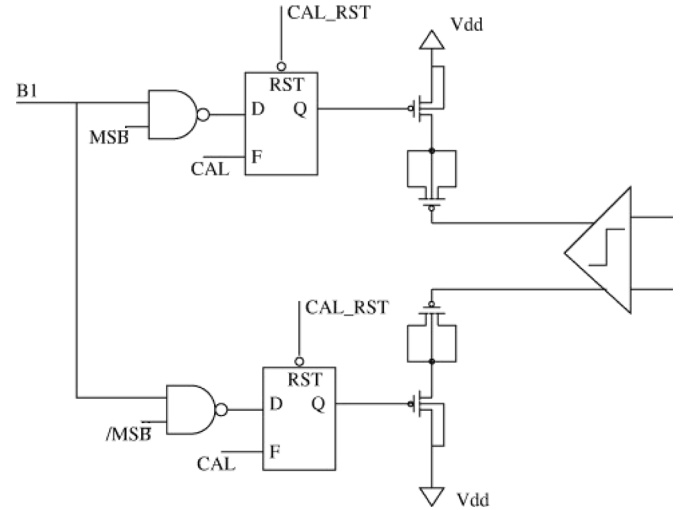


Fig. 8. Simplified schematic of DOC: unit capacitor and control logic.

where  $V_{cm}$  is the common-mode output voltage of the latch during tracking,  $V^*$  is the inverter trip point, and  $A_v$  is the comparator gain during tracking mode. To achieve a calibration full scale of 18 mV and a calibration LSB of 1 mV, a 5-b/side binary-weighted, digitally controlled capacitor array with 0.8 fF unit elements was built using thin-oxide pMOS capacitors. The bulk is tied to the source to maximize the  $C_{on}/C_{off}$  ratio. Fig. 8 shows the circuit schematic for a single calibration capacitor, including control logic and memory latches.

During calibration [8], the inputs of the comparator are tied to  $V_{cmRef}$  by a multiplexer, and the capacitor array is controlled directly by the successive approximation logic, thus performing a successive approximation offset-to-digital conversion. During normal operation, the calibration word is stored in a bank of latches. Calibration is run deterministically (i.e., no averaging is performed) for only one converter cycle (1  $\mu$ S), and the only overhead it requires lies in the aforementioned bank of latches and in the multiplexer.

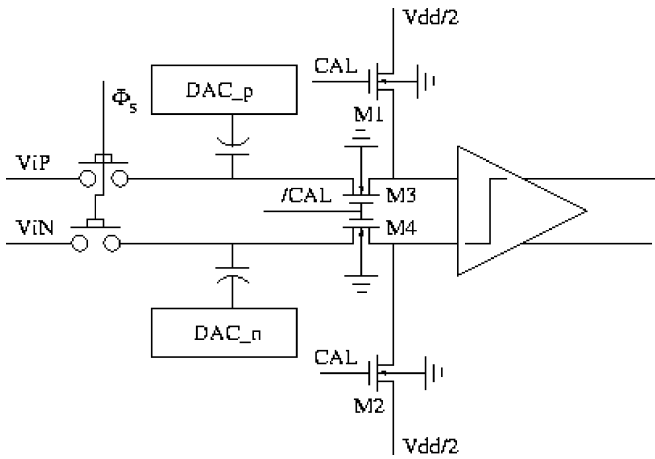


Fig. 9. Placement of calibration mux maximizing sampling linearity.

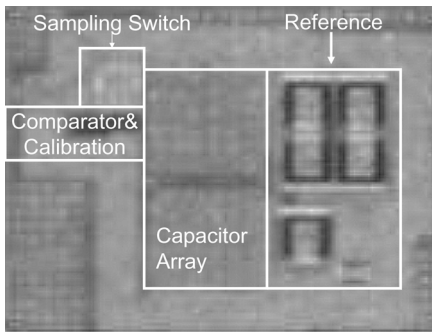


Fig. 10. Die photograph.

The multiplexer is placed in series with the input devices of the comparator, so that its on-resistance does not impact sampling linearity (see Fig. 9). Since to first order the mux only needs to charge the comparator parasitics, much smaller devices can be used than in the sampling switch, thus mitigating charge leakage from this device.

V. MEASURED RESULTS

The prototype converter was fabricated in a 90 nm 7M2P CMOS process from ST Microelectronics (see the die photograph in Fig. 10) and occupies an area of  $350 \mu\text{m} \times 350 \mu\text{m}$ , including reference generator and decap. The converter dies were directly mounted on a custom-designed printed circuit board, avoiding the use of a package, and an on-board high-performance ADI8138 driver was used to convert the single-ended signal source output to differential. A single 0.5 V  $V_{dd}$  connection was used to power analog, digital, and reference circuits during testing.

Fig. 11 displays static linearity, which was obtained through histogram testing. The converter is monotonic and shows a worst case peak INL of about 0.5 LSBs for the maximum full scale. The measured dynamic converter performance is summarized in Figs. 12 and 13. A 32.4 dB Nyquist SNDR (5.07 ENOB) is achieved in the maximum full-scale setting. The SNDR is degraded to 27.5 dB for minimum full scale due to underestimated reference noise. Fig. 14 reports converter dynamic performance versus sampling rate, measured with a 10 kHz input tone. SNDR and SFDR are constant for sampling

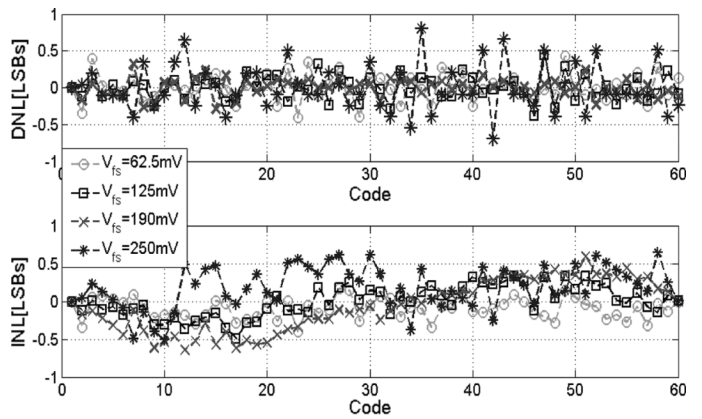


Fig. 11. Measured DNL/INL of the integrated converter system at different full-scale settings.

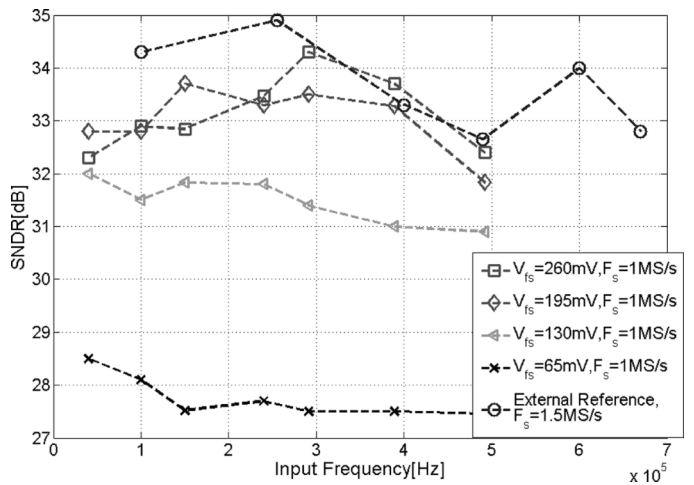


Fig. 12. Measured SNDR of the integrated converter system at different full-scale settings.

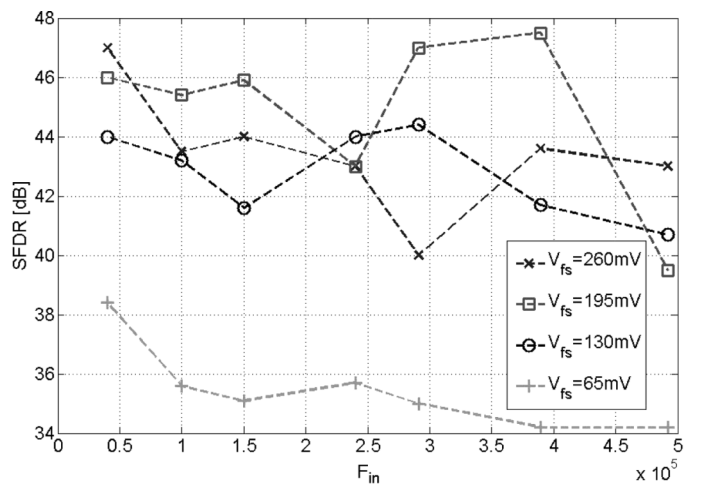


Fig. 13. Measured SFDR under different full-scale settings.

frequencies going from 60 kS/s to 1 MS/s. Above 1 MS/s, performance drops abruptly due to incomplete reference settling. At 31.25 kS/s, a degradation in SNDR and SFDR is observed that can be again attributed to increased charge leakage [1]. The low-frequency SNDR versus operating supply, measured

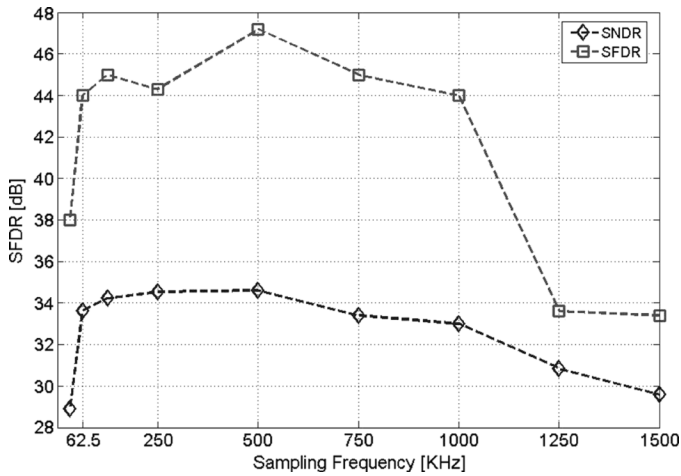


Fig. 14. Low-frequency SNDR and SFDR versus sampling rate.

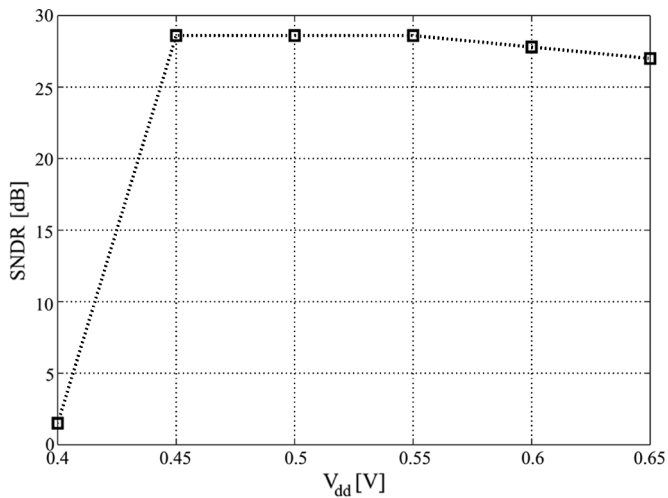


Fig. 15. Low-frequency SNDR versus supply voltage.

at 1 MS/s, is shown in Fig. 15. A minimum operating supply of 0.45 V is supported by the conversion system and limited by the reference generator.

The converter exhibited an input-referred offset larger than the simulated  $3\sigma$  value of 18 mV. As seen in Fig. 16, when the supply is 0.5 V, the offset exceeds the calibration routine full scale and cannot be completely canceled. Increasing the power supply voltage to 0.65 V increases the unit capacitance of the MOS calibration capacitor array and results in a larger calibration full scale. In this case, the offset is successfully reduced below 1 LSB of the minimum full scale, and averaging the ADC output code indicates a residual of approximately 990  $\mu$ V.

The overall power consumption of the converter as a function of sampling frequency is shown in Fig. 17. At 1 MS/s, the core consumes only 6  $\mu$ W, matching simulation to within 10% and demonstrating the effectiveness of the proposed power-reduction techniques. Four  $\mu$ W of power consumption are still contributed from static currents, mostly determined from leakage of digital gates. This fraction could be further reduced

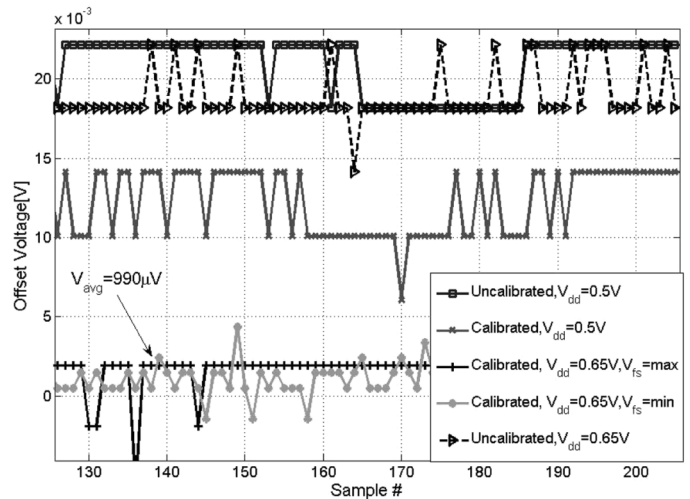


Fig. 16. Residual offset after calibration for a tested sample.

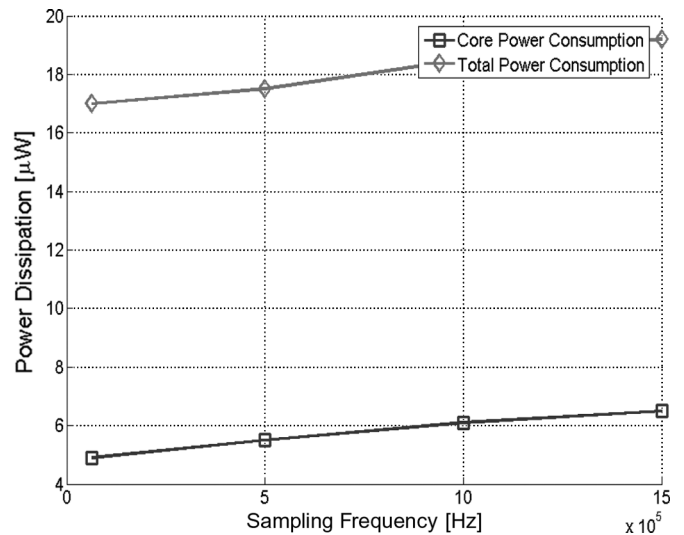


Fig. 17. Power dissipation of the second prototype as a function of sampling frequency.

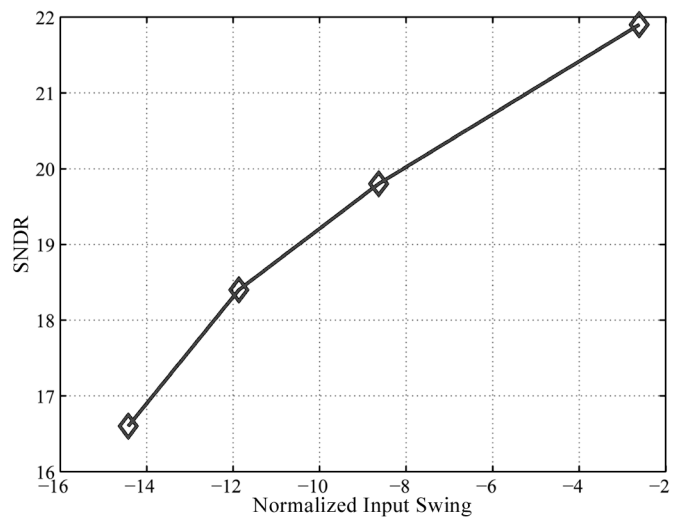


Fig. 18. Performance in reference scaling mode.

TABLE I  
COMPARISON WITH OTHER LOW-VOLTAGE SUCCESSIVE  
APPROXIMATION CONVERTERS

Reference	#Bits	Vdd	Pd ( $\mu$ W)	ENOB @ Nyquist	Fs	FOM (pJ/Conv.)	Tech.
[3]	8	1.4	4.2	7	100 KS/s	.24	0.25 $\mu$ m
[7]	8	.6	1	7	1 KS/s	.35	0.18 $\mu$ m
[8]	8	1	340	<6.5	100 KS/s	26	1 $\mu$ m
[1]	6	0.5	14	5.3	1.5MS/s	.24	90nm
This Work (ADC+VGA)	6	0.5	17	5.07(SND R) /6.07(DR)	1MS/s	.5(SNDR) /.25(DR)	90nm
This Work (External Vref)	6	0.5	7	5.15	1.5MS/s	.14	90nm

at the expense of integration potential by exploiting high- $V_{th}$  devices. The reference generator consumes 11  $\mu$ W independent of sampling speed. Such relatively high power consumption is dictated by the implementation of the variable-full scale feature, which required the use of linear polysilicon resistors in the output branch. Lower power dissipation may be obtained at the price of programmability by employing diode-connected MOS devices as resistors. Finally, the effectiveness of the variable full-scale feature was evaluated by feeding to the input of the converter a sinewave of amplitude equal to the difference between the minimum converter full scale and the post-calibration residual offset. The reference is subsequently scaled from the maximum to the minimum value, giving a 6 dB improvement of SNDR (Fig. 18). The SNDR boost is lower than the theoretical 12 dB due to the residual comparator offset and the increased noise in low full-scale mode.

## VI. CONCLUSION

Thanks to their mostly digital nature, successive approximation converters are bound to experience increased popularity in low-voltage environments. While scaling naturally extends the maximum sampling frequency achievable by this architecture, however, reduced  $R_{off}/R_{on}$  of the sampling switches may limit the performance for sampling frequencies lower than 1 MHz. In this paper and in [1], we have demonstrated design techniques that enable megahertz-rate successive approximation converters to operate from a 0.5 V supply. These moderate resolution converters dissipate less than 20  $\mu$ W and are therefore suited for baseband digitization in a sensor-network environment and for many bio-sensor data acquisition applications. In Table I, the energy efficiency of the designed converters is compared with the results given in recent literature using the well-known figure of merit (FOM) metric ( $FOM = Pd/(2^{ENOB}f_s)$ ), where ENOB is measured at Nyquist input frequency).

The converters presented in [1] and in this paper attain FOM values of the order of 0.2 pJ/Conv.Step, thus comparing favorably to other low-voltage state-of-the-art techniques. Furthermore, they demonstrate for the first time the feasibility of a completely integrated data conversion system operating from a single 0.5 V supply.

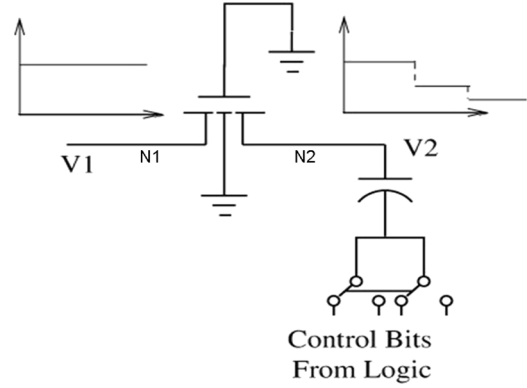


Fig. 19. Sampling circuit during bit-cycling phase.

## APPENDIX

### DERIVATION OF (1)

During the sampling phase, the sampling switch resistance  $R_{on}$  should guarantee B-bit accurate settling within  $1/(Bf_s)$  seconds. Therefore

$$R_{on} \leq \frac{1}{B^2 f_s C_s}. \quad (4)$$

During the bit cycling phase (lasting  $(B-1)/(Bf_s)$  seconds), charge is lost from the floating nodes through the sampling switches obeying the law

$$Q(t) = Q_0 \exp\left(\frac{-t}{\tau_{off}}\right).$$

Evaluating at time  $t = T_s$  and using the Taylor expansion yields

$$Q(T_s) - Q_0 \approx Q_0 \frac{T_s}{\tau_{off}}. \quad (5)$$

Now,  $\tau_{off} = R_{off}C_{off}$  is an exponential function of the gate-source voltage of the switching device and, hence, of the voltage at N1,  $V_{in}$  (see Fig. 19). As N2 swings higher than the input voltage  $V_{in}$ ,  $V_{in}$  acts as the source of the device, and so  $R_{off} = R_0 \exp(-V_{in})$ .

However, if N1 swings below  $V_{in}$ , it becomes the source of the sampling switch, and the off-resistance is  $R_{off} = R_0 \exp(-V1/Vt)$ . The worst case happens when V1 goes to ground, giving the lowest possible  $R_{off}$  value. Assuming node N1 is at ground for the whole bit cycling phase, using (6), and imposing that the total charge lost should be less than 1 LSB, one finally finds

$$\frac{T_s}{\tau_{off}} \leq 2^{-B} \Rightarrow R_{off} \geq \frac{2^B}{C_s f_s}. \quad (6)$$

Combining (4) and (6), (1) is obtained. Notice that the amount of charge lost depends on the dynamics of node N1 during the successive approximation algorithm and will therefore cause distortion in the converter characteristic.

## ACKNOWLEDGMENT

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