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# **A Prototype Broadband CMOS LNA for Universal Radio Receivers**

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## **Research Project**

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## Introduction

### 1.1 Motivation

The last few years have been a revolutionary period for wireless communications. With exponential growth in the area for years, now there are lots of wireless standards for various frequency bands. There have been many attempts to create a transceiver that can operate in different frequencies and standards. The receiver designs for such a transceiver is very critical and poses a lot of challenges such as interferences, noises, power consumptions, and costs. The goal of this work is to investigate the issues in designing a multi-band receiver front-end as well as comparing different receiver architectures in terms of suitability for this application.

As an important building block in the receiver chain, a prototype LNA has been designed and fabricated. The LNA is designed to have a broadband matching in order to fit with universal radio applications. The circuit employs a multi-stage passive matching network and achieves better than -10 dB matching bandwidth from 0.8 GHz to 2.4 GHz. In addition, the dynamic operation characteristic of the LNA is also investigated.

## **1.2 Thesis Organization**

The first part of the report is devoted to the system-level analysis of the universal receiver front-end whereas the second part highlights the design and of a broadband CMOS Low-Noise Amplifier (LNA).

Chapter 2 consists of the reviews of receiver basics and comparisons of different receiver topologies. In chapter 3, the analysis of the universal receiver front-end in terms of specifications, limitation, and suitable topologies will be discussed. In this chapter, the estimated specifications on the building blocks, as well as expected performance of the front-end, will be given.

The second part starts with the reviews of LNA fundamentals and CMOS LNA topologies in chapter 4. Chapter 5 follows with the design of a broadband CMOS LNA. Measurement results and conclusions will be given in chapter 6.

## Receiver Basics

### 2.1 Introduction

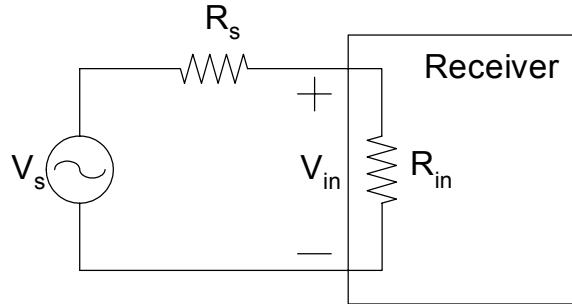
This chapter covers some important concepts about the receiver: selectivity and sensitivity. These two parameters are the most comprehensive figures of merit in the receiver performance and influenced by many sub-figures of merit, such as individual noise performance of the individual building blocks, linearity, gain distribution, and image rejection. The relationships between these sub-figures of merit and selectivity as well as sensitivity will be discussed in section 2.2 and 2.3.

Followed in section 2.4 is the review of some basic receiver architectures characterized by different frequency planning methodologies. This includes super-heterodyne, zero-IF (direct conversion), and low-IF receivers.

### 2.2 Sensitivity

The definition of sensitivity is the minimum detectable signal at the receiver input, such as there is a sufficient signal-to-noise ratio (SNR) at the receiver output for a given application. Sensitivity determines the maximum distance that a receiver can be away from the transmitter or the base station for a mobile phone case. Sensitivity can be

specified in the unit of dBm (decibels relative to one milliwatt) along with the reference impedance ( $50\Omega$  for most systems) and is typically measured in the interference-free environment. Usually, the input of the receiver is matched to a certain source impedance simplified as the real impedance  $R_{in} = R_s$  in figure1.



**Figure 2.1** Impedance matching in receiver

### 2.2.1 Noise Figure Definitions

The overall sensitivity is directly related of the noise figure of the receiver, which is impacted by noise from individual blocks in the receiver as well as gain distribution of the receiver chain. The noise figure is defined as a ratio between the SNR at the input and the SNR at the output of the circuit:

$$F \equiv \frac{\text{Input SNR}}{\text{Output SNR}} \quad (2.1)$$

$$NF \equiv 10 \log(F) \text{ (dB)} \quad (2.2)$$

Where  $F$  is called a noise factor and  $NF$  is the noise figure of the system

Noise figure is usually calculated as referred to specified source impedance and the noise temperature. In standard communication systems, the typical values are  $R_s=50\Omega$  and  $T=293\text{ K}$ . For a circuit building block such as an amplifier in figure 2.2, the total noise figure can be derived in terms of added output noise and the gain of the system. The amplifier with power gain  $G$  with the input signal power  $P_{in}$  and input noise power  $N_{in}$  will have the output signal power  $GP_{in}$  and output noise power  $GN_{in}+N_{add}$ . The noise figure of the amplifier can then be calculated using the definitions in (2.1).

$$F = \frac{\left(\frac{P_{in}}{N_{in}}\right)}{\frac{GP_{in}}{GN_{in} + N_{add}}} \quad (2.3)$$

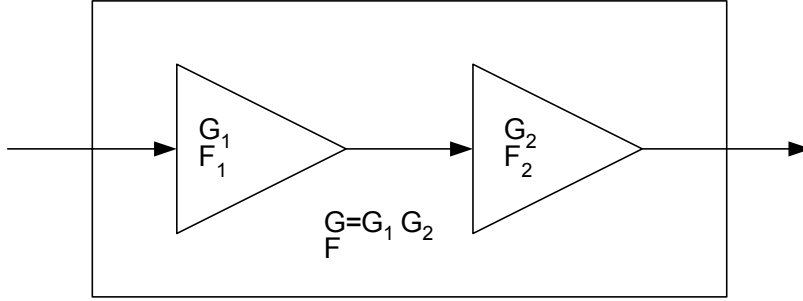
$$F = 1 + \frac{N_{add}}{GN_{in}} = 1 + \frac{N_{add,in}}{N_{in}} \quad (2.4)$$

Where  $N_{add,in}$  is the input-referred added noise from the amplifier defined as  $N_{add,in} = N_{add}/G$ .

### 2.2.2 Noise Figure Calculations for Cascaded Blocks

In the previous section, the definition of the noise figure for a single circuit block has been discussed. In a receiver, however, the overall system noise figure that is resulted from cascaded circuit blocks in the receiver chain must be calculated. The cascaded noise figure depends strongly on the noise figures of individual blocks as well as gain distribution of the receiver chain. If there are two blocks cascaded to each other as shown in figure 2 and the matching is done properly, the total output noise is then given by:

$$P_{noise,out} = F_1 P_{noise,in} G_1 G_2 + (F_2 - 1) P_{noise,in} G_2 \quad (2.5)$$



**Figure 2.2** Cascaded blocks

$G_1$  and  $G_2$  are the power gains for each block in the given matching condition.  $F_1$  and  $F_2$  are the noise figures for each block. The output SNR of the cascaded blocks is then given by

$$SNR_{out} = \frac{S_{out}}{P_{noise,out}} = \frac{S_{in} G_1 G_2}{F_1 P_{noise,in} G_1 G_2 + (F_2 - 1) P_{noise,in} G_2} = SNR_{in} \left( \frac{1}{F_1 + \frac{(F_2 - 1)}{G_1}} \right) \quad (2.6)$$

Finally, the total cascaded noise figure can be calculated:

$$F = \frac{SNR_{out}}{SNR_{in}} = F_1 + \frac{(F_2 - 1)}{G_1} . \quad (2.7)$$

As can be seen from the equation (2.7) the total noise figure of the cascaded blocks depends on the noise figures of both stages and on the gain of the first stage. If  $G_1$

is large, noise from the later stage will have less effect on the overall noise figure. As a result, the first block in the receiver must exhibit low-noise and have at least moderate gain, which is usually called a low-noise amplifier.

### 2.2.3 Relationship between Noise Figure and Sensitivity

There is a direct relationship between the noise figure of the amplifier and the sensitivity of the receiver. It can be derived from noise floor and the required SNR at the input. Since the required SNR at the output of the receiver is set by top-level specifications such as modulation techniques and bit-error-rate (BER), it is usually fixed for given applications. This number is usually derived carrier-to-noise ratio (CNR), which is the ratio between the carrier power and the integrated noise power in the frequency band. Once the CNR is known, the required receiver input SNR can be easily calculated as:

$$SNR_{in}(dB) = CNR_{out}(dB) + NF(dB) \quad (2.8)$$

Finally, the expression for the sensitivity is given by:

$$Sensitivity(dBm) = SNR_{in}(dB) + NoiseFloor(dBm) + 10\log(BW)(dB) \quad (2.9)$$

BW is the bandwidth of the communication channel.

## **2.3 Selectivity**

In the last section, we discussed the performance of the receiver in terms of sensitivity to the desired signal without considering the fact that there are also interfering signals received at the receiver. The receiver selectivity is a performance measure of the ability to separate the desired signal from these unwanted interfering signals. It usually becomes important in the near-far situation where the desired signal is weak and there is a strong adjacent-band/channel interfering signal at the receiver input.

There are no clear quantitative measures for the selectivity, especially at the circuit level. It is usually specified in physical layer as blocking masks, in which can be used to obtain the filtering, nonlinearity, and phase noise requirements in the circuit. The other test related to sensitivity of the receiver is the third-order intermodulation or two-tone test. In this case, a pair of undesired signals is applied to the receiver in a way that its third order intermodulation will line up in the same band as the desired signal. We will discuss in details on these specifications and tests in the incoming sections.

### **2.3.1 Blocking Performance**

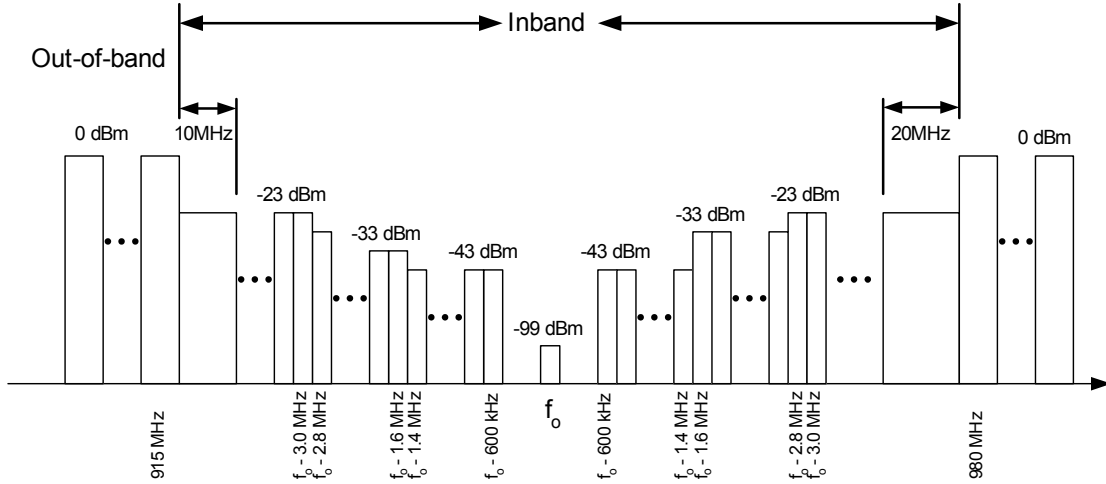
Blocking performance is usually specified with a desired signal applied to the receiver at 3dB above the required sensitivity. Simultaneously, an additional signal, called a blocker, is also applied to the receiver at a defined power level and offset from the carrier. In this condition, the receiver must maintain the required bit error rate (BER) in the presence of blocking signal.

A strong blocker can degrade the receiver performance in several ways. First of all, it can cause gain compression as well as degradation of the noise figure of the receiver. This effect directly reduces the sensitivity of the receiver for the desired signal

[2.1]. The second problem comes from nonlinearity of the system. When the large blocker goes through second-order nonlinearity in the receiver chain, it can mix with itself down to very low frequency and creates problems especially in the direct conversion or low-IF receivers. Detailed analysis about nonlinearity will be discussed in the next section. Lastly, the strong blocker can mix with the local oscillator sidebands resulted from its phase noise. The mixed signal can potentially be in the same frequency band as the desired signal, effectively decreases the signal to noise ratio. More details about the reciprocal mixing can be found in [2.2].

An example of the blocking definition is shown in figure 2.3 below for the GSM 900 standard [2.3]. The blocking test is performed by applying a GMSK modulated signal at 3dB above the required sensitivity, along with the signal-tone blocker at the input of the receiver. The blockers are located at the frequencies of 200 kHz increments away from the desired signal with the amplitudes shown in the figure 2.3. To pass the test, the receiver must maintain the bit-error-rate to be within the specifications.

There are two types of blockers: Inband and out-of-band blockers. Usually, the band-select filter in front of the receiver will filter out the out-of-band blockers. As a result, those blockers will be highly attenuated before actually arriving at the real receiver input. However, this is not the case for Inband blockers where all the signals are in the passband of the filter.



**Figure 2.3** GSM 900 Blocking Definition

### 2.3.2 Second-Order Nonlinearity

As mentioned previously, second-order nonlinearity in the receiver blocks causes a lot of problems especially in direct-conversions or low-IF receivers. This can be understood by examining an expression that relates the input and output signals of a block. Firstly, assuming that we have a relationship given by:

$$S_{out}(t) = a_1 S_{in}(t) + a_2 S_{in}^2(t) + a_3 S_{in}^3(t) + \dots \quad (2.10)$$

Where  $S_{in}(t)$  is the input signal and  $S_{out}(t)$  is the output signal. If the input signal (the blocker) is a sine wave, we then have:

$$S_i(t) = S_i \cos(\omega_b t) \quad (2.11)$$

Where  $\omega_b$  is the frequency of the blocker. Applying equation 2.11 to equation 2.10, the output terms created by the second-order nonlinearity is then given by:

$$S_{out}(t) = a_2 (S_i \cos(\omega_b t))^2 = a_2 S_i^2 \left( \frac{1}{2} + \frac{\cos(2\omega_b t)}{2} \right) \quad (2.12)$$

There are two components in the right hand side of equation 2.12, one is located at the DC and the other one is located at the frequency of  $2\omega_b$ . This DC component can superimpose onto the baseband signal at DC and degrades the receiver performance. This problem becomes problematic in direct conversion receivers with the presence of a strong blocking signal.

Defining second order harmonic distortion and second order intermodulation as in [2.4], the expressions for  $HD_2$  and  $IM_2$  are given by:

$$HD_2 = \frac{\frac{a_2}{2} S_i^2}{a_1 S_i} = \frac{1}{2} \frac{a_2}{a_1} S_i \quad (2.13)$$

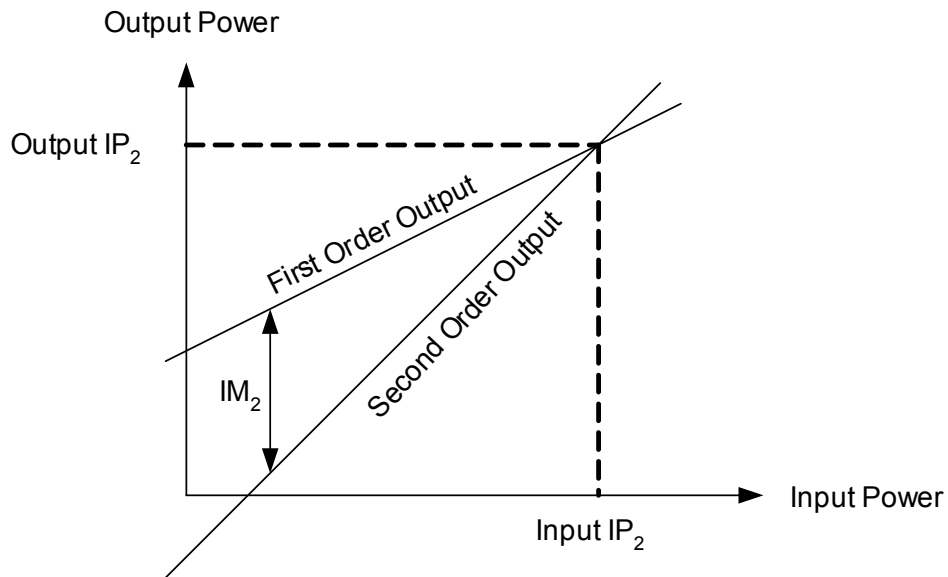
$$IM_2 \cong HD_2 + 6dB \quad (2.14)$$

Since  $IM_2$  increases linearly with input signal level, there will be an intercept point where the interpolated  $IM_2$  is equal to the extrapolated first-order output signal (figure 2.4). The second-order input intercept point ( $IIP_2$ ) is an important figure of merit in receiver designs and given by:

$$IIP_2 = \frac{a_1}{a_2} \quad (2.15)$$

Given the  $IIP_2$ , one can calculate the output  $IM_2$  for a given input blocker power by using the equation:

$$IM_2(dB) = P_{blocker}(dB) - IIP_2(dB) \quad (2.16)$$



**Figure 2.4**  $IM_2$  plot and  $IIP_2$  intercept point

### 2.3.4 Third-Order Nonlinearity

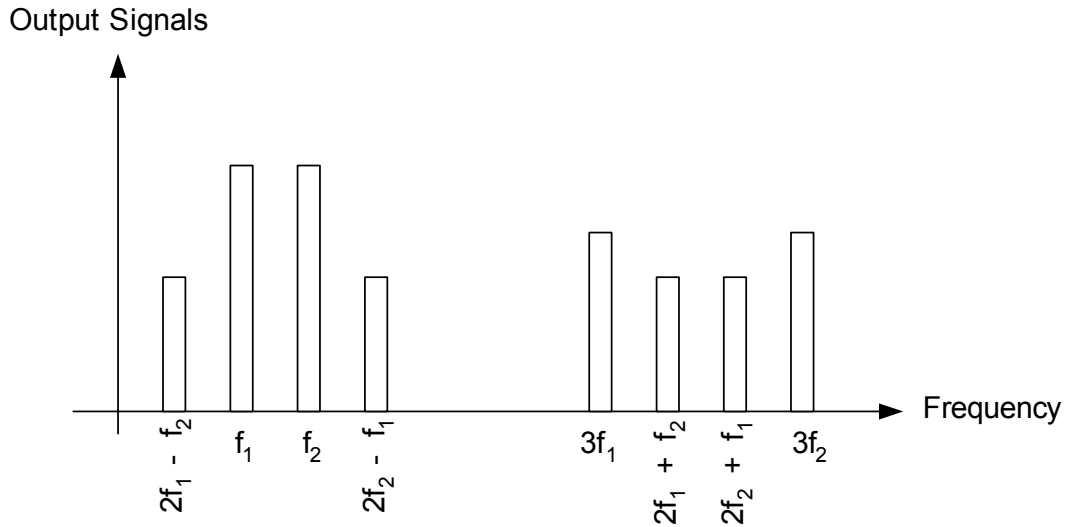
Another important type of nonlinearity in the receiver system is the third-order nonlinearity. Problems associating with the third-order nonlinearity arise from two out-of-band signals passing through the nonlinear blocks. Assuming that these two signals are sinusoidal, we can write them combined as an input signal:

$$S_i(t) = S_1 \cos(\omega_1 t) + S_2 \cos(\omega_2 t) \quad (2.17)$$

After  $S_i(t)$  passes through the third order nonlinearity in equation 2.10, several spectrum at different frequency are generated. After simplification, we get:

$$\begin{aligned} a_3 S_i^3 = & \frac{a_3 S_1^3}{4} (\cos(3\omega_1 t) + 3 \cos(\omega_1 t)) + \frac{a_3 S_2^3}{4} (\cos(3\omega_2 t) + 3 \cos(\omega_2 t)) + \\ & \frac{3}{4} a_3 S_1 S_2^2 [2 \cos(\omega_1 t) + \cos((2\omega_2 - \omega_1)t) + \cos((2\omega_2 + \omega_1)t)] + \\ & \frac{3}{4} a_3 S_1^2 S_2 [2 \cos(\omega_2 t) + \cos((2\omega_1 - \omega_2)t) + \cos((2\omega_1 + \omega_2)t)] \end{aligned} \quad (2.18)$$

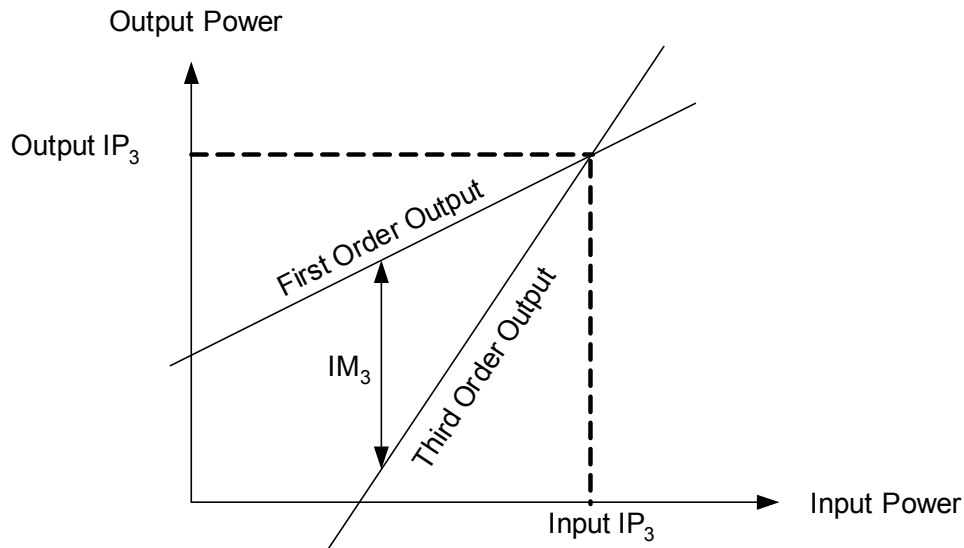
The graphical presentation of the equation 2.18 is shown in figure 2.5. There are linear terms ( $\omega_1, \omega_2$ ), third order harmonics ( $3\omega_1$  and  $3\omega_2$ ), and third-order intermodulation terms ( $2\omega_2 - \omega_1, 2\omega_1 - \omega_2, 2\omega_2 + \omega_1, 2\omega_1 + \omega_2$ ).



**Figure 2.5** Third-order products in frequency domain

One interesting point is that if the tow-tones are closely spaced to each other, some of the  $IM_3$  products will lie just next to  $\omega_1$  and  $\omega_2$ . If the desired channel is located

at either  $2\omega_2 - \omega_1$  or  $2\omega_1 - \omega_2$ , it will experience interference by these components. This is often the most concerned case for receiver application where there might be alternate band users that present very close in frequency to the receiver's desired channel. .



**Figure 2.6** Third order intercept points

Figure 2.6 is the logarithmic plots between output and input signals assuming the same power of the two-tones, the third order intermodulation grows with the input power at three times the rate at which the linear components increases. The third order intercept point ( $IP_3$ ) is defined to be the intersection of the two lines. The horizontal coordinate of this point is called the input  $IP_3$  ( $IIP_3$ ), and the vertical coordinate is called the output  $IP_3$  ( $OIP_3$ ). Using equation 2.16, the  $IIP_3$  can be calculated by equating the linear term and the  $IM_3$  term and given by:

$$IIP_3 = \sqrt{\frac{4}{3} \frac{a_1}{a_3}} \quad (2.19)$$

Alternatively, if the IIP3 and the power of two-tone signals are given, the input referred IM<sub>3</sub> power can be expressed as (all units are in dB):

$$IM_{3,in} = IIP_3 - 3(IIP_3 - P_{in}) = 3P_{in} - 2IIP_3 \quad (2.20)$$

For cascaded nonlinear stages like the one in figure 2.2, the overall IIP3 is affected by the nonlinearity of each block and gain distribution. As shown in [2.5], the overall IIP<sub>3</sub> is given by:

$$\frac{1}{IIP_{3,overall}^2} \approx \frac{1}{IIP_{3,1}^2} + \frac{G_1^2}{IIP_{3,2}^2} + \frac{G_1^2 G_2^2}{IIP_{3,3}^2} + \dots \quad (2.21)$$

Where IIP<sub>3,k</sub> and G<sub>k</sub> are the voltage IIP<sub>3</sub> and voltage gain for the block k. If there is one block dominating the overall third-order nonlinearity of the system, the IIP<sub>3</sub> can be estimated as [2.6]:

$$IIP_{3,overall} \approx \min \left[ IIP_{3,1}, \left( \frac{IIP_{3,2}}{G_1} \right), \left( \frac{IIP_{3,3}}{G_1 G_2} \right), \dots \right] \quad (2.22)$$

## 2.4 Receiver Dynamic Range

Dynamic Range (DR) of a receiver is defined as the ratio of the maximum input level that the circuit can tolerate to the minimum input level that is still detectable. The

quantitative definitions differ from applications to applications. In analog circuits such as A/D converters, it can be defined as a ratio between “full-scale” (FS) input level and the input level for which SNR=1. In RF receivers, however, it is very hard to define FS input level. The commonly used way is to define the upper limit of the input power as the maximum two-tone input level at which the produced output IM<sub>3</sub> is still below the noise floor. Such a definition is called the “spurious-free dynamic range” (SFDR) [2.5].

Rewrite the equation 2.20, we have:

$$P_{in} = \frac{2IIP_3 + IM_{3,in}}{3} \quad (2.23)$$

The integrated noise floor over the bandwidth (N) at the input of a receiver is given by:

$$N_{in}(dBm) = NoiseFloor(dBm) + 10\log(BW)(dB) \quad (2.24)$$

The *input referred* integrated noise floor at the *output* of the receiver is then given by:

$$N_{out,in}(dBm) = N_{in}(dBm) + NF(dB) \quad (2.25)$$

The input referred IM<sub>3</sub> must be equal or less than N<sub>out,in</sub>, this gives us:

$$P_{in,max} = \frac{2IIP_3 + N_{out,in}}{3} \quad (2.26)$$

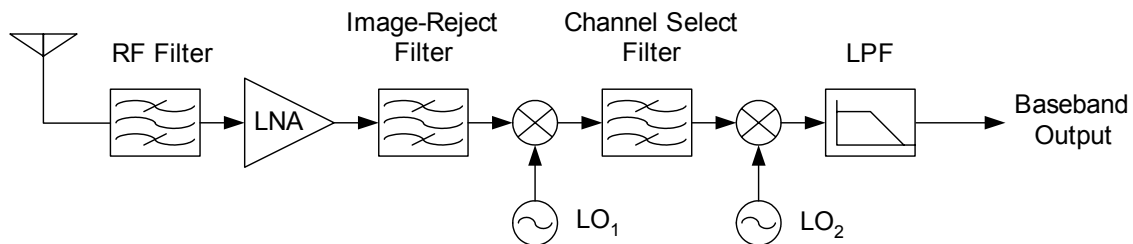
Since the lower bound of the input power is the sensitivity or minimum detectable signal (MDS) of the receiver,

## 2.5 Receiver Architecture Reviews

The basic understandings of receiver functionality and figure of merits have been presented in the previous sections. Now we will change our focus into how to design receiver systems to meet both selectivity and sensitivity requirements. In this section, the two most popular receiver architectures, heterodyne receivers and homodyne receivers, will be reviewed. The contents in this section follow the reviews in [2.7].

### 2.5.1 Heterodyne Receiver

The heterodyne architecture has been used in the wireless receiver for years [2.8] and is the architecture that provides superior sensitivity and selectivity as will shown later. The basic block diagram of the receiver is shown in figure 2.7. Right after the antenna, there is a RF bandpass filter used to filter the out-of band signal following by the low noise amplifier (LNA), image-reject filter, RF mixer, channel select filter, IF mixer, and finally the low-pass filter and baseband processing.



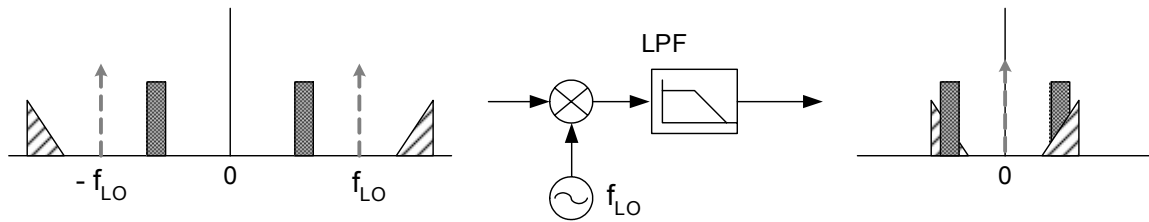
**Figure 2.7** Heterodyne receiver architecture

The main concept of this architecture is that the frequency translation process is divided into two steps. The first one is the translation of the signal from radio-frequency (RF) to the intermediate frequency (IF). The other one is the frequency translation from IF to baseband. The channel filtering takes place at the IF frequency by using a bandpass filter with *fixed* center frequency at the IF. This means that the channel selection takes place at the first mixing process by using the local oscillator (LO) frequency such that the RF signal is shifted down by different amounts to center the desired channel at the IF. By doing the channel filtering at the fixed IF frequency, the requirements on the channel-select filter is greatly relaxed. If we want to do this job at the RF frequency, this would require a tunable RF filter with prohibitively high Q.

The RF bandpass filter is a fixed frequency filter that attenuates out-of-bands signals. The low noise amplifier then provides primary gain for the receiver front-end. As shown in the previous sections, this first block in the receiver chain (besides the bandpass filter) has significant impact on the overall noise in the system. Thus, the main objective of the LNA design is to provide large gain with minimal noise. The other constraint in the LNA design is that its input impedance has to match with the output impedance of the RF filter, which is usually  $50\Omega$ .

Since the components at IF frequency can be created by RF signals on both sides of the LO, there will be an undesired image signal that will be superimposed on the desired signal after the first mixing (figure 2.8). This signal can be very large and may interrupt all the information if not treated properly. In this case, an image reject filter is used before the first mixing to attenuate the image of the desired RF signal.

Although the RF bandpass filter suppresses the image signal by some extent, it will be amplified by the LNA before the mixing. This is why the image-reject mixer is placed right before the mixer. The other benefits of having this filter is that noise in the image band will be reduced as well.



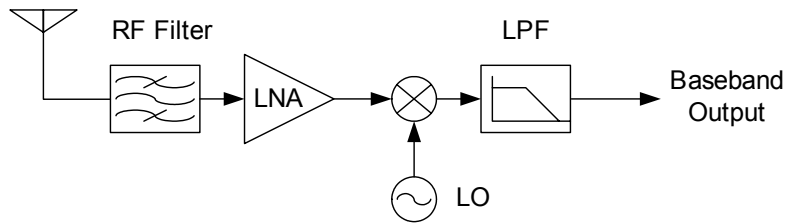
**Figure 2.8** Image Problem

As discussed, the heterodyne architecture provides superior selectivity performance due to the benefits from having the IF stage. However, it requires many functional blocks in the system, in which many of them are very hard to be integrated on-chip. For example, the image-reject and channel-select filters are difficult to be implemented on-chip finite  $Q$  of the on-chip inductors.

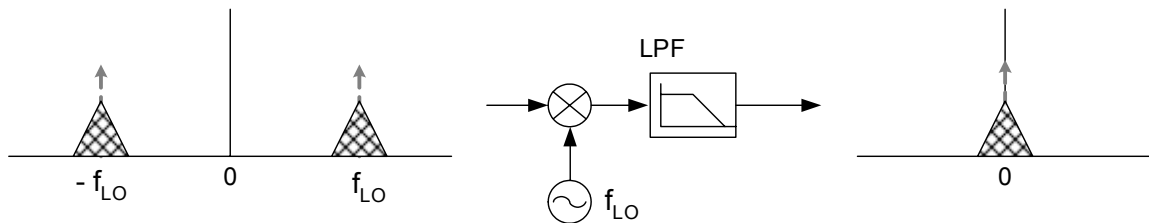
### 2.5.2 Homodyne Receiver

In homodyne receiver, shown in figure 2.9, the RF signal is mixed directly to DC (or near DC) through matching of the LO frequency with the center frequency of the RF passband. In the direct-conversion case where the signal at RF is converted to baseband directly, the signal is placed on both sides of the LO frequency as illustrated in figure

2.10. Thus, an image-reject filter is not needed in this case. In addition, since the channel filtering filter is now done at baseband, it is possible to be implemented as a high-Q on-chip low-pass filter.



**Figure 2.9** Homodyne Receiver



**Figure 2.10** Direct-conversion without image problem

The direct-conversion system, however, does have some serious problems not presented in heterodyne systems. Because the signal is now mixed directly to DC, any DC offset in the receiver path will potentially corrupt the desired signal or saturate the signal path. One way to remove the offset is by placing an AC coupling capacitor at the mixer output. However, this negatively impacts the bit-error-rate since the signal energy at DC will be removed as well. In high-bandwidth system such as wireless LANs, an on-

chip AC coupling capacitor might be used to mitigate the offset at DC without significant penalty [2.9]. However, in the system with narrower channel bandwidths, the AC coupling capacitors are sized such that they must be placed off-chip [2.10]. Techniques used to reduce the DC content of the signal through coding or redefinition of the baseband signal can be used to alleviate this problem. The other approach to remove the offset is by using the training signal to estimate the existing DC offset. Based on the estimation, the offset can be removed or neglected from the mixer output [2.11].

An alternative to address the DC offset problem in the direct-conversion receiver is the low-IF architectures [2.12]. In this case, the RF signal is down-converted to a very low IF rather than baseband. In this case, the DC offset problem is relaxed since the power at DC can be removed by using an on-chip AC coupling capacitor without affecting the desired signal much. However, the image becomes a problem in this case because the signal is on the only one side of the LO frequency. Since the image power is set by the blocking profile and usually gets stronger when the frequency moves away from the desired carrier, the IF frequency is usually not more than one or two channel away from the DC. All of the image rejection must be performed with some Weaver-like structures and depends strongly on the matching between I and Q paths of the receiver. The other drawbacks of this architecture are that it requires higher bandwidth of the baseband blocks because the signal is not moved to higher frequency.

### **2.5.3 Image-Reject Mixers and Complex Filters**

To solve the image problem in heterodyne or low-IF receivers without using an off-chip image-reject filter, several systems have been proposed which cancel the image. These systems called image rejected architectures. The most common ones are Hartley

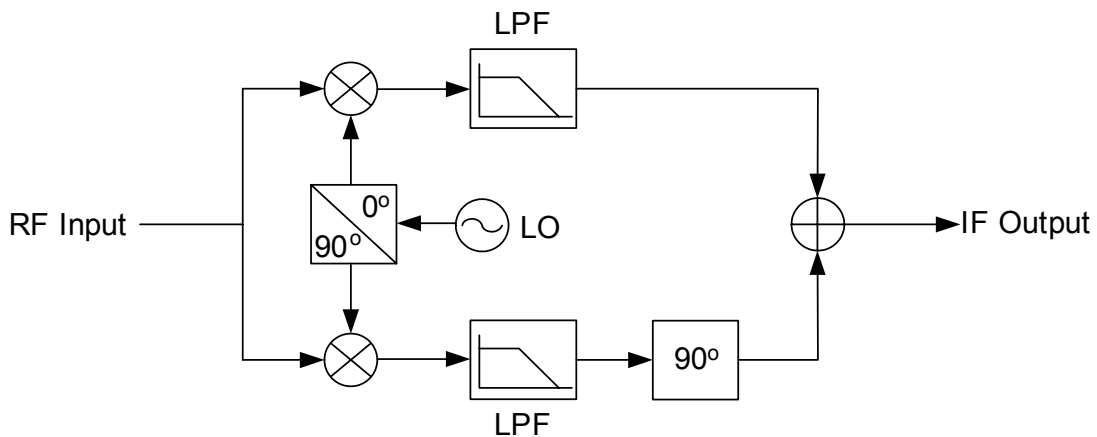
image reject mixers, Weaver image-reject mixers, and complex filters which will briefly reviewed in this section. More complete descriptions and analysis on these architectures can be found in [2.5], [2.13]

### 2.5.3.1 Hartley Architecture

The Hartley architecture is shown in figure 2.21. Note that the 90° phase-shifter is a Hilbert transformer with the transfer function:

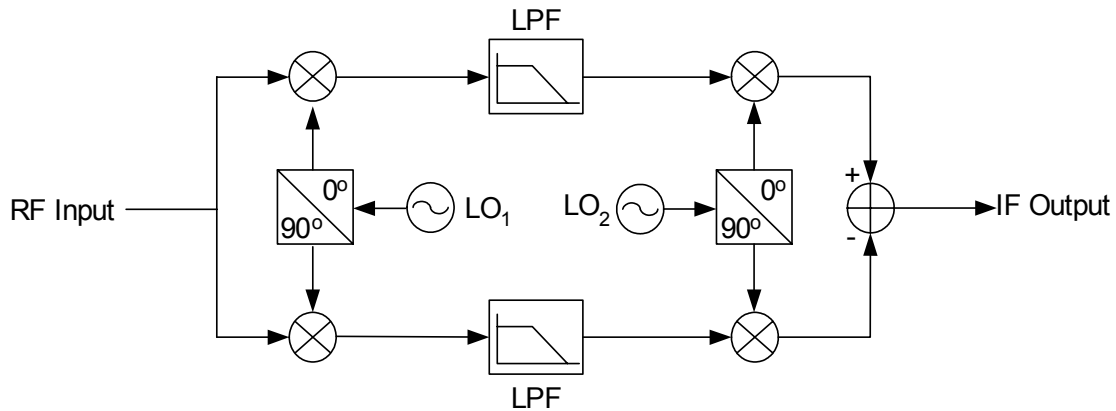
$$H(j\omega) = -j \operatorname{sgn}(\omega) \quad (2.27)$$

The multiplication of the RF signal with the 90° phase-shifted LO followed by the 90° degree phase-shift inverts the signal on one side of the LO, hence distinguishing the signal from the image. Adding this to the signal that is downconverted with nonphase-shifted LO leads to image-rejection. A disadvantage of this architecture is the need of a wideband phase-shifter that provides 90° phase shifts for the entire signal bandwidth.



**Figure 2.11** Hartley Architecture

### 2.5.3.2 Weaver Architecture



**Figure 2.12** Weaver Architecture

Unlike the Hartley architecture, the Weaver architecture uses two additional mixers placed after the low pass filters to perform the phase-shifting instead of using a wideband phase shifter. The RF signal is first downconverted to a “temporary” intermediate frequency, then downconverted once again to the “final” IF. After the first down conversion, one path is multiplied by the sine wave, which is simply the phase shifted cosine wave, equivalently downconverting the signal to the output frequency and phase-shifting by  $90^\circ$  at the same time. The other path, which is multiplied by the cosine wave, is downconverted without the phase shift. Like in the Hartley architecture, summing these two paths results in image rejection.

One obvious advantage of using the Weaver architecture is that the wideband is now removed. Although the  $90^\circ$  phase shifters for the LO quadrature signals are needed, they are narrowband and should be easier to design.

### 2.5.3.3 Complex Filters

In addition to image-reject mixers, complex filters are important and widely used in receiver designs especially in low-IF architectures [2.14], [2.15]. Complex filters use cross coupling between the real and imaginary signal paths in order to realize filters having transfer function that do not have conjugate symmetry (in frequency domain) of real filters. This implies that their transfer function have complex coefficients. The filters can be realized using basic operations of addition and multiplication, and delay operator for discrete-time digital filters or the integrator operator for continuous-time analog filters. Interested readers can get more information on complex mixers in [2.13].

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# Universal Receiver Architectures

## 3.1 Introduction

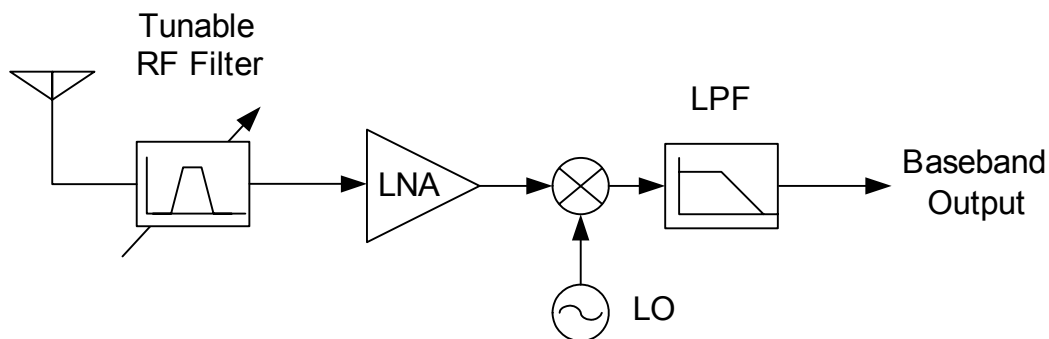
In the past few years, there have been trends in electronics industry to integrate many features including the multi-bands multi-standards compatibility into a single handheld device. This creates the needs for receivers that can be compatible with as many standards as possible. However, most wireless receivers, especially the front-end parts, are optimized to work for only one or few standards. As a result, these devices need a lot of individual receivers placed in parallel, with some level of path sharing, which is costly and space-inefficient. In addition, this type of designs also has a forward-compatibility problem since the hardware mainly work with limited number of standards, and will need to be upgraded or replaced whenever new standards are introduced.

Therefore, there are clearly reasons to make a wireless receiver that has multi-standard capabilities as well as is “forward-compatible”. Such a receiver is usually called “universal radio” or “software-defined radio” [3.1]. Another application of a universal radio receiver is the cognitive radio [3.2]. Cognitive radio is a transceiver with a special ability to adapt itself to the environment.

In this chapter, we will focus on the preliminary design architectures and issues on the design of universal radio front-ends. Firstly, the challenges and limiting factor in designing a broadband receiver will be discussed. One important issue is that most of the existing receiver topologies are designed for a fixed single band or only few bands [3.3], [3.4]. Next, we will investigate the possible architecture for universal radio receivers based on the existing topologies presented in the previous chapter. Comparisons between many topologies will be discussed in terms of suitability for integration and multi-band multi-standards capabilities. Finally, performance estimation of a broadband receiver based on the selected topology will be discussed.

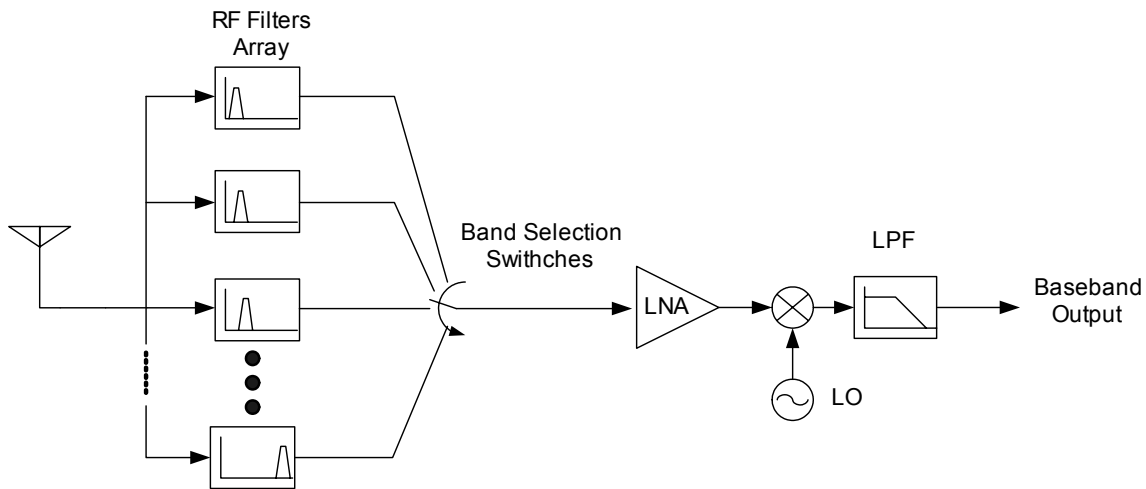
### 3.2 Architectures for Universal Radio Receivers

Unlike conventional narrow-band receivers, the universal receiver front-ends must be able to detect and process signals at different frequency bands. Since the operations are still narrow-band, one way to implement the receiver is to use a high-Q tunable RF bandpass filter for frequency band selections in conjunction with broadband LNA and mixer as shown in figure 3.1. However, such a filter is hard, if not impossible, to be implemented on chip [3.5].



**Figure 3.1** A multi-band multi-mode receiver utilizing a tunable RF bandpass filter

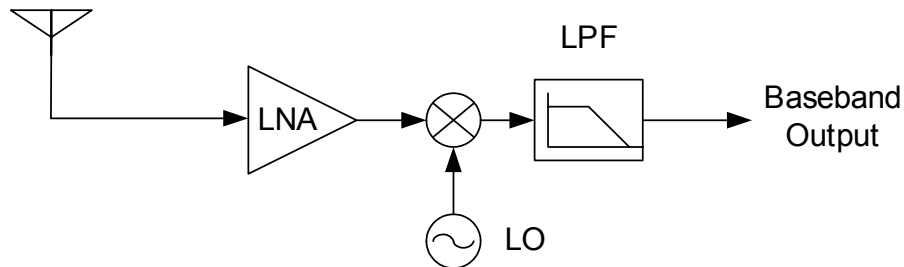
The mentioned problems can be solved by using different high-Q RF bandpass filters for different frequency bands in conjunction with switches that select the frequency band to use. This figure of this method is shown in figure 3.2. Although, this method is good for up to few narrow frequency bands, it is becoming impractical for generic universal radio or configurable radio, where the receiver must be able to operate at *any* bands in the frequency range of interests hence would requires too many bandpass RF filters.



**Figure 3.2** A receiver using multiple RF filters and switches

One obvious way to solve the problem of using too many RF bandpass filters is to not using them at all. This leaves us the broadband receiver with no bandpass filterers for the front-ends, shown in figure 3.3. Since there is no bandpass filtering, any big interference signals can saturate the signal path or create intermodulation products that overtake the desired signal. Therefore, the linearity and gain compression point

requirements in this type of receiver are very high. In general, very linear RF blocks (LNA and mixers) would be needed.

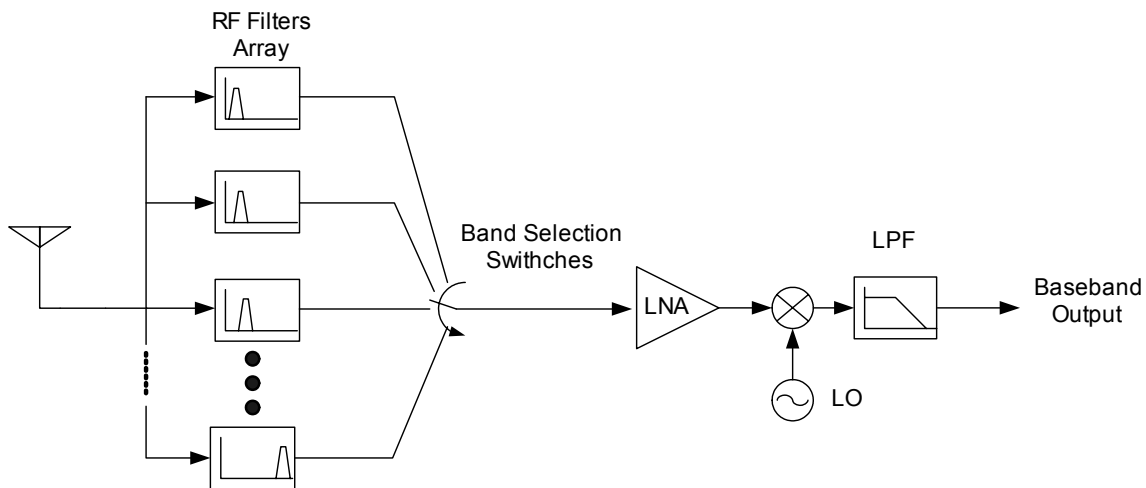


**Figure 3.3** A broadband receiver with no RF bandpass filtering

If the receiver is very broadband, there will be problems with the harmonic distortion as well as sub-harmonic-mixing. For example, if the receiver takes in signals from 0.5MHz to 5GHz, a strong signal at 0.8GHz will create a third-order harmonic distortion at 2.4GHz and interrupt any desired signals at that frequency. Likewise, if the desired signal and LO are at 0.8GHz (narrow channel bandwidth), a strong signal at 2.4GHz will sub-harmonically mix with  $3F_{LO}$  and potentially corrupts the desired signal. Moreover, signals at 0.9GHz and 2.4GHz can create  $IM_2$  and corrupt desired signals at 1.5GHz.

Unless these problems are addressed in different ways, the ratio between highest frequency and lowest frequency should be lower than two. This can be done by placing an RF bandpass filter for a “group” of bandwidth. For example, one might use a filter with the passband ranges from 0.8GHz to 1.5GHz to avoid any conditions described above. If more bandwidth is needed, multiple bandpass filters can be used as shown in figure 3.4. Although this might look similar to the architecture in figure 3.2, the number

of required RF bandpass filters is different. For example, to cover from 0.5GHz to 5GHz of frequency bands, the number of filters needed in this topology would be only 3 or 4 no matter how many standards exist in the range. This architecture, however, still requires out-of-band blocking and linearity requirements as the one without any bandpass filter. If needed, multiple broadband LNAs can be used for signals from multiple frequency groups as well.



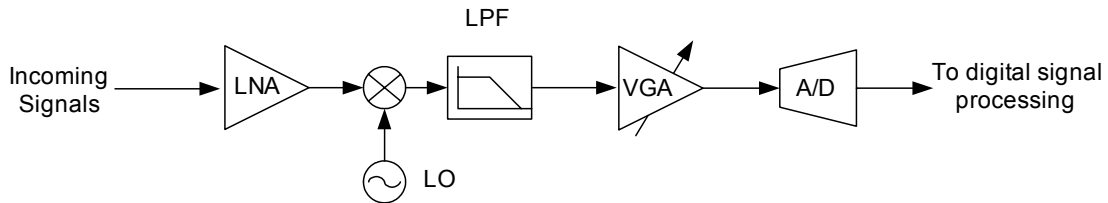
**Figure 3.4** A receiver with multiple “wideband” RF bandpass filter

### 3.3 Broadband Receiver Prototype

Having reviewed the possible topologies for universal receivers, one can see that a broadband receiver is essential in most architectures being discussed. In this section, we will propose a simple receiver architecture that is broadband and highly-tunable.

The conceptual diagram of the receiver is shown in Fig. 3.5. The major building blocks are the LNA, mixer, synthesizer, IF Filter and VGA, and A/D converter. The LNA is broadband with high linearity and low noise over the operating frequency range. It can

be designed as one broadband LNA, or a few broadband LNAs connected in parallel in order to extend the bandwidth.



**Figure 3.5** Conceptual diagram of the receiver

The I/Q image-rejection mixers (the above conceptual diagram shows only one mixer) downconverts the frequency down to IF with the LO signal from the synthesizer. The LO needs a wideband frequency tuning scheme in order to work with multiple bands and standards. Also, it is necessary to have a channel bandwidth adjustment scheme to accommodate different channel bandwidth for different standards. The two most logical ways are to use the direct conversion topology with tunable low-pass IF filter or low-IF topology with tunable bandpass IF filter. The first approach is simpler but may suffer from the DC offset and  $1/f$  noise problems. The second approach is more complicated since it needs a tunable bandpass filter, but the low frequency issues are eliminated.

### 3.4 Performance Estimation

To get the idea on how well the receiver can operate, we calculated the NF,  $IIP_3$ , and some blocking specifications based on the following assumptions on building blocks shown in table 1:

**Table 1** Assumptions on the building blocks

	Gain (dB)	NF (dB)	IIP3 (dBm)	P -1dB (dBm)
LNA	16	3	0	-10
Mixer	-5	12	20	10
Filter+VGA @ Min Gain	10	10	10	0
Filter+VGA @ Max Gain	70	5	-10	-20

- Assume that the A/D is 10bit
- Assume that the filter has 0dB gain and is very linear with high stopband attenuation

From the data above, the total receiver noise figure is about 5dB, dominated by the LNA NF. The maximum input power set by  $P_{-1dB}$  is -31dBm (set by the VGA) and maximum acceptable blocker power is -1dBm (set by the VGA). The receiver can detect a signal of around -100dBm for 100 kHz channel bandwidth and -75 dBm for 100 MHz channel bandwidth.

An A/D with an effective 10 bit resolution gives a dynamic range at the A/D input of around 50dB (assume 10dB of SNR at the A/D input is required). This requirement should be met easily since we have the IF filter to attenuate any unwanted signals.

For calculations of  $IIP_3$ , we ignore the VGA since there is a filter to attenuate any interference in front of it. The  $IIP_3$  of the system is about 0dBm given by the LNA. This results in the maximum blocker power of around -40dBm for -100dBm sensitivity and -30dBm for -80dBm sensitivity.

Reciprocal mixing is also an important issue in receiver designs. For the universal radio, there are a lot of out-of-band blockers that can mix with the phase noise and increase the amount of noise in the desired signal channel. Fortunately, these blockers are very far away from the LO center frequency and do not have any significant effects comparing to in-band blockers. As the results, the phase noise requirement is not very

much different from in the narrow-band case. The reasonably good phase noise of around -120 dBc at 1 MHz is derived from the noise floor and input blocker level.

### **3.5 Conclusion**

In this chapter, we have compared several receiver architectures in terms of their suitability to the universal radio applications. One promising way to implement such a receiver is to use multiple broadband receiver front-ends, in which each of them covers a group of frequencies in the band. This would make a good compromise between using too many narrow-band front-ends and having too much interference from using only broadband front-end.

In addition, the performance of the broadband universal receiver has been estimated. The estimation methodology is similar to narrow-band system except that, in broadband case, there is no narrow-band bandpass filter preceding the LNA that attenuates out-of-band blockers or interference. This results in higher linearity requirement for the LNA and mixer. In our opinion, insertion of a RF variable-gain attenuator [3.6] would be helpful in controlling signal level and should increase the  $P_{-1dB}$  as well as maximum acceptable blocker powers as the expense of the noise figure.

Although the direct conversion and low-IF topologies are suitable for highly configurable multi-mode applications, they are subjected to DC offset and  $1/f$  noise problems. The IF filter must be highly tunable since we have to deal with different standards and signal bandwidths. A low-pass IF filter for direct-conversion is simpler than a bandpass filter for low-IF but there are more low-frequency problems associate

with the direct-conversion topology. In addition, although not mentioned in this chapter, the image-reject mixer as well as I/Q matching must be done carefully.

In terms of future research topics, one interesting problem is the detailed analysis of using broadband front-end for narrow-band applications, especially in practical situations where noise and linearity are not both required in most of the times. Another problem is the tradeoff analysis between the front-end performance and configurability. In addition, since the broadband receiver tends to need higher linearity, a receiver linearization would be an exciting research topic.

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# 4

## CMOS LNA Fundamentals

### 4.1 Introduction

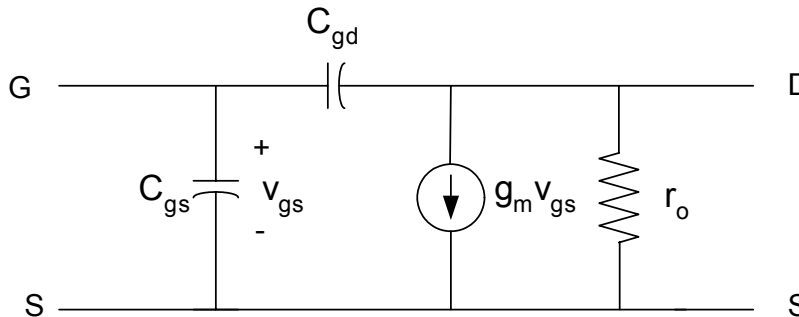
Low-noise amplifier (LNA) serves as the first amplification block in the receive path in a RF receiver. As explained in chapter 2, it is a critical building block in the receiver path since its performance greatly affects both sensitivity and selectivity of the system. In this chapter, the basic properties of CMOS LNA will be investigated. Starting from NQS effects and noises analysis in CMOS transistors in section 4.2 and 4.3, we will then go through a classic two-port theory for noises in section 4.4. Finally, reviews on input matching and topologies of the LNA will be discussed.

### 4.2 Non-Quasi Static Effect

An important issue that needs to be taken into account in the design of narrowband CMOS LNAs is the non-quasi static effect. This effect worsens the noise and gain performance of the LNAs as will be discussed later in this section. The flow in this section follows the procedures in [4.1].

### 4.2.1 Physical Origin

In order to understand the phenomenon, first take a look at a model of MOS transistors operating at low frequencies ( $\omega \ll \omega_T$ ) shown in figure 4.1.

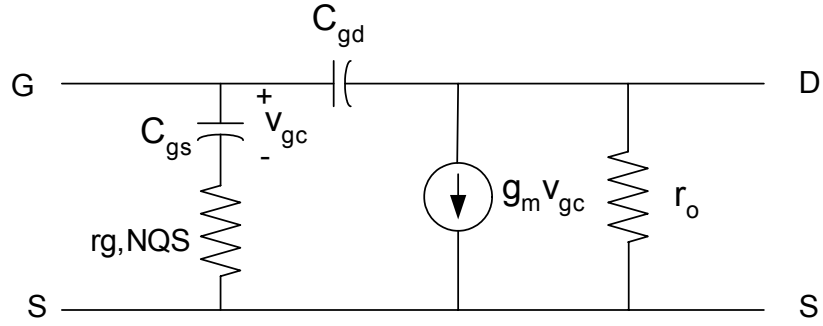


**Figure 4.1** Simple small signal model for MOS at low frequencies

This model works well at low frequencies because the inversion layer channel charge builds up fast enough relative to the frequency of the signal applied to a terminal. However, at high frequency this assumption is not valid due to the finite channel conductance limiting the speed of the build-up of the inversion layer. As a result, the channel needs time to get into equilibrium with the source and drain voltages. This high frequency phenomenon is called non-quasi static effect.

### 4.2.2 First Order Model

Figure 4.2 presents a small-signal non-quasi static equivalent circuit model proposed in [4.2] for a transistor operating in the strong inversion region.



**Figure 4.2** First order small signal model including NQS effect.

The NQS model uses an extra resistance in series with the gate to source capacitance to model the non-quasi static effect. This resistance is referred to as the non-quasi static gate resistance, and it is the effective resistance seen by the gate to source capacitance. The non-quasi static gate resistance is given in the equation below:

$$r_{g, NQS} = \frac{1}{5 g_m} \quad (4.1)$$

Note that the non-quasi static gate resistance is that the derivation was done for long channel transistors without considering short-channel effects.

As mentioned before, the non-quasi static effect occurs when a high frequency signal is applied to the gate. For most practical circuits, the frequency is low enough such that the imaginary part of the impedance (due to  $C_{gs}$ ) is much greater than the real part (due to  $r_{g,NQS}$ ). However, when an inductor is placed in series with  $C_{gs}$  (as is often the case in LNA design), then at the resonance the impedance of the inductor will cancel out

the impedance of the capacitor. As a result, the input impedance is solely determined by  $r_{g,NQS}$ .

## 4.3 Noise Sources in CMOS

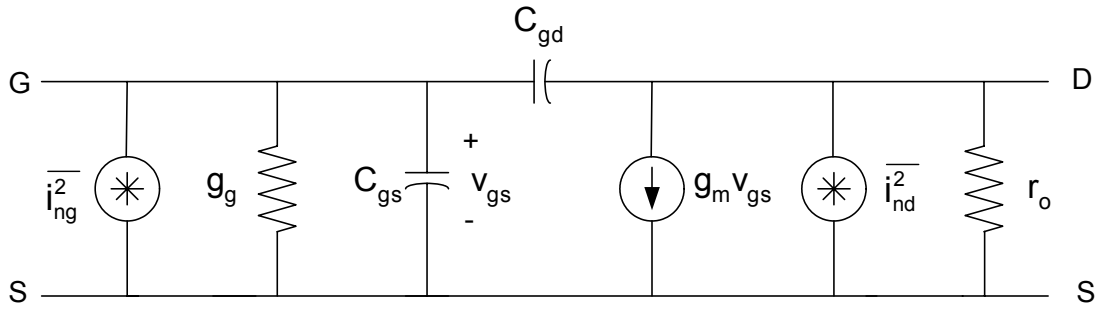
Before beginning an analysis of how to design for low noise, the origins of noise must be identified and understood. This section gives insight into the most important noise source in MOS transistors such as drain current noise, induced gate noise, and flicker noise.

### 4.3.1 Drain Current Noise

Since the channel material in MOS transistors is resistive, it exhibits thermal noise. This noise source can be represented by a current noise generator connecting from drain to source in the small signal model as shown in figure 4.1 and called “drain current noise”. The expression for this noise is given by [4.3]:

$$\overline{i_{nd}^2} = 4kT\gamma g_{d0}\Delta f \quad (4.2)$$

Where  $g_{d0}$  is the drain to source conductance at zero  $V_{ds}$ . The parameter  $\gamma$  has a value of unity at zero  $V_{ds}$  and moves toward 2/3 in saturation for long channel device. In the short channel device, however, the value of  $\gamma$  can be considerably larger (typically 2-3 but can be much higher) due to carrier heating by the large electric field in short channel devices [4.4].



**Figure 4.3** Drain current and gate noise models

### 4.3.2 Induced Gate Noise

The other consequence from the thermal agitation of channel charge, besides drain current noise, is the induced gate noise. This noise is caused by the non-quasi static effect discussed earlier in this chapter. The fluctuating channel potential couples capacitively into the gate terminal, leading to a noisy gate current. This noise is negligible at low frequencies because the coupling effect is small. However, it can be problematic at radio or microwave frequencies. This noise is modeled as a current noise generator connecting from gate to source in the small signal model (see figure 4.3) and maybe expressed as [4.3]:

$$\overline{i_{ng}^2} = 4kT\delta g_g \Delta f \quad (4.3)$$

Where the parameter  $g_g$  is

$$g_g = \frac{\omega^2 C_{gs}^2}{5g_{d0}} \quad (4.4)$$

The parameter  $\delta$  is a gate noise coefficient and equal to  $4/3$  for long-channel devices [4.3], which is twice as large as  $\gamma$ . For short channel devices, however, this value is still not accurately known. The reasonable approximation is that  $\delta$  should continue to be about twice as large as  $\gamma$ . Since  $\gamma$  is around 2-3 for the short-channel device,  $\delta$  should be around 4-6 [4.5].

As mentioned earlier that the gate noise is related to the drain noise. In fact, it is partially correlated to the drain noise, with a correlation coefficient  $c$ , stated in equation 4.5 below.

$$c = \frac{\overline{i_g i_d^*}}{\sqrt{\overline{i_g^2} \overline{i_d^2}}} \quad (4.5)$$

The value for  $c$  is given by [4.2] as  $0.395j$  for long-channel devices. Since the coupling between the gate noise and drain noise is through the gate capacitance, correlation coefficient is the purely capacitive

### 4.3.3 Flicker Noise

The other important noise source in MOS transistors is the flicker noise. The origins of this noise are varied, but mainly attributed to traps associated with contamination and crystal defects. Since MOS transistors conduct current near the surface of silicon where surface acts as traps that capture and release current carriers, their flicker noise components can be large. These traps capture and release carriers in random fashion and the trapping times are distributed in a way that leads to a  $1/f$  noise spectrum.

Flicker noise can be modeled as a current noise generator connecting from drain to source in the small signal model as shown in figure 4.3 and can be expressed by [4.5]:

$$\overline{i_{nf}^2} = \frac{K}{f} \frac{g_m^2}{WLC_{ox}^2} \Delta f \quad (4.6)$$

Where K is a constant varied from processes to processes.  $C_{ox}$  is the gate oxide capacitance per unit area. Note that the flicker is inversely proportional to the area of the gate (WL) because the larger gate capacitance smoothes the fluctuation in channel charges. Also, it is worth mentioning that flicker noise is always associated with a flow of direct currents. If there is now direct current flowing in the device, this noise should be minimal [4.6].

#### 4.3.4 Other Noise Sources

The distributed gate resistance of the CMOS transistor also contributes to the noise in low noise amplifiers. This noise sources is usually modeled as a series resistance at the gate and the noise power is given by:

$$\frac{\overline{v_g^2}}{\Delta f} = 4kTR_g \quad (4.7)$$

$$R_g = \frac{R_{sq} W}{3n^2 L} \quad (4.8)$$

Where  $R_g$  is the gate resistance,  $R_{sq}$  is the sheet resistance of polysilicon, and  $n$  is the number of fingers. The factor 3 comes from the distributed nature of the gate resistance assuming that each finger is only contacted at only one end. If both ends are contacted, then the factor reduces to 12. This noise source can be reduced by increasing the number of fingers used to make a transistor.

Another noise source mentioned in [4.7] is from the resistance due to the lightly doped drain diffusion regions. Because no distinction is made between the source and drain, this resistance is also present at the source, and cannot be mitigated by proper layout. This resistance is given in equation by.

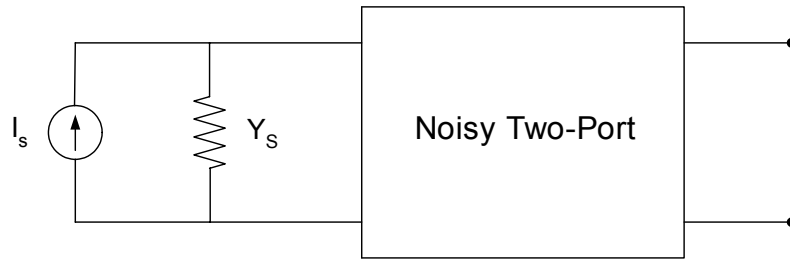
$$R_{source, drain} = \frac{R_{LDS}}{W} \quad (4.9)$$

Where  $R_{LDS}$  is the resistance of a unit width transistor.

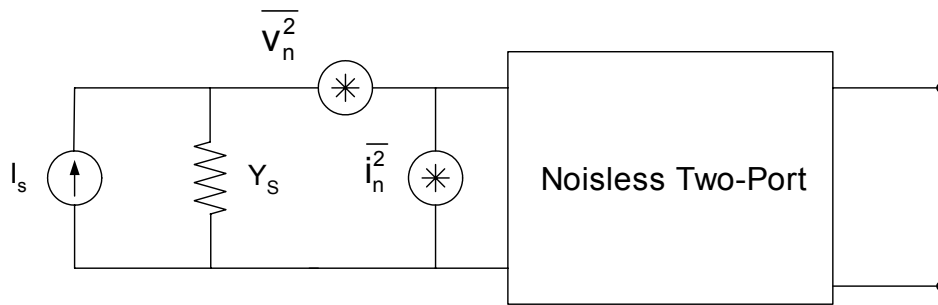
#### **4.4 Two-Port Noise Theory**

In this chapter, we will take a look at noise in the macroscopic points of view using a two-port network. Using the system model will greatly simplify the noise problems as will be shown later in this chapter.

Starting with the model in figure 4.4a, the linear noisy two-port network is driven by a source with admittance  $Y_s$ . If we are interested in only the input-output behaviors, it is not necessary to keep track of all the internal nodes of the circuits. In this case, the noisy two-port can be replaced by a noiseless two-port network with external current and voltage noise generators at the input as shown in figure 4.4b.



(a)



(b)

**Figure 4.4** (a) Noisy two-ports driven by noise source, (b) equivalent noise model

Recall from the chapter 2 that the noise factor is defined as:

$$F \equiv \frac{\text{total output noise power}}{\text{output noise due to input source}} \quad (4.10)$$

All the noise sources are now input referred as in figure 4.4b and the output power contributions from each term is proportional to its short-circuit current at the input. As a result, we can now calculate the noise factor by calculating the total short-circuit mean-square input noise current, and divide that total by the short-circuit mean-square noise current generated from the input source. The expression then becomes:

$$F = \frac{\overline{i_s^2} + \overline{|i_n^2 + Y_s v_n^2|^2}}{\overline{i_s^2}} \quad (4.11)$$

In the equation above, we have assumed that the noise from the source and the equivalent noise generators are not correlated. However, there is a correlation between the current noise generator and the voltage noise generator. We can write  $i_n$  as:

$$i_n = i_c + i_u \quad (4.12)$$

Where  $i_c$  is the part of  $i_n$  that is correlated with  $v_n$  and  $i_u$  is the part of  $i_n$  that is uncorrelated with  $v_n$ . Since  $i_c$  is correlated with  $v_n$ , it can be written as:

$$i_c = Y_c v_n \quad (4.13)$$

The constant  $Y_c$  is known as the correlation admittance [4.5].

Putting the equation (4.12) and equation (4.13) into the equation (4.11), we get a modified expression for the noise factor:

$$F = \frac{\overline{i_s^2} + \overline{|i_u^2 + (Y_c + Y_s) v_n^2|^2}}{\overline{i_s^2}} = 1 + \frac{\overline{i_u^2} + \overline{|Y_c + Y_s|^2 v_n^2}}{\overline{i_s^2}} \quad (4.14)$$

The expression above contains three independent noise sources. We can then define:

$$R_n = \frac{v_n^2}{4kT\Delta f} \quad (4.15)$$

$$G_u = \frac{i_u^2}{4kT\Delta f} \quad (4.16)$$

$$G_s = \frac{i_s^2}{4kT\Delta f} \quad (4.17)$$

Using the equation (4.14)-(4.17), we can then write the noise factor in terms of noise admittances and impedances as followed:

$$F = 1 + \frac{G_u + |Y_c + Y_s|^2 R_n}{G_s} = 1 + \frac{G_u + [(G_c + G_s)^2 + (B_c + B_s)^2] R_n}{G_s} \quad (4.18)$$

At this point, the optimal admittance can be found by taking the first derivatives of the equation above with respect to the source conductance and source susceptance and turning it into zero. This yield:

$$B_s = -B_c = B_{opt} \quad (4.19)$$

$$G_s = \sqrt{\frac{G_u}{R_n} + G_c^2} = G_{opt} \quad (4.20)$$

Substituting equations (4.19) and (4.20) into (4.18) gives the following result for the minimum noise figure:

$$F_{min} = 1 + 2R_n(G_{opt} + G_c) \quad (4.21)$$

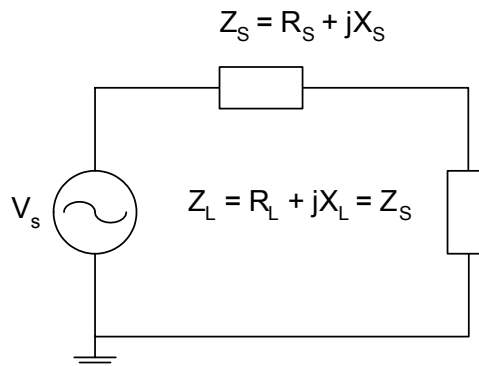
Using the equation 4.21, we get the general expression for noise figure as:

$$F = F_{min} + \frac{R_n}{G_s} [(G_s - G_{opt})^2 + (B_s + B_{opt})^2] \quad (4.22)$$

From equation 4.22, it can be seen that contours of constant noise factor (and noise figure) are circles centered about  $(G_{opt}, B_{opt})$  in the admittance plane.

## 4.5 Impedance Matching in LNA Design

Impedance matching is important in LNA design because often times the system performance can be strongly affected by the quality of the termination [4.7]. For instance, the frequency response of the antenna filter that precedes the LNA will deviate from its normal operation if there are reflections from the LNA back to the filter. Furthermore, undesirable reflections from the LNA back to the antenna must also be avoided. An impedance is matched when  $Z_S = Z_L$  as in figure 4.5.



**Figure 4.5** Condition for an Impedance Match

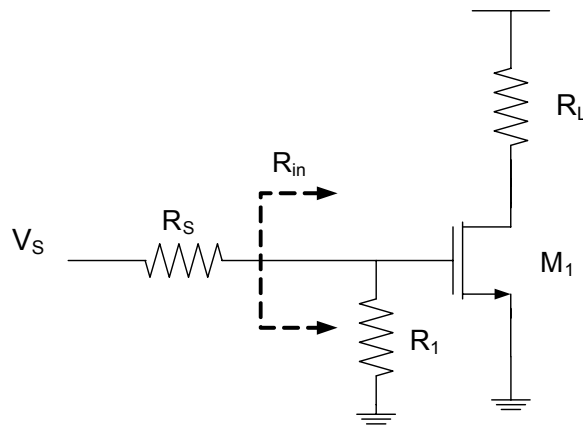
There is a subtle difference between impedance matching and power matching. As stated in the previous paragraph, the condition for impedance matching occurs when the load impedance is equal to the characteristic impedance. However, the condition for power matching occurs when the load impedance is the complex conjugate of the characteristic impedance. When the impedances are real, the conditions for power matching and impedance matching are the same.

## 4.6 LNA Input Matching Topologies

As mentioned in the previous section, impedance matching is very important in LNA designs. In most cases, the source impedance of the LNA is  $50\Omega$  in wireless system. Since the input impedance of the MOS transistor is almost purely capacitive, providing a good match to the source without degrading noise performance is a challenge. In this section, we will investigate a number of circuit topologies that can be used of the task and discuss their properties.

### 4.6.1 Resistive Termination

This is the most straightforward approach to achieve the broadband  $50\Omega$  matching at the input as shown in figure 4.6. The  $50\Omega$ -resistor ( $R_1$ ) is placed across the input terminal of the LNA and hence providing a broadband input matching.

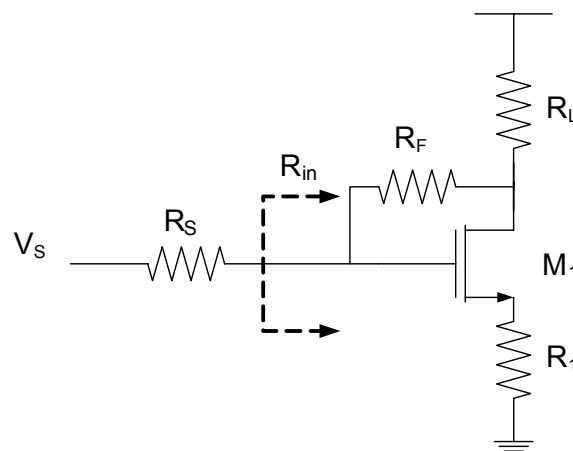


**Figure 4.7** Resistive termination matching

The bandwidth of this matching topology is determined by the input capacitance of the transistor  $M_1$  and can be very high. However, the resistor  $R_1$  adds its own thermal noise to the circuit as well as attenuates the incoming signal by a factor of two before it hits the gate of the transistor. These two effects results in an unacceptably high noise factor of the circuit [4.5] and hence is not practical in most applications. Ignoring all the noises from the transistors, the lower bound of the noise factor is 2.

#### 4.6.2 Shunt-Series Feedback

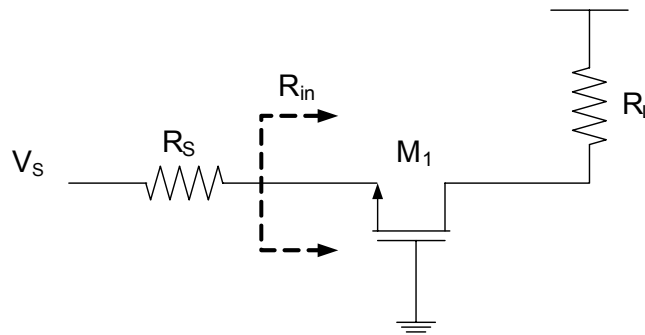
The other method used for getting a good input matching is the shunt-series feedback amplifier as shown in figure 4.7. Unlike in the resistive termination case, it does not attenuate the signal by a noisy attenuator before reaching the gate of the amplifying device and hence the noise figure is expected to be much higher. However, the feedback resistor continues to generate thermal noise of its own. These results in the relatively high noise figure, usually a few decibels above the optimal number [4.5].



**Figure 4.7** Shunt-series feedback matching

### 4.6.3 Common-Gate Input

Another method for realizing a resistive input matching is to use a common-gate configuration. As can be seen in the figure 4.8, the source terminal is used as an input terminal. Since the impedance looking into source of is  $1/g_m$ , it can be set by proper device sizing and adjusting the bias current of the circuit. This creates a drawback of this configuration that  $g_m$  is fixed once the source resistance is know.



**Figure 4.8** Common-gate input matching

This matching method is broadband by nature like the  $g_m$  of the circuit. Since the impedance changes with  $g_m$  of the transistor, we can expect that the matching bandwidth is approximately equal to the  $f_t$  of the device.

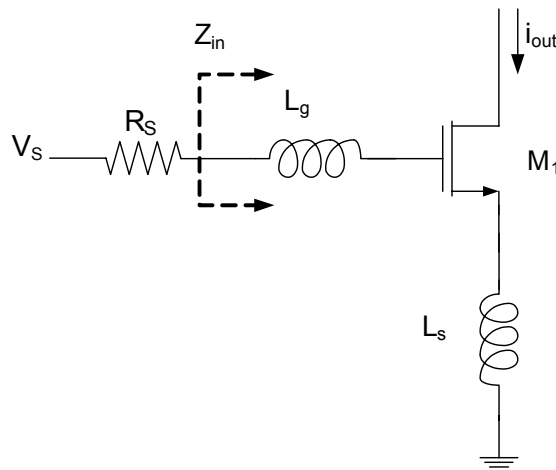
Neglecting gate and flicker noises and assuming a perfect match, we can express the lower bound of the noise figure for the amplifier that uses this matching technique as follow:

$$F \geq 1 + \frac{\gamma g_m}{g_{d0}} \quad (4.23)$$

Numerical value for the lower bound expressed above is about 2.2dB for long-channel devices and 4.8dB for short channel devices [4.5].

#### 4.6.4 Inductive Source Degeneration

Unlike the other previously mentioned techniques, this matching topology provides a perfect match without adding any noise to the system or giving any restrictions on the device  $g_m$ . It uses an inductor as a source degeneration device and has another inductor connecting to the gate as shown in figure 4.9.



**Figure 4.9** Inductive source degeneration matching

Using the small signal analysis and neglecting  $r_{g,NQS}$  as well as the  $C_{gd}$  of  $M_1$ , the impedance looking through the gate inductor can be expressed as:

$$Z_{in} = j\omega(L_g + L_s) + \frac{1}{j\omega C_{gs}} + \omega_T L_s \quad (4.24)$$

Where

$$\omega_T = \frac{g_m}{C_{gs}} \quad (4.25)$$

At the resonance frequency where the inductor impedance and the capacitor impedance are canceled out, the input impedance is then just the last term in the equation (4.24). If the  $r_{g,NQS}$  is taken into consideration, the tuned impedance is then given by:

$$Z_{in}(\omega_0) = R_{eq} = \omega_T L_s + r_{g,NQS} \quad (4.26)$$

Where

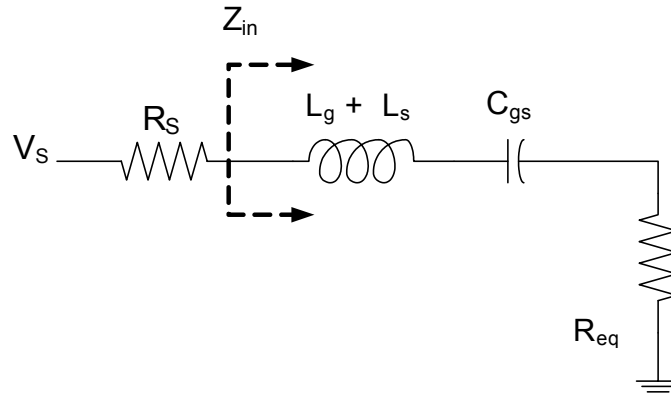
$$\omega_0 = \frac{1}{\sqrt{(L_g + L_s)C_{gs}}} \quad (4.27)$$

Since all the inductors are reactive, they do not add any noise into the circuit. In fact, the LC resonating mechanism improves noise and gain performance of the amplifier. Starting from the equivalent model of the input matching (figure 4.10), the quality factor of the circuit given by:

$$Q = \frac{\omega C_{gs}}{R_{eq}} \quad (4.28)$$

At the resonance, the voltage amplitude across the  $C_{gs}$  is Q times the voltage across the input terminal from the source given matched condition. This effectively increases the transconductance of the input transistor by a factor of Q.

$$G_m = Qg_m \quad (4.29)$$



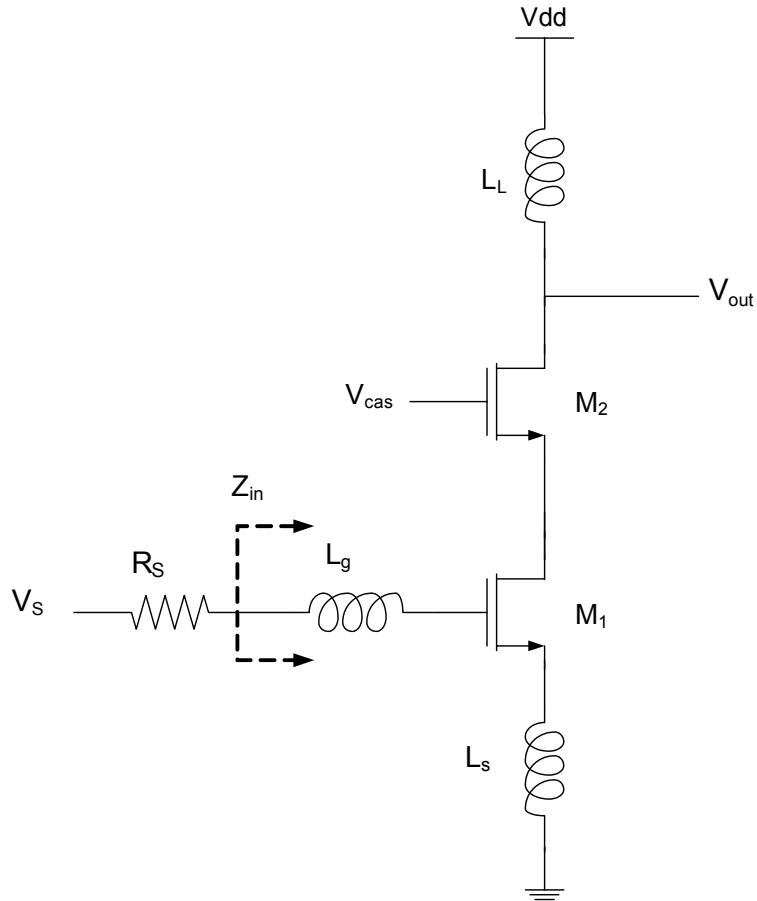
**Figure 4.10** Equivalent Circuit

In typical narrow-band matching, this factor is usually around 3-5. Assuming that the matching network is lossless, this effect helps to reduce the input-referred added noise by a factor of  $Q$  as well as increasing the voltage gain of the circuit by the same factor. As a result, this topology is preferred in most narrow-band applications.

One major limitation of this topology is that the matching is narrow-band. As can directly derive from the equation 4.24, it is a series RLC network with finite  $Q$ . However, since most wireless receivers are narrow-band, this is usually not a big concern.

#### **4.7 Example: CMOS Inductive Degeneration LNA**

Having established the backgrounds in LNA design, now we will turn our focus into a full LNA circuit as an example.



**Figure 4.11** A typical CMOS Low Noise Amplifier

Figure 4.11 shows a circuit that is commonly used in the design of CMOS low noise amplifiers. This circuit uses the input stage described in section 4.5.4 to provide an input match and current gain at the resonant frequency. A cascode is added to the input stage to reduce the interaction between the input tank and output tank as well as the reverse gain from output to the input. This reverse gain reduction effectively increases the stability of the amplifier. Furthermore, the cascode reduces the effect of the  $C_{gd}$  of  $M_1$  by presenting a low impedance node at the drain of  $M_1$  hence the miller-effect of  $C_{gd}$  is mitigated. The output inductor,  $L_L$ , is designed to resonate at  $\omega_o$  with the node capacitance at the output. The input and output tank can be aligned to provide a

narrowband gain, but can also be offset from each other to provide a broader and flatter frequency response [4.5].

## **4.8 References**

- [4.1] R. Lu, “ CMOS Low Noise Amplifier Design for Wireless Sensor Networks”, Master Thesis, UC Berkeley, 2003
- [4.2] Y. Tsividis. *Operation and Modeling of the MOS transistor*. McGraw-Hill, Boston, 1998
- [4.3] A. Van Der Ziel. *Noise in Solid-State Devices and Circuits*. New York: Wiley, 1986
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- [4.5] T. Lee. *The Design of CMOS Radio-Frequency Integrated Circuits*. Cambridge University Press, Cambridge, UK, 1998
- [4.6] P. R. Gray, R.G. Meyer, P. J. Hurst and S. H. Lewis, *Analysis and Design of Analog Integrated Circuits*, Fourth Edition, Wiley, New York, 2001.
- [4.7] J. Janssens and M. Steyaert. *CMOS Cellular Receiver Front-Ends*. Kluwer, The Netherlands, 2002

# 5

## Broadband CMOS LNA Design

### 5.1 Introduction

As discussed in chapter 3, the proposed universal radio receiver needs a low-noise amplifier that is broadband; this means that it needs to have enough gain, acceptable noise figure, and good matching over the wide range of frequencies. In this chapter, the design of such an LNA will be discussed. Starting from topology reviews and selections, we will go through the design considerations covering from the components sizing through the practical implementation, and then circuit simulation results and layout will be provided at the end of this chapter.

### 5.2 Topology Selection

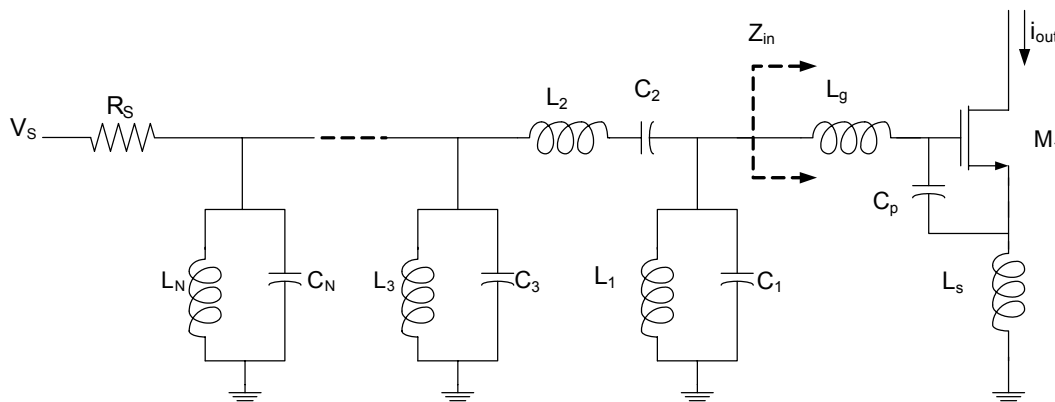
Most LNAs in the integrated wireless receivers are narrow-band and each of them is optimized for only one frequency band. Design methodology for these LNAs is straightforward and most of them are designed using the inductively degenerated topology, in which delivers both noise and power match at the same time [5.1]. In the universal radio receiver case, however, the design generally must be broadband as shown

in chapter 3. Fortunately, since the modes of operations are still narrow-bands, the linear-phase property is not required and results in less design constraints.

As can be seen in the previous chapter, there are few LNA topologies that are suitable for broadband operations. One of them is the common-gated topology using a source of the transistor with  $g_m=1/R_{in}$  as an input device. This method gives a good matching over a wide range of frequency but has a severe noise penalty. The better way is to use the modified version of the inductively degenerated LNA with broadband input matching. [5.2], [5.3]. This method, in theory, can achieve noise figure much lower than that of the other broadband matching topologies and still simple enough to be practically designed and implemented. The detail discussion of this topology will be discussed in the next sections.

### 5.3 Multi-Section Input Matching

The multi-section input matching topology is an extension of the inductive degeneration input matching topology discussed in the previous chapter. The generalized schematic of the broadband input matching topology is shown in figure 5.1 where N is the number of input stages.



**Figure 5.1** Generalized schematics of the multi-stage input matching topology

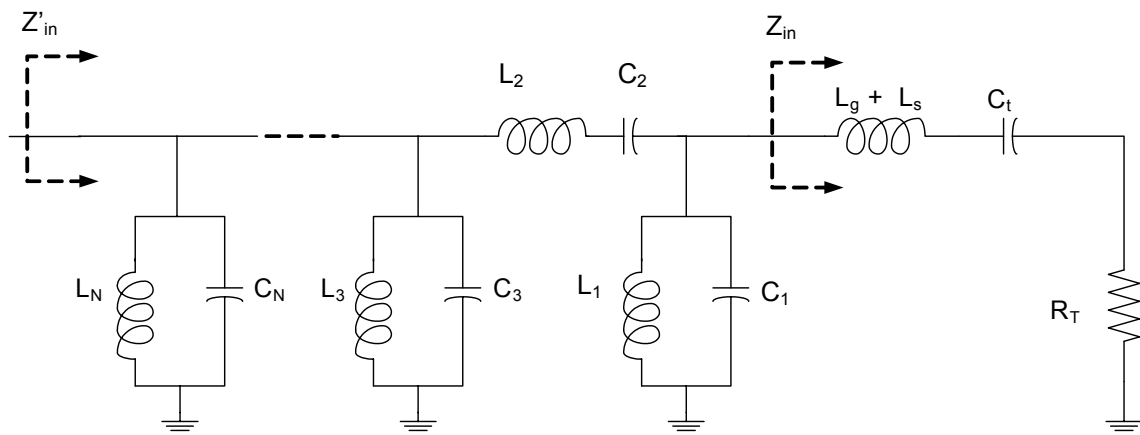
Please note that the external  $C_p$  is added between the gate and source of M1 in order to increase the degree freedom in the design. As shown in chapter 4 and ignoring the effect of  $C_{gd}$ , the input impedance of the LNA excluding  $L_n$ 's and  $C_n$ 's is given by:

$$Z_{in} = sL_g + \frac{1}{sC_t} + \frac{g_m L_s}{C_t} = sL_g + \frac{1}{sC_t} + R_T \quad (5.1)$$

Where

$$C_t = C_p + C_{gs} \quad (5.2)$$

Combining  $Z_{in}$  with  $L_n$ 's and  $C_n$ 's, we get the equivalent circuit for the input impedance as shown in Fig. 5.2. The impedance  $Z_{in}$  and the entire  $L_n$ 's and  $C_n$ 's form a bandpass filter with the termination resistor  $R_T$  at the end. If we look at the inductive degeneration topology as a first-order filter, this  $L_n$ 's and  $C_n$ 's additions effectively increase the order of the filter beyond one order. As known from the filter theory [5.4], it is easier to get high bandwidth from a higher-order filter than from a lower-order filter given the comparable component values and quality factor. This makes wideband matching feasible from multi-stage input matching.



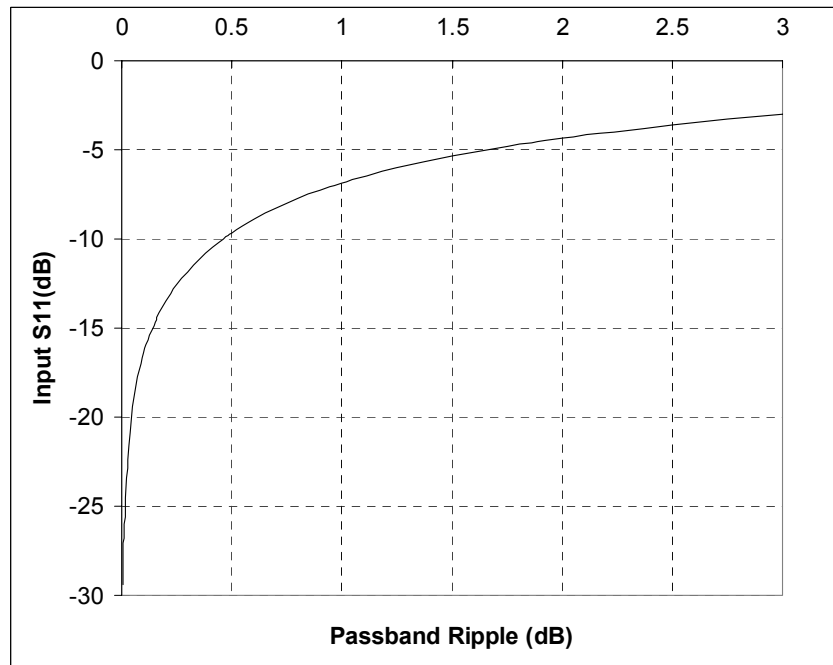
**Figure 5.2** Equivalent input impedance

### 5.3.1 Input Match

In order to get an input match, the real part of the input impedance ( $Z_{in}$ ) must be equal or close to the source impedance  $R_S$ . This means that we want  $R_T = \omega_T L_S = R_S$  at the termination. Given this condition, the passive of the filter must have 0dB gain (since it is passive) with a ripple  $\rho_r$ . The input reflection coefficient can be related to the ripple by:

$$|\Gamma_{in}|^2 = \left| 1 - \frac{1}{\rho_r^2} \right| \quad (5.2)$$

As a numerical example, we need to have  $0.953 \leq \rho_r \leq 1.054$  for input matching of -10dB or better. This translates to about less than  $\pm 0.46$  dB gain variation in the passband. The plot between passband ripple and the reflection coefficient, both in dB, is shown in figure 5.3.



**Figure 5.3** Relationship between passband ripple and  $S_{11}$

The reactive element values for any given bandwidth and matching specifications can be obtained by using well-established LC filter design methodology such as in [5.4] and [5.5]

### 5.3.2 Effective Transconductance

The effective  $g_m$  of this topology can be derived in the same way as in the section 4.5.1. It depends on the device  $g_m$  and the voltage transfer function from the input terminal to the  $v_{gs}$  at the device terminal. Assuming the transfer function of the filter is  $W(j\omega)$ , the current flowing into the gate of  $M_1$  is then given by [5.2]:

$$i_{M1,in} = \frac{v_{in}}{R_T} W(j\omega) \quad (5.3)$$

Where  $v_{in}$  is the terminal voltage as shown in figure 2. In the passband,  $W(j\omega)$  is approximately unity and the current is simply the terminal voltage divided by  $R_T$ . However,  $W(j\omega)$  becomes very small out-of-band and the current is minimal in this case. The  $v_{gs}$  of  $M_1$  can be found directly by multiplying the gate current to the impedance from  $C_{gs}$ :

$$v_{gs} = \frac{i_{M1,in}}{j\omega C_t} = \frac{v_{in}}{R_T} \frac{W(j\omega)}{j\omega C_t} \quad (5.4)$$

Using equation 5.4, the effective transconductance can be found as:

$$G_m(j\omega) = g_m \frac{v_{gs}}{v_{in}} = \frac{g_m W(j\omega)}{j\omega R_T C_t} \quad (5.5)$$

If only the magnitude of  $G_m$  is concerned, it can be simplified to:

$$|G_m(j\omega)| = g_m Q |W(j\omega)| \quad (5.6)$$

The expressions in equations 5.5 and 5.6 are the generalization of the equation 4.27 in the previous chapter. As shown above, the effective  $G_m$  of the circuit depends strongly on matching network  $Q$ . For on-chip implementation, this value is limited by either the practical values of the inductors or parasitic capacitances on the input transistor.

### 5.3.3 Noise Analysis

There are two main sources of noise in this matching topology. The first one is the loss at the input-matching network due to finite  $Q$  of the matching inductors. One important effect is that the series resistance of the inductor creates thermal noise at the input as well as reduces the passband gain. The other noise source is the input device  $M_1$  in figure 5.1. Its thermal drain and gate current noises are the major contributors to the overall device noise. The optimal device size based on given bias current for a narrow-band case is discussed in [5.1]. In the wideband matching case, the method to minimize in-band average noise figure is shown in [5.2].

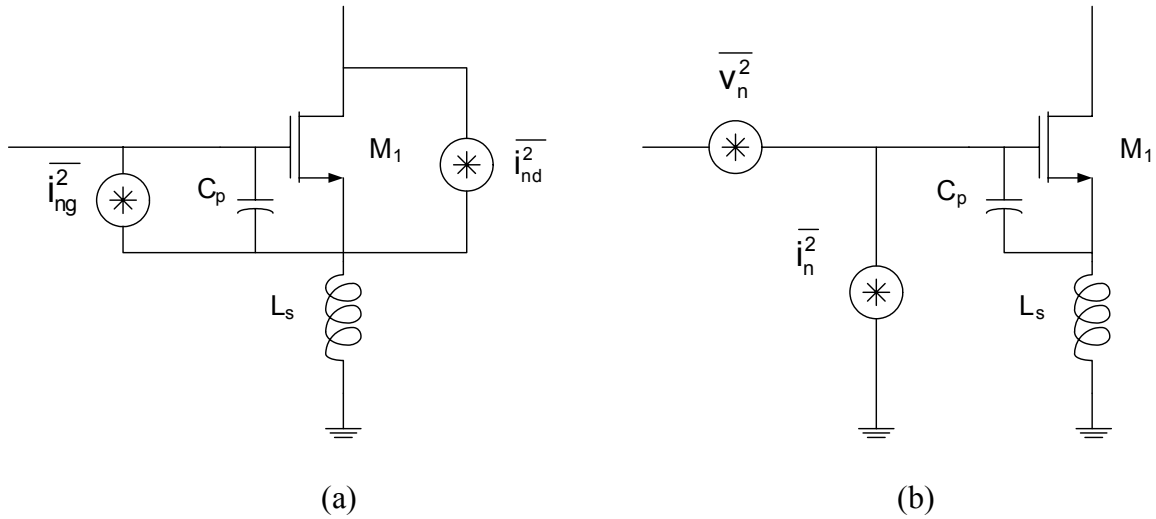
To see the effect of noise from the transistor, we will follow the analysis in [5.2]. The input transistor with the degeneration inductor is shown in figure 5.4a along with its

gate and drain current noises, the noises sources can be replaced by input referred voltage and current noise sources given by:

$$i_n = i_{ng} + \frac{j\omega C_t}{g_m} i_{nd} \quad (5.7)$$

$$v_n = j\omega L_s i_{ng} + (1 - \omega^2 C_t L_s) \frac{i_{nd}}{g_m} = \frac{i_{nd}}{g_m} + j\omega L_s i_n \quad (5.8)$$

Where  $i_{nd}$  and  $i_{ng}$  are the drain current noise and the gate current noise, respectively. The spectrum densities of these two current noises are discussed in the previous chapter and given again below:



**Figure 5.4** Drain and gate current noise models

$$\overline{i_{nd}^2} = 4kT\gamma g_{d0} \Delta f \quad (5.9)$$

$$\overline{i_{ng}^2} = 4kT\delta \frac{\omega^2 C_{gs}^2}{5g_{d0}} \Delta f \quad (5.10)$$

These two noises are correlated with the correlation coefficient of approximately j0.4. This makes the correlation admittance has only the imaginary part and is given by [5.2]:

$$Y_c = \frac{i_n}{v_n} = G_c + jB_c = jB_c = \frac{j\omega C_t}{\frac{1 + |c|\rho\alpha\chi}{1 + 2|c|\rho\alpha\chi + \rho^2\alpha^2\chi^2} - \omega^2 L_s C_t} \quad (5.11)$$

Where  $\rho = C_{gs}/C_t$ ,  $\chi = \sqrt{\delta/(5\gamma)}$  and c is the correlation coefficient between  $i_{ng}$  and  $i_{nd}$ . The parameter  $\alpha = g_m/g_{d0}$  accounts for short-channel effects due to velocity saturation and mobility decreases [5.1], [5.5].

The optimal source admittance is then given by [5.2]:

$$G_{opt} = \sqrt{\frac{G_u}{R_n} + G_c^2} = \sqrt{\frac{G_u}{R_n}} = \frac{\omega C_t (1 + 2|c|\rho\alpha\chi + \rho^2\alpha^2\chi^2)}{\rho\alpha\chi\sqrt{1 - |c|^2}} \quad (5.12)$$

$$B_{opt} = -B_c = \frac{\omega C_t}{\omega^2 L_s C_t - \frac{1 + |c|\rho\alpha\chi}{1 + 2|c|\rho\alpha\chi + \rho^2\alpha^2\chi^2}} \quad (5.13)$$

Where  $G_u$  and  $R_n$  are defined as in equation (4.11) and (4.12). Equation 5.13 shows that the optimal admittance (or impedance) is approximately the one that resonate the series combination of  $C_t$  and  $L_s$ . This means that nearly minimum noise figure can be obtained over the wide bandwidth by using the multi-section matching network and the corresponding noise factor is given by:

$$F \approx 1 + \frac{1}{G_u R_s} + \frac{R_s}{R_n} = 1 + \frac{P(\omega)}{g_m R_s} \frac{\gamma}{\alpha} \quad (5.14)$$

Where

$$P(\omega) = \frac{\rho^2 \alpha^2 \chi^2 (1 - |c|^2)}{1 + 2|c| \rho \alpha \chi + \rho^2 \alpha^2 \chi^2} + \omega^2 C_t^2 R_s^2 (1 + 2|c| \rho \alpha \chi + \rho^2 \alpha^2 \chi^2) \quad (5.15)$$

As seen from equation (5.14) and (5.15), the noise figure depends on frequency, device  $g_m$ ,  $C_t$ , and other process parameters. For any given bias current, there is an optimal device size to obtain the minimum noise figure for single frequency.

As mentioned previously, there are other sources of noise such as loss at the input matching network. These all noise sources must be considered altogether when designing the circuit. The total noise figure is then expected to be worse than what is given in the equation (5.14)

## 5.4 0.8-2.4 GHz Broadband LNA Design

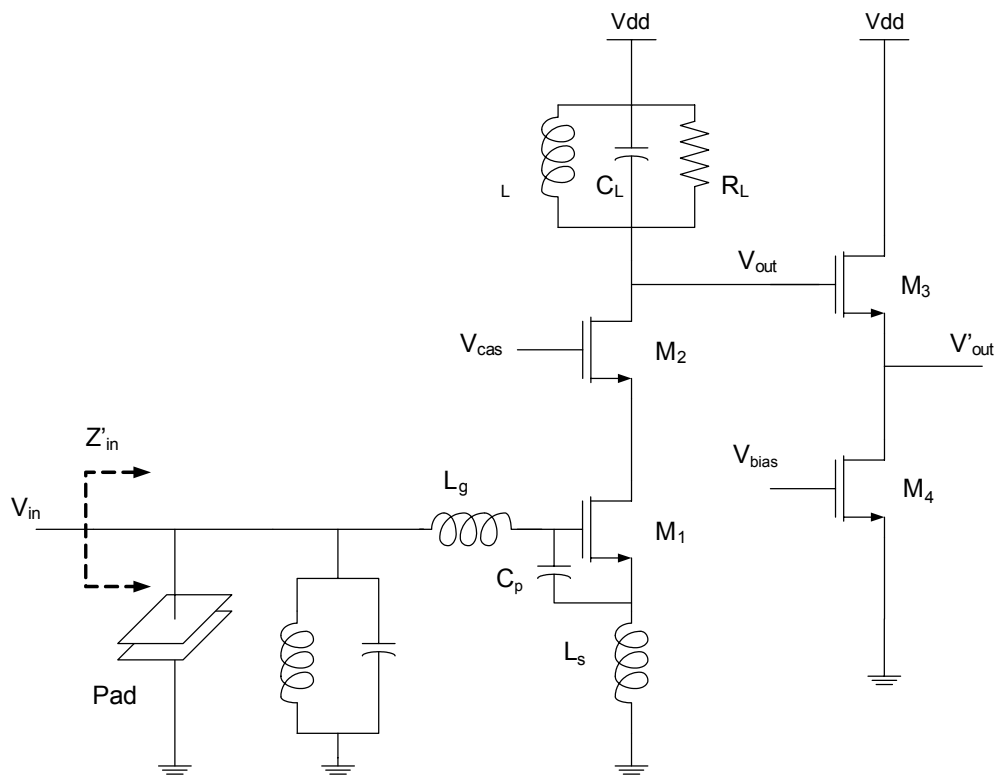
Having discussed on the matching topology, now we turns our interests to the LNA circuit implementation. The simplified schematic of the LNA is shown in the Fig. 5.5. It consists of the main (first) stage and the buffer (second) stage for output matching purpose. Please note that the second stage is added for measurement purposes only and can be eliminated when integrating the LNA with the mixer.

### 5.4.1 First Stage Design

The first stage employs the multi-section input matching in order to obtain both noise and power match at the input of the amplifier. Although we can get more

bandwidth by using more sections for the matching, inductors added in the signal path degrades the noise performance significantly due to its lossy property. As a result, the minimal number of stages is preferred as long as the required bandwidth can be achieved with reasonable passive component values. In this case, only two stages are enough given that the inductor values are still below 10nH.

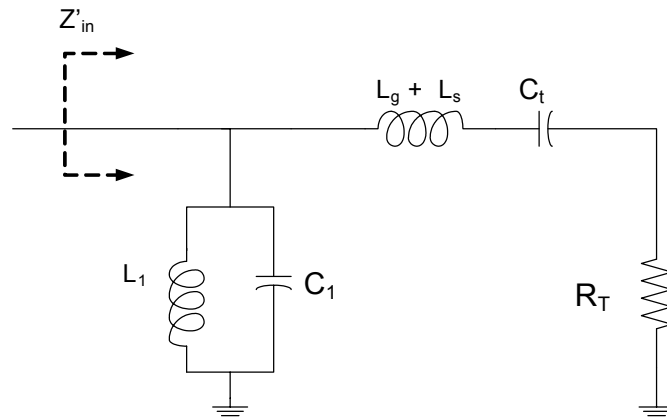
The output of the first stage is a low-Q tuned circuit with the center frequency of around midband. Using tuned load reduces out-of-band interferences and noise, while its low-Q property ensures broadband operation. The reason for not using the shunt-peaking topology is bias headroom issues. Since the bias current is high in our design (up to 16mA) and frequency can be as low as 0.8GHz, shunt-peaking would require either very high inductor value or very high resistor value at the load, which is undesirable.



**Figure 5.5** Broadband LNA topology using 2-section input matching

The design process begins with proper sizing of  $M_1$ ,  $L_s$ ,  $C_p$  as well as other input matching components. The size of  $M_1$  is affected by two factors: noise figure and gain. For any given bias current, the bigger  $W/L$  ratio means less noise and higher gain due to higher  $g_m$  up to a certain level where the increases in  $g_m$  can not offset the noises from increasing  $C_{gs}$ . This optimal point usually results in high device width and very low  $V_{dsat} = V_{gs} - V_{th}$ , in which results in and low linearity. In addition, although not related to this case since the design is single-ended, having low  $V_{dsat}$  usually results in poor device matching due to  $V_{th}$  variation [5.5]. In practice, since the noise figure is not very sensitive to the device size near the optimal point [5.1], it is preferable to make  $M_1$  to be as big as possible while maintaining a reasonable value of  $V_{dsat}$ . From the simulations, we have reached reasonable gain and noise with  $W/L = 480/0.18$  and 16mA bias current. This gives us a  $V_{dast}$  of around 120mV and  $g_m$  of around 140mA/V.

Combining  $Z_{in}$  with  $L_1$  and  $C_1$ , we get the equivalent circuit for the input impedance as shown in Fig. 5.6:



**Figure 5.6** Equivalent circuit for input impedance

The next step is to find the passive component values in order to get the broadband –10dB matching. The component values for the filter topology as in figure 5.6 can be obtained from standard filter synthesis [5.5] and shown below for Butterworth and Chebyshev prototype. Note that the bandwidth is from 0.8GHz to 2.4GHz with the center frequency of  $\sqrt{(0.8\text{GHz})(2.4\text{GHz})} \approx 1.4\text{GHz}$ . The passband ripple and cutoff frequency, as discussed before, is 0.46 dB.

**Table 2** Component values based on Chebyshev and Butterworth prototypes

Filter Type	$L_1$	$C_1$	$L_g + L_s$	$C_t$	$R_T$
Chebyshev	7.78 nH	1.69 pF	4.24 nH	3.11 pF	26 $\Omega$
Butterworth	8.24 nH	1.60 pF	4.00 nH	3.30 pF	50 $\Omega$

From the table, there are some differences in component values for  $L_g$ ,  $C_{gs}$ , and  $R_T$  for different prototypes. The Chebyshev topology has been chosen as the design starting point since it provides steeper transition band edges. Note that the termination resistance obtained from the Chebyshev prototype is not exactly 50 $\Omega$ , but is however around 26 $\Omega$ .

In practice, parasitic capacitance of  $L_1$ ,  $L_g$ , and the input pads increase the effective value of  $C_1$ . Series parasitic capacitances also reduce the effective values of  $L_1$  and  $L_2$ . As a result, we need higher values of  $L_1$  and  $L_2$  and lower value of  $C_1$ . In addition,  $C_{gd}$  of  $M_1$  increases the effective value of  $C_{gs}$  (Fig. 5.6) and reduces the required value of  $C_g$  (Fig. 5.5). After simulations, the final numbers for the components are:  $L_s=1.31\text{nH}$ ,  $L_1= 9.6\text{nH}$ ,  $C_1= 400\text{fF}$  (there is about 1pF of parasitic capacitances added to this number),

$L_g = 5.52\text{nH}$ , and  $C_g = 850\text{fF}$ . As will be shown later, the final simulated matching response deviates from the expected Chebyshev response in some extent but still provides -10 dB wideband matching over the desired bandwidth.

The cascode device ( $M_2$ ) is chosen to be as small as possible to reduce the parasitic capacitances. The voltage headroom as well as its noise contribution set the lower bound of the size. The chosen size is  $W/L = 120/0.18$ , exactly  $\frac{1}{4}$  in size comparing to  $M_1$ .

The output of the first stage is chosen to be a low-Q tuned circuit. Although, shunt-peaking technique is simpler and provides more bandwidth, it requires a moderate value of the series resistance resulted in reduction of the voltage headroom by a large factor. In fact, this problem is much more relaxed when the operating frequency is pushed higher as in [5.2] when a small value of series resistance is enough to keep the zero at the lower band-edge. The load is low-Q tuned in order to suppress out-of-band interference as well as to reduce the gain variations within the operating frequencies. The value of  $R_L$  is chosen to be  $300\Omega$  and the  $-3\text{dB}$  gain frequency band is ranging from  $800\text{MHz}$  and  $2.4\text{GHz}$ .

#### 5.4.2 Second Stage Design

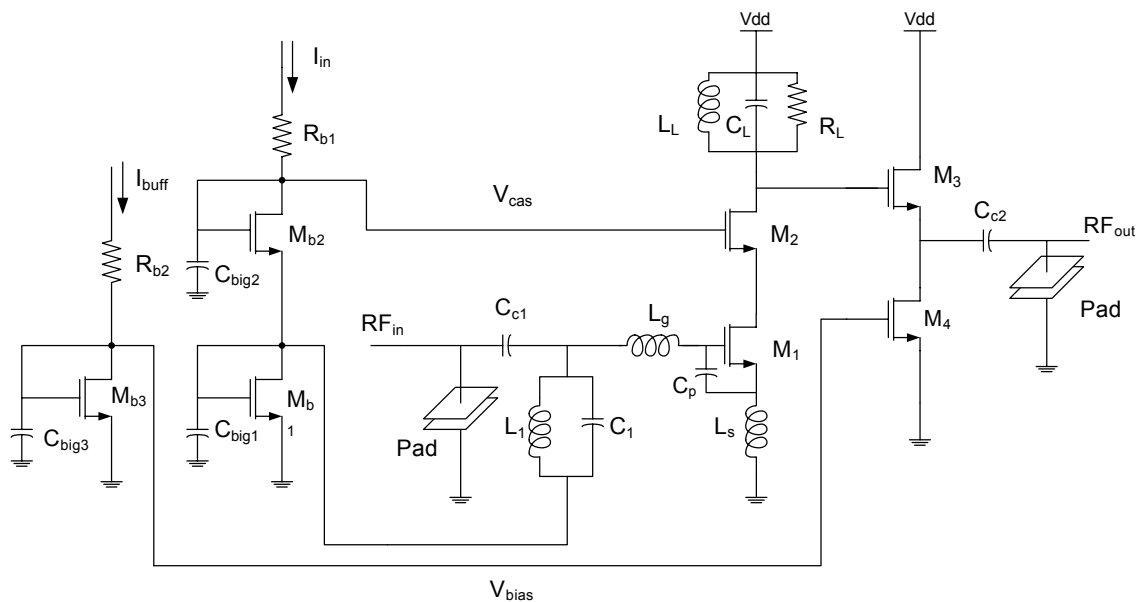
The second stage is a simple source follower added for the output matching purpose. The output impedance of this stage is  $1/g_m$  and has been set to  $50\Omega$ , which is the external load impedance during measurement. The voltage gain as this stage can be calculated as:

$$\frac{V'_{out}}{V_{out}} = \frac{g_m R_L}{1 + g_m R_L} = \frac{1}{1 + 1} = 0.5 \quad (5.16)$$

The measured output voltage ( $V'_{out}$ ) is 6dB less than the output voltage from the core amplifier ( $V_{out}$ ). When designing an LNA with a mixer,  $V_{out}$  is the output voltage that drives the mixer input. The device  $M_3$  is designed with minimum channel length in order to minimize the parasitic capacitances associate with it. The current source, however, has been design with higher channel length in order to make the current less sensitive to the output voltage. The bias current of this stage is set 10mA.

### 5.4.3 Biasing Circuits and Full Schematic

Full schematic for the LNA is shown in the figure 5.7 below. The biasing circuits are simple current mirrors for both the first and the second stages. Currents in both bias networks are externally controlled for measurement purposes. The bias voltage for the cascode device in the first stage is mirrored from the diode connected cascode device in the bias net work as well. The inputs and output signals are both Ac coupled though  $C_{c1}$  and  $C_{c2}$ .

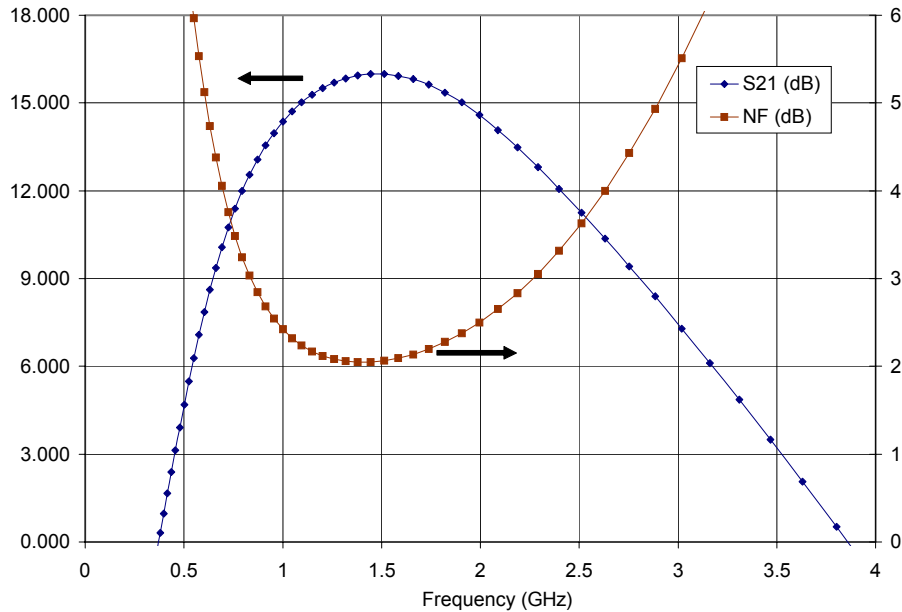


**Figure 5.7** Full schematics including the bias circuitry

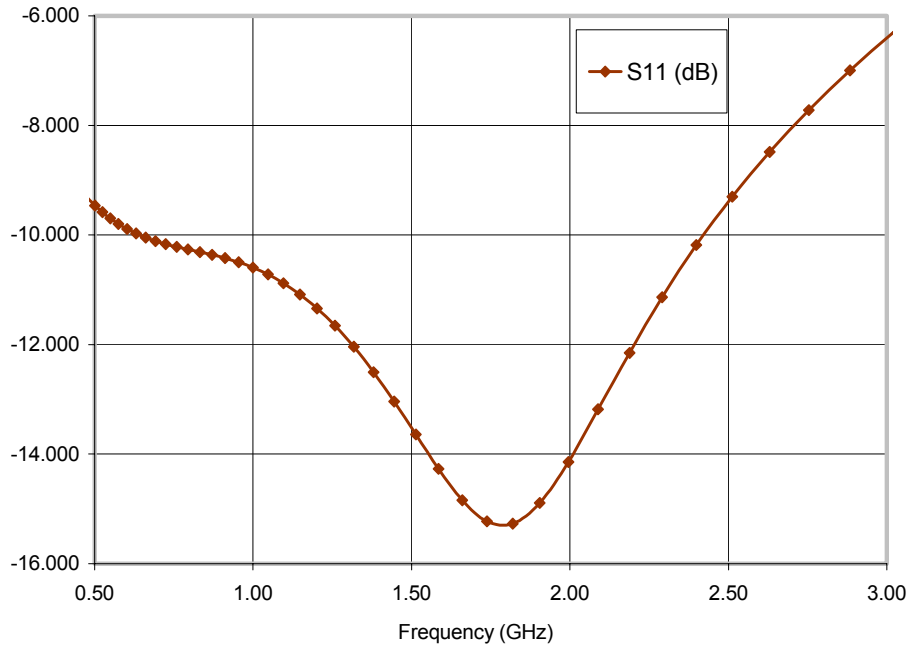
## 5.5 Simulation Results

All the simulations have been done with  $50\Omega$  termination system. The simulation plots of the LNA are shown in the Fig.5.8a-c. At 16mA bias current, the LNA has the  $S_{11}$  below  $-10\text{dB}$ , NF below  $3.5\text{dB}$ , and  $S_{21}$  above  $10\text{ dB}$  for the frequency range from 0.8-2.4 GHz. Note that the 6dB gain attenuation from the output buffer is already included. As a result, the real gain should be higher in practical on-chip design, when there is likely no output buffer.

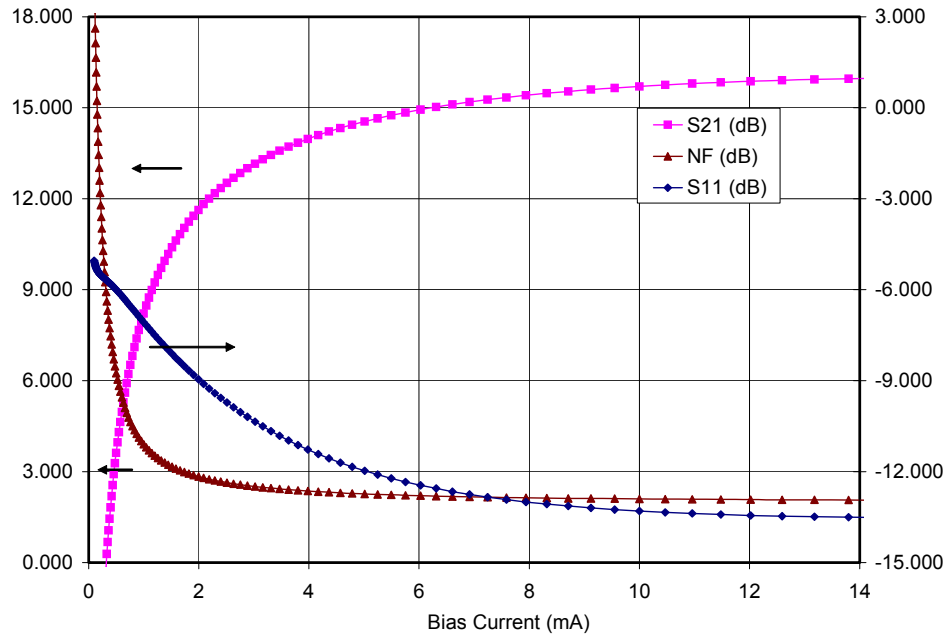
In addition, the LNA parameters ( $S_{11}$ ,  $S_{22}$ , NF, and Gain) are plots against the bias current at 1.5GHz. According to the plots, we can reduce bias current to as low as 2mA while maintaining an acceptable performance and good matching.



**Figure 5.8a** NF and S21 plots versus frequency



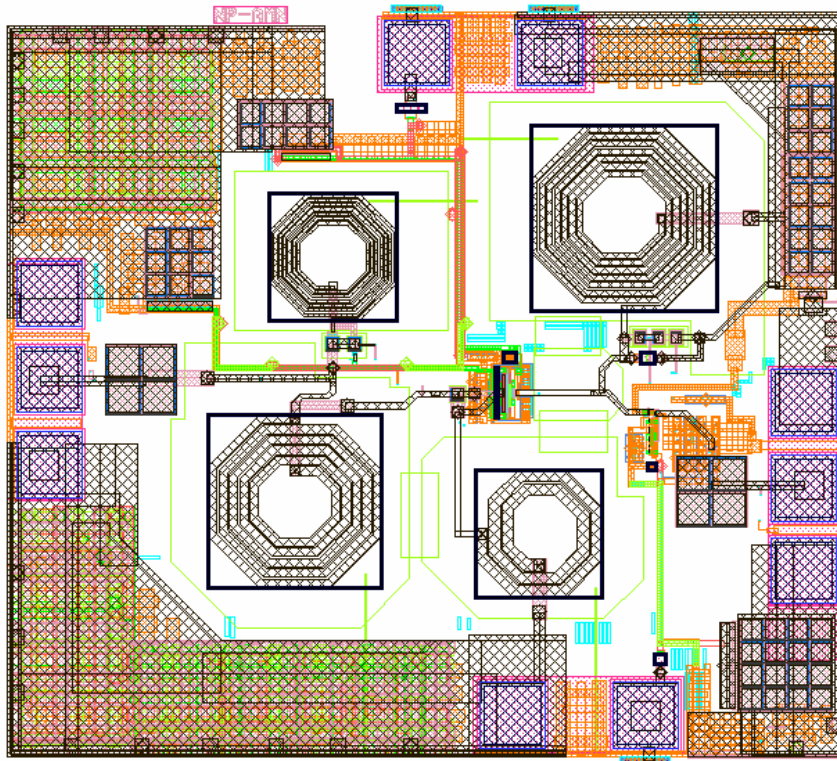
**Figure 5.8b**  $S_{11}$  plot versus frequency



**Figure 5.8c** NF,  $S_{21}$ , and  $S_{11}$  plots versus bias current

## 5.6 Layout

The circuit has been designed for fabrication in the IBM 0.18 $\mu\text{m}$  technology. The layout is shown in Fig. 5.9 below and the total chip area is approximately 1.9mm<sup>2</sup> (1.3mm x 1.5mm). Looking into the picture, the input is on the left and the output is on the right with AC coupled for both. Inductors are placed as far from each other as possible in order to reduce parasitic mutual coupling. In addition, the bias lines are shielded with ground lines and routed in the way that the distances from them to inductors are minimized.



**Figure 5.9** Layout of the LNA

## 5.7 References

- [5.1] T. H. Lee. *The design of CMOS Radio-Frequency Integrated Circuits*. Cambridge University Press, 1998
- [5.2] A. Bevilacqua and A. M. Niknejad, “*An Ultra Wideband CMOS Low Noise Amplifier for 3.1-10.6 GHz Wireless Receivers*”, IEEE J. Solid-State Circuits, vol. 39, no. 12, pp. 2259-2268, December 2004.
- [5.3] A. Ismail and A. Adibi, “*A 3-10-GHz Low Noise Amplifier with Wideband LC-Ladder Matching Network*”, IEEE J. Solid-State Circuits, vol. 39, no. 12, pp. 2269-2277, December 2004.
- [5.4] R. Schaumann and M. E. V. Valkenburg. *Design of Analog Filters*. Oxford University Press, New York, 2001
- [5.5] G. Matthaei, L. Young, and E. M. T. Jones. *Microwave Filters, Impedance-Matching Networks, and Coupling Structures*. McGrall-Hill, New York, 1964
- [5.5] P. R. Gray, R.G. Meyer, P. J. Hurst and S. H. Lewis, *Analysis and Design of Analog Integrated Circuits*, Fourth Edition, Wiley, New York, 2001.
- [5.5] B.E. Boser. *EE240 Lecture Notes*. University of California, Berkeley, 2003

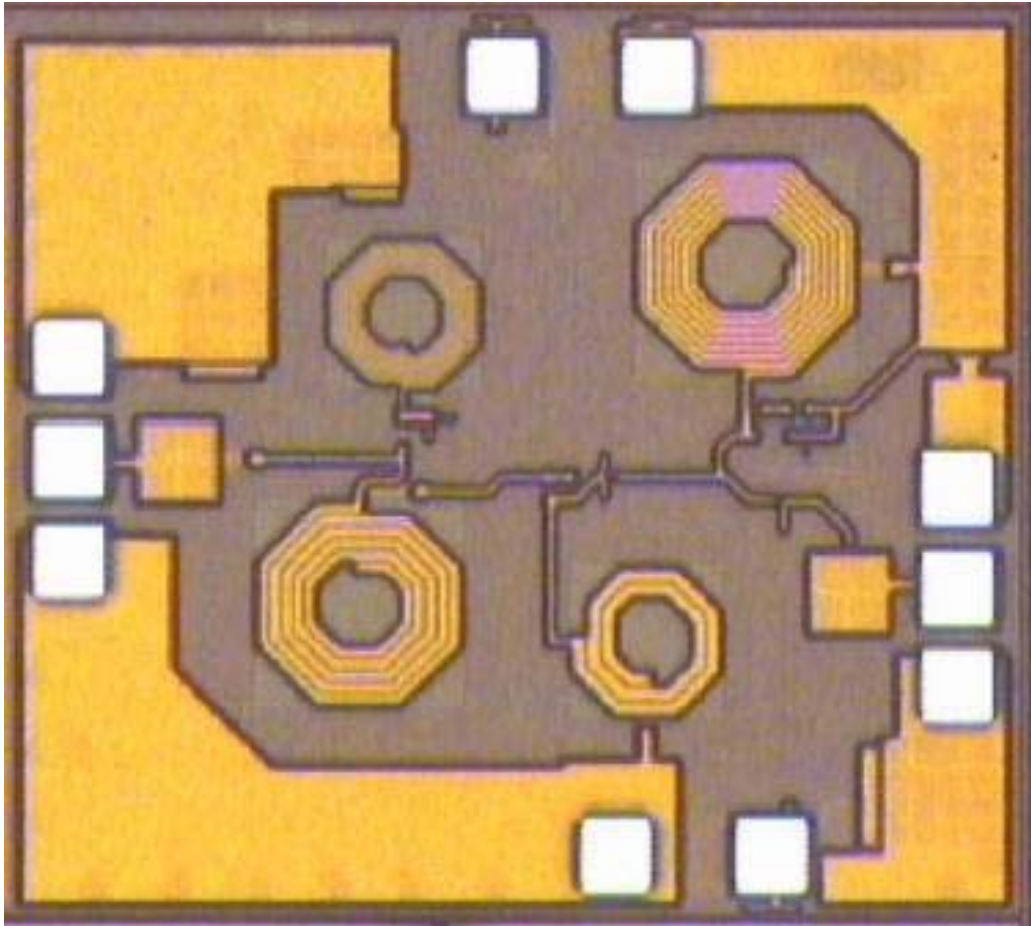
# Measurements and Conclusion

## 6.1 Introduction

As mentioned in the previous chapter, the LNA has been taped out in order to verify the functionality and performance. In this chapter, the measurement results of the taped out LNA will be presented. Starting from the die photo of the chip, we will then move to various types of measurement results including the all the S-parameters and noise figure. Then, the circuit performance as a function of the bias current will be presented. Finally, the conclusion and future research topics will be discussed.

## 6.2 Measurement Results

The LNA die photo is shown in the figure 6.1. The s-parameters, noise figure, and  $IIP_3$  of the LNA have been measured by using the probe station in Berkeley Wireless Research Center (BWRC). The measurements cover the frequency from 0.8GHz to 2.4GHz with different bias current. All the cable losses are compensated either by calibration (for s-parameters) or subtraction (for NF and  $IIP_3$  measurements). The results are shown on the next pages. Note that all the bias currents shown are not including the current from the buffer stage, which is 10mA.



**Figure 6.1** LNA Die Photo

### 6.2.1 $S_{11}$

$S_{11}$  plots at different bias currents are shown in figure 6.2a-e. From the pictures, it is clear that the -10dB matching is achieved over the wide range of frequencies and bias currents.

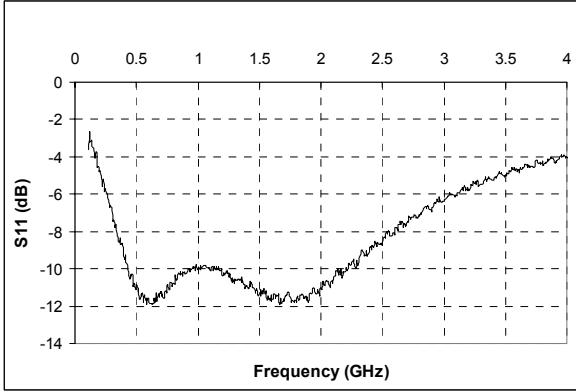


Figure 6.2a  $I_d=2\text{mA}$

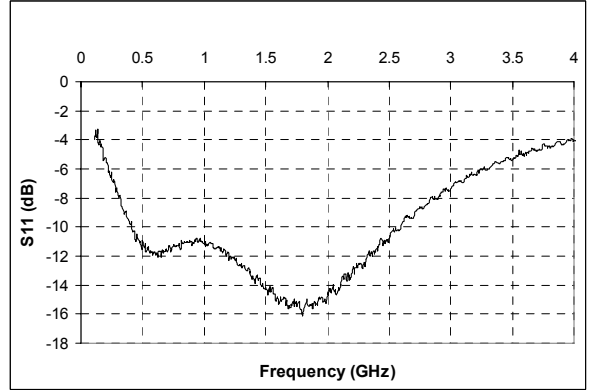


Figure 6.2c  $I_d=4\text{mA}$

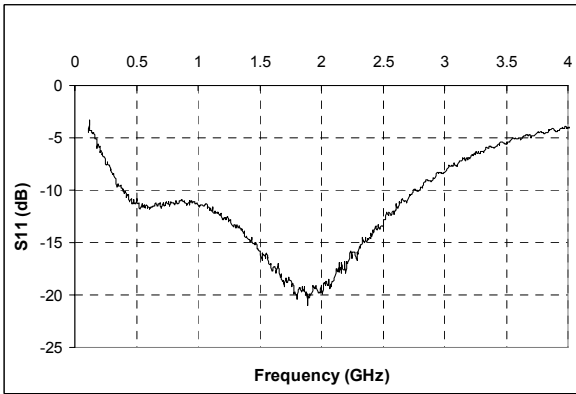


Figure 6.2b  $I_d=8\text{mA}$

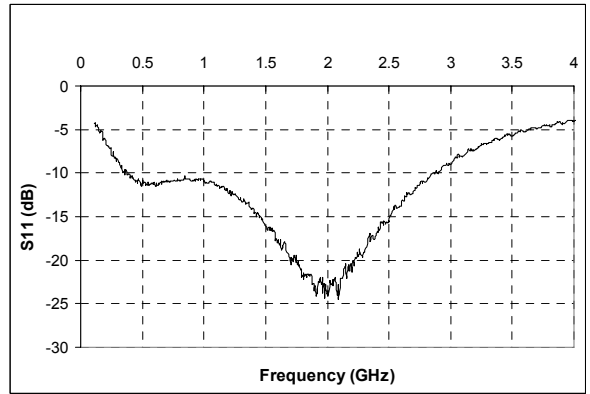


Figure 6.2d  $I_d=16\text{mA}$

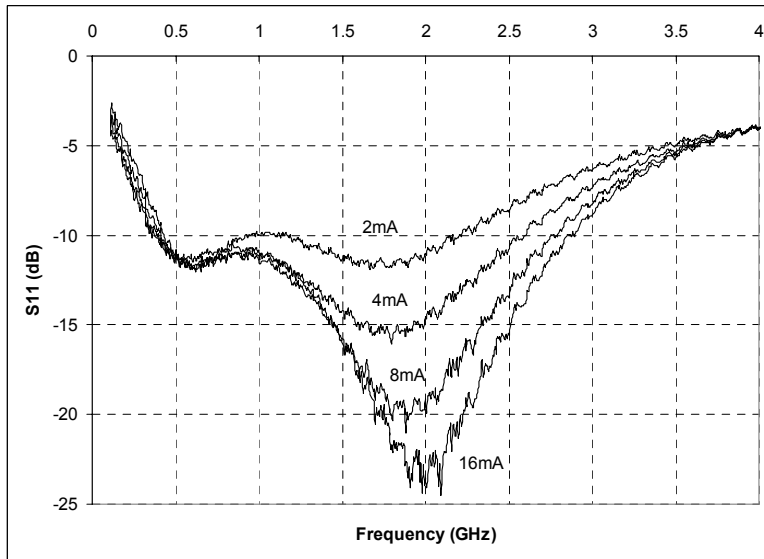
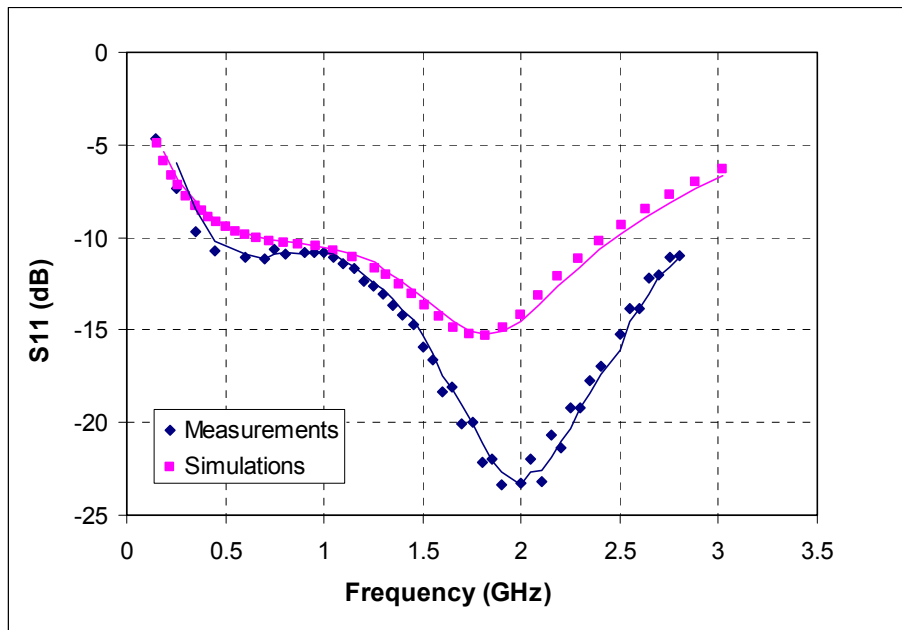


Figure 6.2e  $S_{11}$  comparisons from different bias currents

**Figure 6.2**  $S_{11}$  plots for different bias currents

As a comparison, the  $S_{11}$  plots from simulation and measurements are shown in the same graph for  $I_d=16\text{mA}$  in figure 6.3. As seen from the plots, the measurements actually yield better matching over the range of interests. In addition, they are off-tuned by a little even though the plots share the same trend. The source of discrepancies between these two curves is not well understood. However, since the matching is dominated by the passive element values at the input, it most likely comes from parasitic associated with the layout.



**Figure 6.3** Comparison between measure and simulations of  $S_{11}$  at 16mA

### 6.2.2 $S_{21}$

Like  $S_{11}$ ,  $S_{21}$  plots at different bias currents are shown in figure 6.4a-e. The peak gain is around 17dB at 1.5GHz with 16mA bias current. In this case, the -3dB bandwidth is approximately from 1GHz to 2GHz, although a sufficient gain is obtained from 0.8GHz to 2.4GHz. As the bias current changes from 2mA to 16mA,  $S_{21}$  changes by

approximately 5dB. This means we can trade off some sensitivity with bias current in dynamic operations. More discussion about this topic will be present in section 6.3.7.

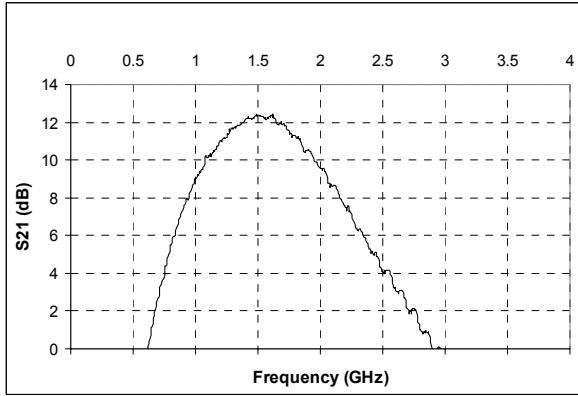


Figure 6.4a  $I_d=2\text{mA}$

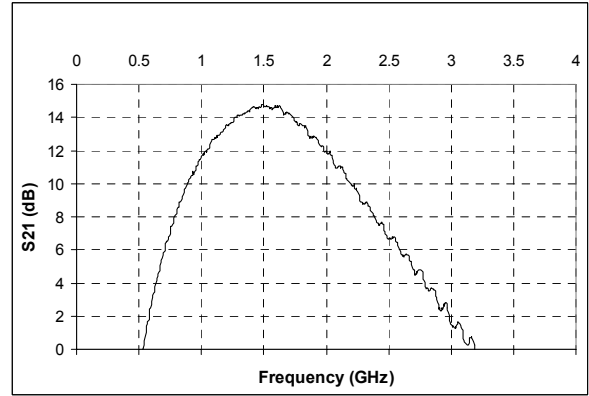


Figure 6.4b  $I_d=4\text{mA}$

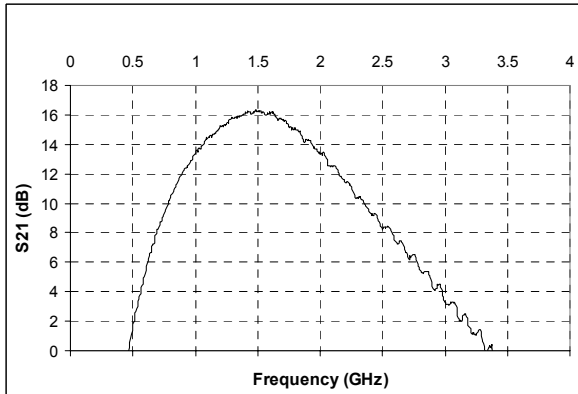


Figure 6.4c  $I_d=8\text{mA}$

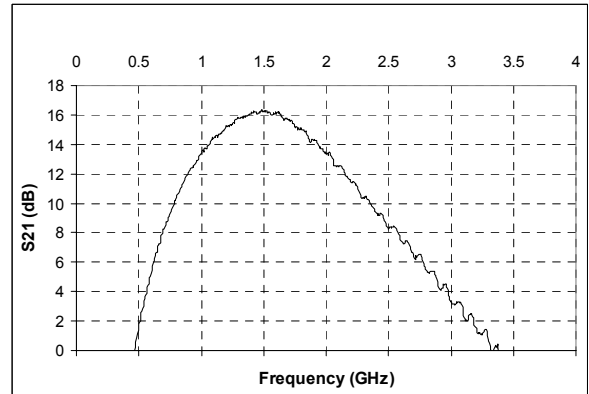


Figure 6.4d  $I_d=16\text{mA}$

**Figure 6.4**  $S_{21}$  plots for different bias currents

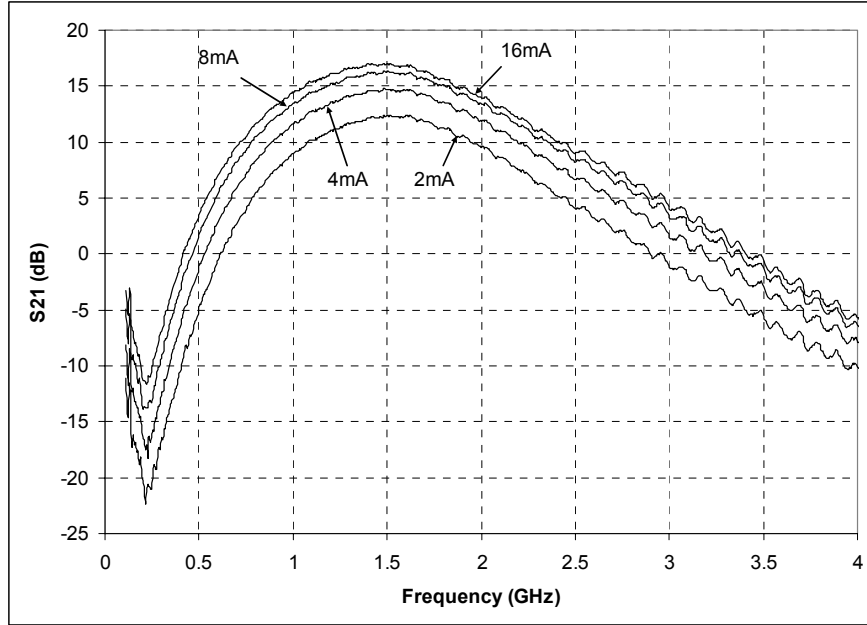
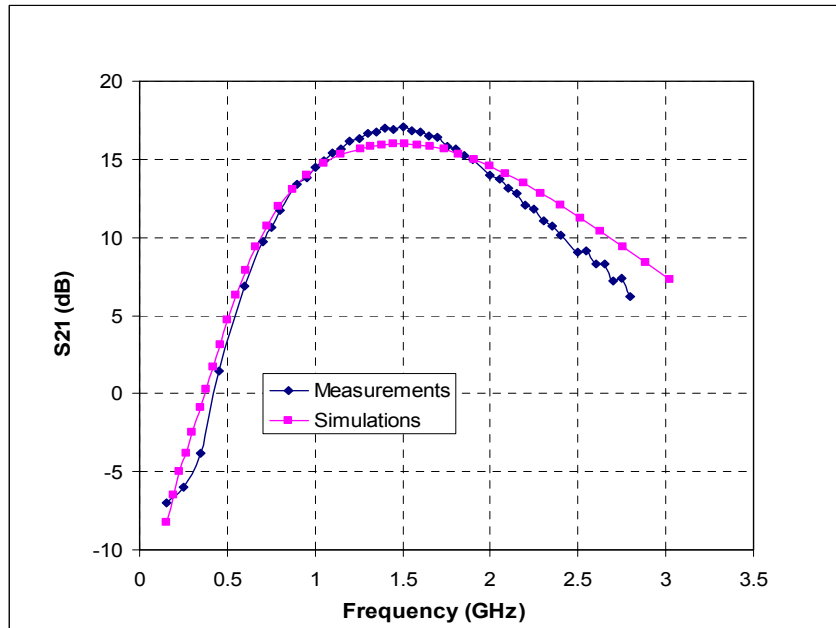


Figure 6.4e  $S_{21}$  comparisons from different bias currents

**Figure 6.4**  $S_{21}$  plots for different bias currents (continue)

In addition, the  $S_{21}$  plots from simulation and the measurement at 16mA bias current are plotted on the same graph in figure 6.5.



**Figure 6.5** Comparisons between measure and simulations of  $S_{21}$  at 16mA

### 6.2.3 $S_{12}$

$S_{12}$  has been measured and plotted at different bias currents are shown in figure 6.6a-d. From the measurements, the isolation from the buffer output to the amplifier input is roughly between 40dB to 50dB over the operating range. It does not depends on the bias current and only weakly depend on the frequency.

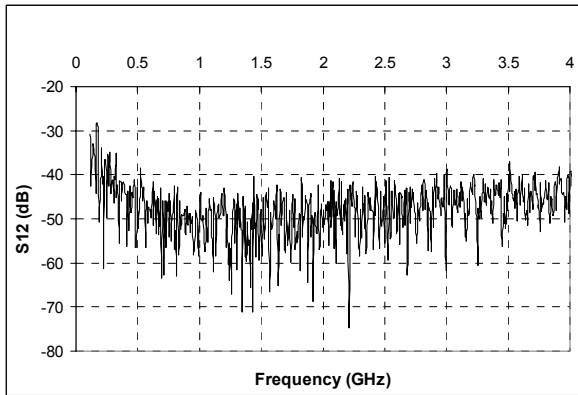


Figure 6.6a  $I_d=2\text{mA}$

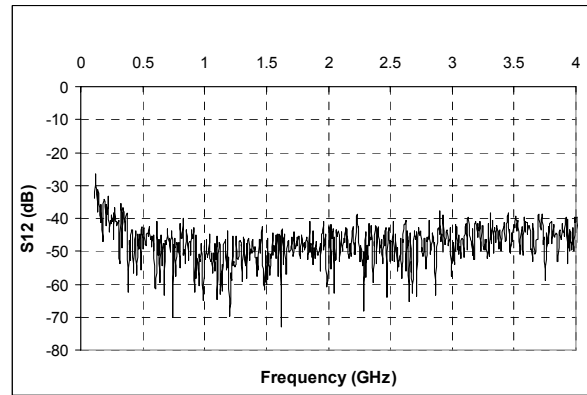


Figure 6.6c  $I_d=4\text{mA}$

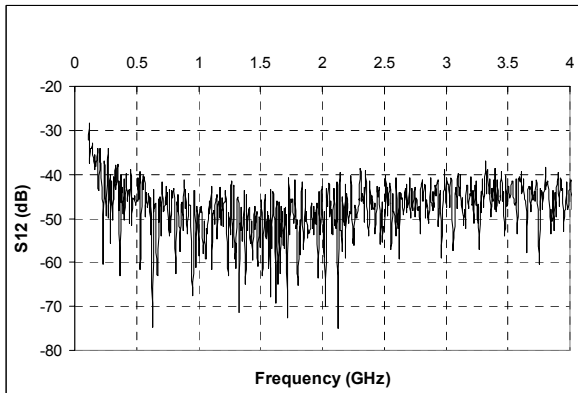


Figure 6.6b  $I_d=8\text{mA}$

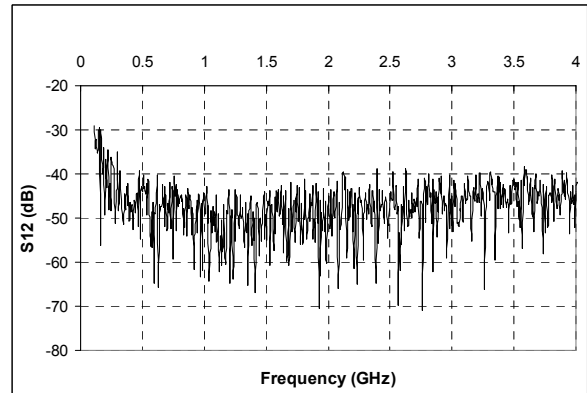


Figure 6.6d  $I_d=16\text{mA}$

**Figure 6.6**  $S_{12}$  plots for different bias currents

### 6.2.4 $S_{22}$

The output matching,  $S_{22}$ , is measured and the results are shown in figure 6.7a-d. Better than -10dB of matching is achieved over the frequency ranges and the main amplifier bias current. Please note that the buffer current is fixed to 10mA for all the measurements and this makes  $S_{22}$  almost independent to the main stage bias condition. According to the data, we can then assume that 6dB loss occurs at the buffer stage and the first-stage gain is higher than the overall gain by the same amount.

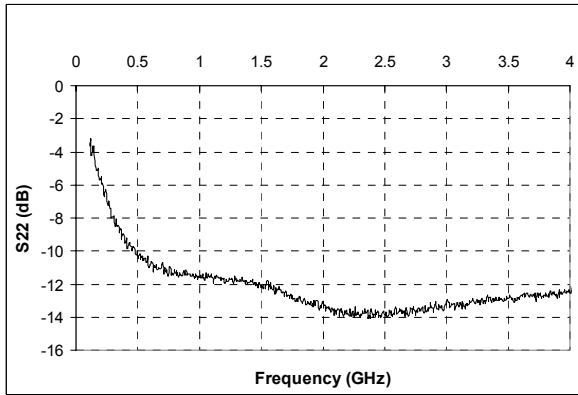


Figure 6.7a  $I_d=2\text{mA}$

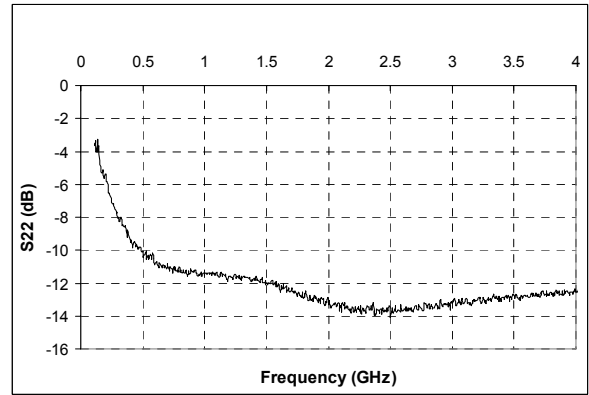


Figure 6.7c  $I_d=4\text{mA}$

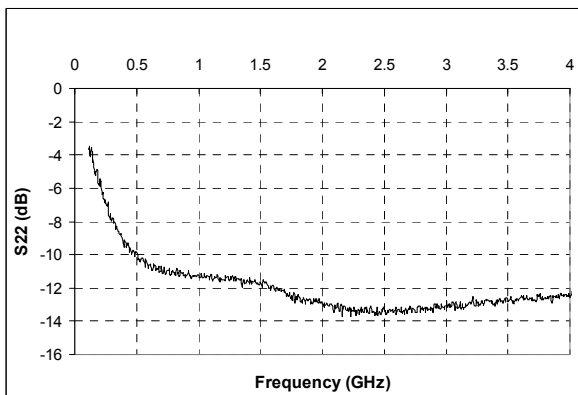


Figure 6.7b  $I_d=8\text{mA}$

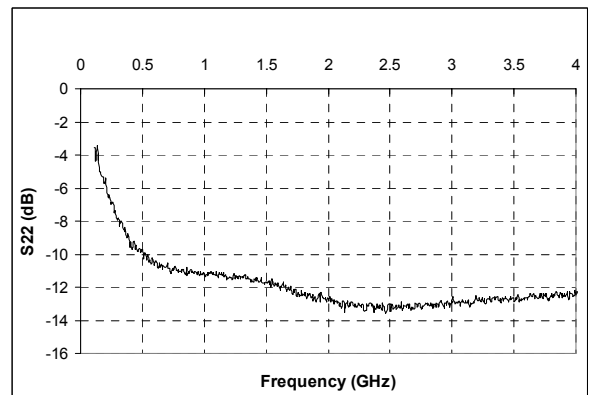
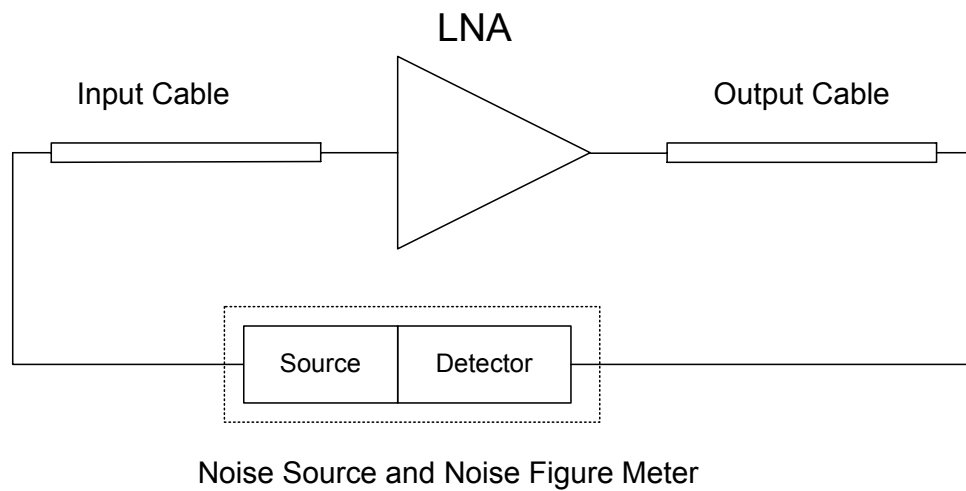


Figure 6.7d  $I_d=16\text{mA}$

Figure 6.6  $S_{22}$  plots for different bias currents

### 6.2.5 Noise Figure

The noise measurements have been done using a noise figure meter in conjunction with the probe station. Since the measurement cable is not perfect, the measured noise figure number must be subtracted by the input cable attenuation. The measurement setup and are shown in figure 6.8.



**Figure 6.8** Noise measurements setup

If the loss at the output is small, the LNA noise figure can be calculated as follow:

$$NF_{LNA}(dB) = NF_{measured}(dB) - L_{cable}(dB) \quad (6.1)$$

Where  $L_{cable}$  is the loss at the input cable. Using the set up and calculations above, the noise measurement results are shown in figure 6.9a-d. In addition, comparisons between the simulated and measured noise figures are shown in figure 6.10.

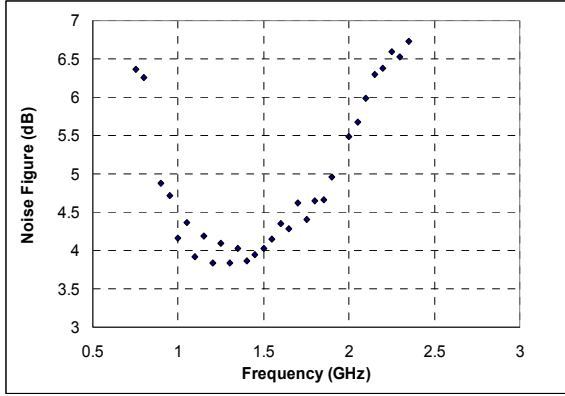


Figure 6.9a  $I_d=2\text{mA}$

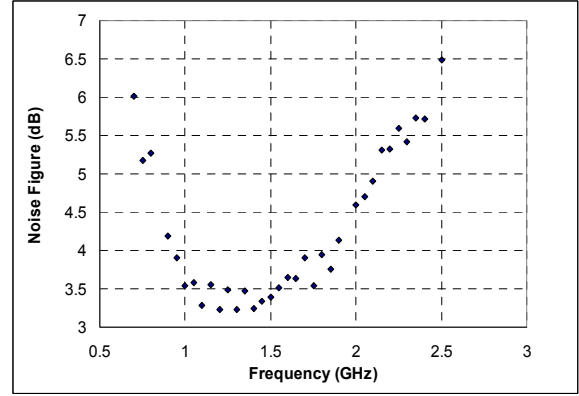


Figure 6.9b  $I_d=4\text{mA}$

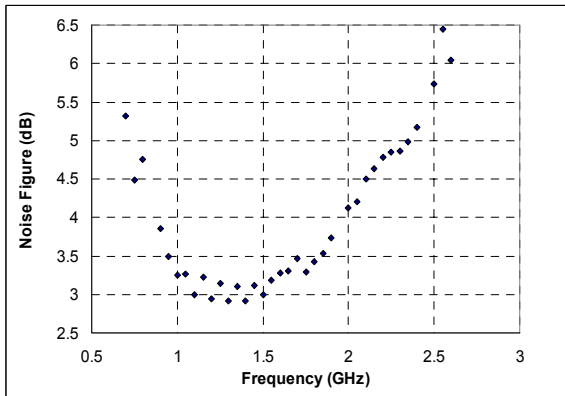


Figure 6.9c  $I_d=8\text{mA}$

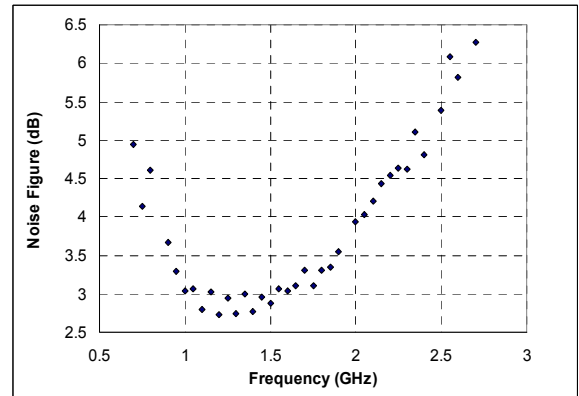
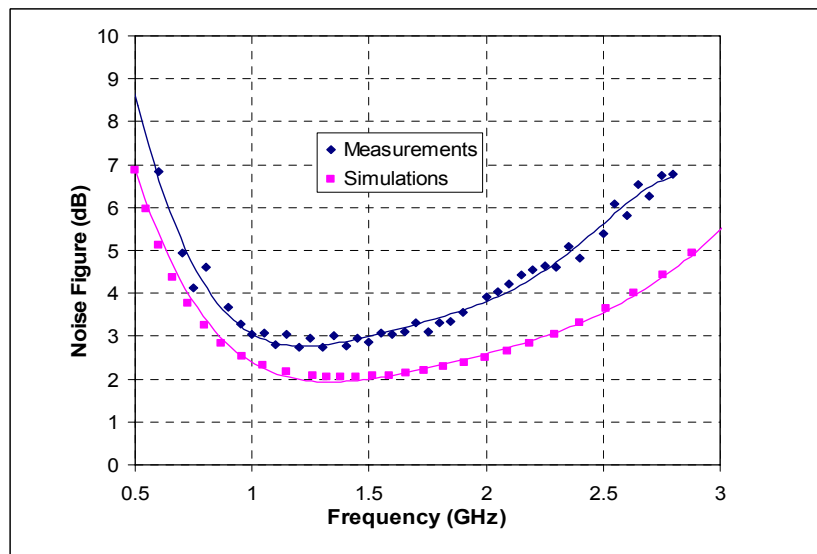


Figure 6.9d  $I_d=16\text{mA}$

**Figure 6.9** NF plots for different bias currents



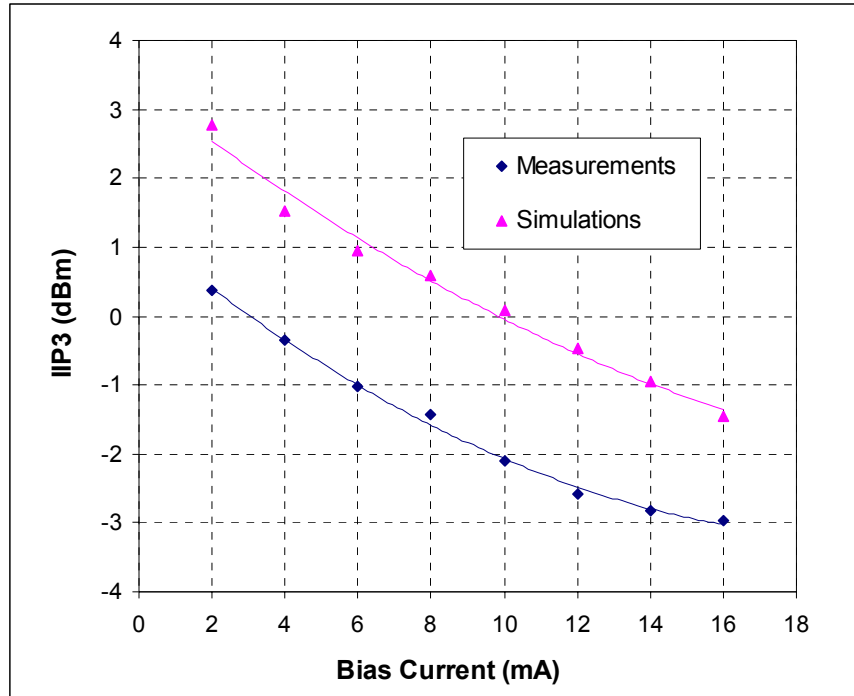
**Figure 6.10** Comparisons between measure and simulations of NF at 16mA

As shown in the plots, the minimum measured noise figure is approximately 2.7dB at around 1.2GHz and 16mA bias current. For the same bias condition, noise figure is below 4dB between 0.8GHz-2GHz and is around 5dB at 2.4GHz. The noise performance gets worse when the bias current decreases as expected. At 2mA bias, the minimum NF is around 4dB.

Comparing to the simulations, the measured noise figure is around 0.5dB-1dB higher than expected. Although the exact reason is unknown, this probably caused by the induced gate noise and NQS effect, which is not included in the device model. This can be fixed by manually adding the gate induced noise and NQS resistor into the model done in [6.1],

### **6.2.6 IIP<sub>3</sub>**

To test the linearity of the circuit, the input IP<sub>3</sub> of the LNA has been measured using the two-tone inputs method. The frequencies of the test signals are 1.5GHz and 1.501GHz, which are around the midband of the LNA. The measurements results are plotted against bias current in figure 6.11 for different bias currents. The measured IIP<sub>3</sub> values are between 0 to -3dBm for bias currents from 2mA to 16mA. In addition, the simulated IIP<sub>3</sub> numbers are shown on the same graph as a comparison.



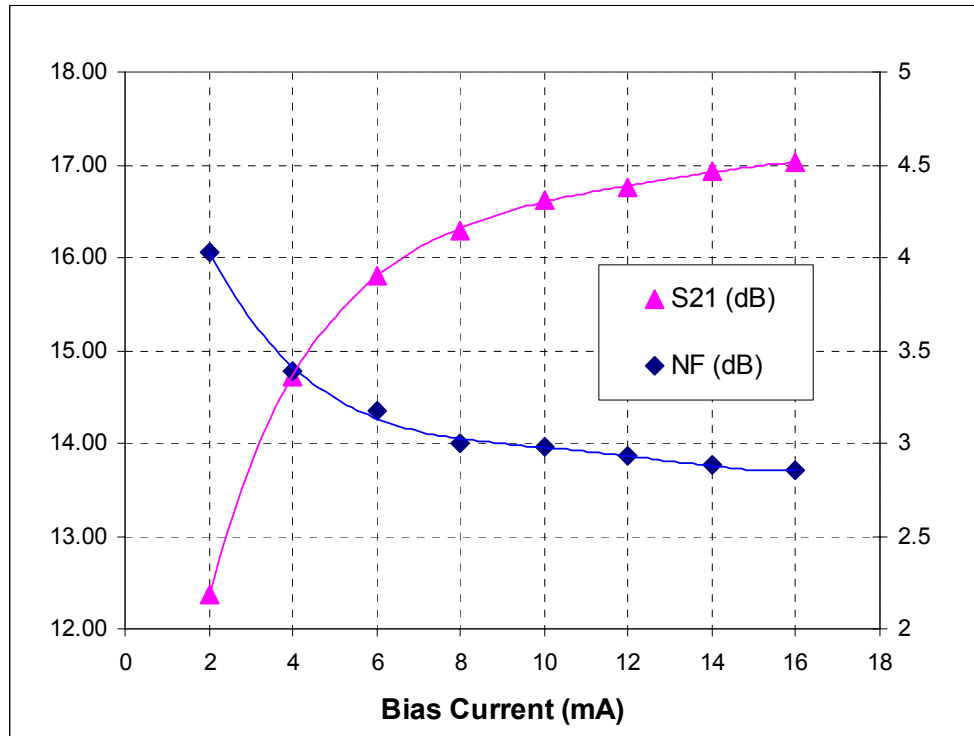
**Figure 6.11** LNA IIP<sub>3</sub> plots

As seen from the figure 6.11, the IIP<sub>3</sub> values obtained from the measurements are approximately 2dB lower than the numbers from the simulations. However, they both exhibit the same trend. One interesting point is that the IIP<sub>3</sub> decreases as bias current increases; this means that it is likely limited by the nonlinearity of the buffer stage. Since the IIP<sub>3</sub> of the buffer stage is fixed, the overall IIP<sub>3</sub> is inversely proportional to the gain at the first stage.

### 6.3.7 Dynamic Performance

One interesting aspect of the circuit is the dynamic operation of the LNA, or how the performance metrics changes with the bias current. As we can see from figure 6.2, the S<sub>11</sub> of the LNA stays below -10dB for the bias current from 2mA to 16mA in the band of

interests. This means that we can vary the bias current and adjust the performance without violating the matching requirement. The plots of LNA gain and NF as a function of bias current at 1.5 GHz is shown below in figure 6.12. From the plots, it is clear that we can nicely trade the performance with current consumption.



**Figure 6.12** LNA Dynamic Characteristics

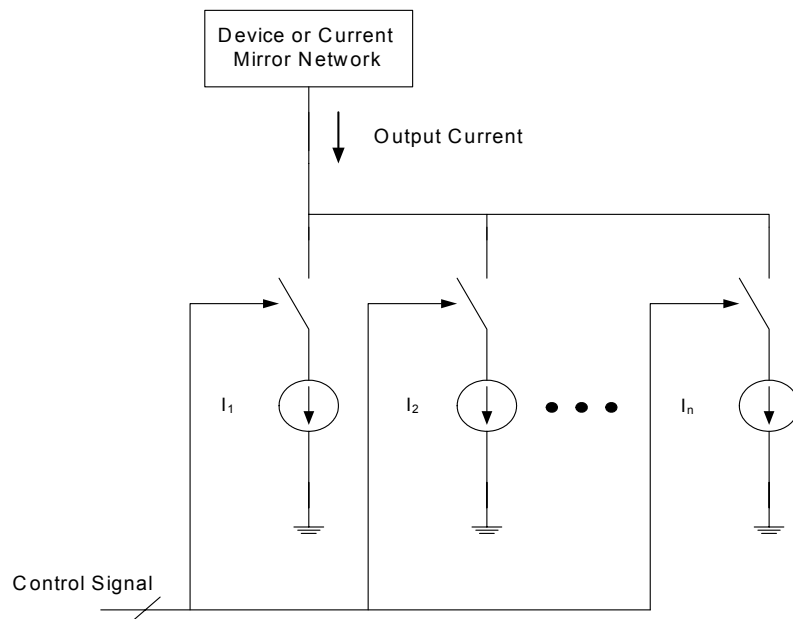
### 6.3 Conclusion and Future Research Topics

The broadband CMOS LNA has been designed, fabricated, and measured in IBM 0.18 $\mu$ m technology process. The LNA achieves -3dB bandwidth from 1 GHz to 2 GHz with 16mA bias current and 17 dB peak voltage gain. The noise figure is below 4dB for the same input frequency range and bias current with the minimum value of 2.7 dB

around 1.2 GHz. The LNA has -10dB or better input matching for an entire range of bandwidth even if the bias current is varied from 2mA to 16mA. As a result, it is suitable for dynamic broadband operation in multi-band multi-mode receivers.

We have found that there are some discrepancies between simulations and measurement results. One major problem is the noise modeling, since the gate noise is not accurately modeled in the transistor modeled, this results in as much as 1 dB underestimation of the noise figure. In addition, there are some frequency response mismatches that might be due to unexpected parasitic, causing narrower LNA bandwidth in the measurements. All of these problems can be solved by careful layout and parasitic calculations. In addition, the parasitic problems might be alleviated by adding more stages, in which will reduce the required passive component sizes and then make the layout more compact.

There are several future research topics that are worth looking into. One of them is to look for new ways of enhancing the linearity of the LNA in order to make it more compatible with universal receiver as mentioned in the chapter 3. In addition, more efficient and digital-compatible circuit implementation of the dynamic biasing schemes should be investigated. One way is to use multiple current sources that can be turned on and off by a digital controller as shown in Fig. 6.13. By using binary steps for the amount of currents, only three current sources would be required for eight step adjustments. Another interesting point to look at is the minimization or reduction of passive components. As shown in the chip layout, most of the area was taken by the inductors. If the inductors can be implemented in the way that does not take much area, or if a high effective inductance can be made, it would help reducing the chip cost significantly.



**Figure 6.13** Dynamic biasing schemes.

## 6.4 References

- [6.1] A. Bevilacqua and A. M. Niknejad, "An Ultra Wideband CMOS Low Noise Amplifier for 3.1-10.6 GHz Wireless Receivers", IEEE J. Solid-State Circuits, vol. 39, no. 12, pp. 2259-2268, December 2004.

