A 5.8 GHz Linear Power Amplifier in a Standard 90nm CMOS Process using a 1V Power Supply

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***Abstract*— A fully integrated 5.8 GHz Class AB linear power amplifier (PA) in a standard 90nm CMOS process using thin oxide transistors utilizes a novel on-chip transformer power combining network. The transformer combines the power of four push-pull stages with low insertion loss over the bandwidth of interest and is compatible with standard CMOS process without any additional analog or RF enhancements. With a 1 V power supply, the PA achieves 24.3dBm maximum output power at a peak drain efficiency of 27% and 20.5dBm output power at the 1 dB compression point.**

***Index Terms*— Power amplifiers, CMOS power amplifier, power combiners**

I. Introduction

The need for ubiquitous wireless communication systems during the past decade has been a key driver in the development of high frequency low cost integrated circuit building blocks. Though most of the radio frequency (RF) building blocks have been successfully integrated into CMOS process, the power amplifier is mostly implemented in a different process technology. A fully integrated CMOS solution would offer several benefits such as lower cost, less area and no need of individual tuning of the different building blocks. To achieve this integration the PA must use the same fabrication process and supply voltage level as the digital circuits and secondly the matching networks must be on chip. However, the low breakdown voltage and high knee voltage of transistors in 90 nm CMOS process, together with the low quality factor of on-chip passives pose a big challenge. Some researchers have recently demonstrated that CMOS technology becomes a viable option for building power amplifiers if power combining technique is used [1][2][4]. The principle is shown in Fig.1 where the secondary coils of N independent 1:1 transformers are connected in series. Therefore the ac voltages are added in the secondary, while the primaries can be driven with low voltages. The efficiency of such a circuit is given by

$$\eta_{max} = \frac{1}{1 + \frac{2}{Q_1 Q_2 k^2} + 2\sqrt{\frac{1}{Q_1 Q_2 k^2}(1 + \frac{1}{Q_1 Q_2 k^2})}} \tag{1}$$

necessitating a high coupling coefficient (k) and high quality factor windings (Q_1, Q_2), a non-trivial requirement in a standard CMOS process due to the lossy substrate and the lack of a second thick metal layer.

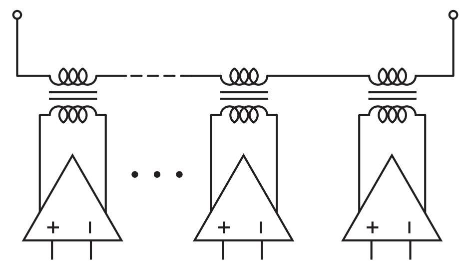

Fig. 1. Power combining network principle.

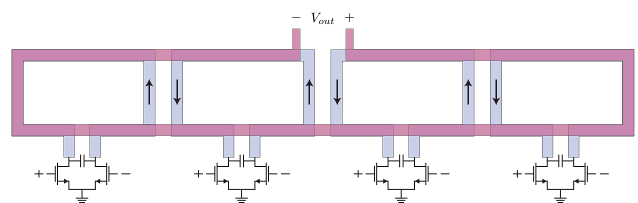

Fig. 2. A simple power combining transformer layout.

Transformer based power combiners have been demonstrated utilizing “slab” inductors to realize a distributed active transformer [1]. However the structure relies on creation of virtual grounds at the supply nodes, hence all the stages have to remain on preventing enhanced efficiency at power back-off [2]. In this work we propose a new transformer based power combiner. Each pair of windings are realized with ring based transformer structures that are simple to design and scale with frequency. Since each stage is DC isolated, each amplifier runs on a low supply voltage, allowing low breakdown transistors to be employed. An additional benefit of the ring based structure is simple power control. Since each stage operates independently, we can turn off amplifier stages to back-off power without dramatically altering the efficiency of the power combiner [2].

II. Transformer Power Combiner

In Fig.2 a simple power combining with rectangular loop based transformer structures is shown. But, it is easily seen that in a simple transformer layout, the adjacent windings have currents in opposite direction, and thus do not contribute much flux and coupling to the secondary. To minimize this internal flux cancellation the space between the adjacent windings can be increased. At the expense of area, this is an effective approach and an efficient dual layer approach has been demonstrated in [2]. However [2] uses special RF process options with two thick metal layers. With a single thick metal layer, as is commonly the case in digital CMOS process, a lateral structure is better suited, where the primary and secondary coils lie in the same metal layer next to each other. There are several problems coming up with such a power combining network. The biggest problem is the low magnetic coupling factor between the primary and secondary windings, which is typically around 0.5 even with minimum metal spacing. Secondly, since the metal spacing is small, capacitive coupling increases and degrades the quality factor of the coil. In addition, a major shortcoming of the lateral transformer structure is current crowding at the inner conductor edges due to proximity effect. This in turn increases the resistance of the structure and lowers the quality factor, resulting in lower transformer efficiency. Thus, the efficiency of a simple lateral transformer configuration is poor. In this paper, a novel transformer based lateral power combiner is presented, which alleviates most of the problems mentioned above and achieves very low insertion loss over the bandwidth of interest.

A new “figure 8” structure as shown in Fig.5 has been utilized. This structure, first proposed in [5], has been integrated into the PA. Each individual differential power amplifier drives the primary but the secondary is implemented in alternating orientation, resembling an “8”. This layout minimizes the effects of internal flux cancellation because now the currents in the primaries of two adjacent stages flow in the same direction. This results in significant efficiency improvement. An additional benefit stems from the alternating direction of the secondary windings. The secondary loop is now immune to common mode coupling from a distant source since the incoming magnetic flux induces voltages of opposite polarity across each section of the “figure 8”. It is thus advantageous to employ an even number of stages. A second important feature of the proposed structure is the use of two parallel coils for each primary, as shown in Fig 3. Because of the presence of primary windings on either side of each secondary winding, the current crowding effect discussed earlier is mitigated. In a single turn case, due to proximity effect, the edge coupled to the secondary takes the bulk of the current and results in enhanced resistance. But, here the current is spread more uniformly in the secondary, cutting the loss substantially. If we assume that the parallel inductors are equal, $L1 = L2$ and $R1 = R2$, then the resulting quality factor of the the primary coil is

$$Q = Q_1(1 + k) \tag{2}$$

resulting in an enhancement in the quality factor.

The final feature of this combiner is the minimization of eddy current losses. In the layout of the amplifier, it is convenient to place a ground ring around the inductor to provide low inductance paths to supply rails for the amplifier bypass caps. This loop lowers the quality factor of the transformer due to induced eddy currents. The eddy currents arise from the magnetic leakage due to the imperfect coupling between primary and secondary loops. By alternating the orientation of the secondary loops, the eddy currents are suppresses substantially, allowing a more practical layout to be realized.

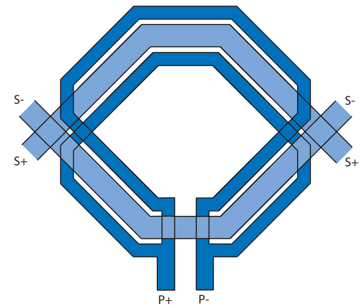

Fig. 3. Two parallel primary coils and one secondary coil.

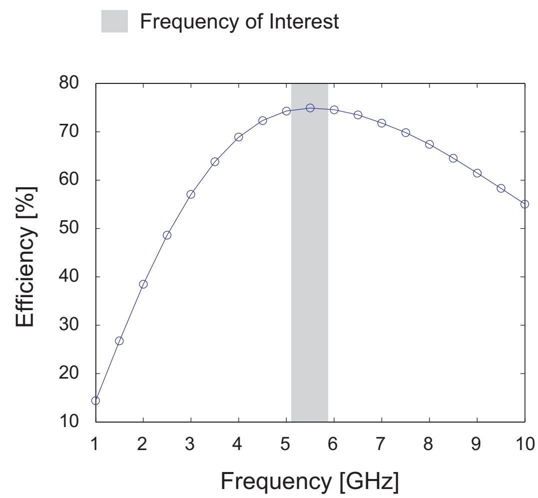

Fig. 4. Efficiency of the power combining network in the band of interest.

Full wave electromagnetic simulation has been performed using Agilent Momentum. Only the top metal layer was used for the windings while the underpass elements were realized with the lower metal layers. The insertion loss of the power combiner is 1.35 dB (75%) as shown in Fig. 4 and varies by only 0.4% over the band of interest. The proposed combiner is one of the smallest reported (0.65 mm × 0.15 mm), even compared to a 20 GHz combiner [3]. While the efficiency is not the highest reported, it should be noted that no special options like gold metal or thick metal layers were used.

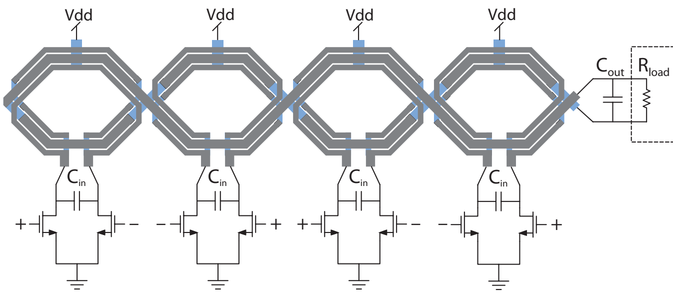

Fig. 5. Simplified schematic of final PA with the implemented power combining network.

III. Class AB Power Amplifier

The power combiner designed above was used to build a four stage differential Class AB power amplifier. The intended application for the power amplifier is a system which uses variable envelope modulation, requiring linearity. Class AB gives the best compromise between linearity and efficiency and hence was chosen as the preferred topology. The transformer power combining network described in the previous section also acts as an impedance transformation network. This helps to avoid the dc blocking capacitors at the output of each differential pair and leads to considerable area saving. Moreover, because the supply voltage is only 1 V, each stage needs to drive a small resistance in order to generate sufficient amount of power. This implies a large transformation ratio from the 50 Ω load to a small value seen by each stage. In a conventional LC matching network, the insertion loss of the network increases as the transformation ratio increases. However, a transformer has the property that its insertion loss is ideally independent of the transformation ratio, assuming that the quality factor of the primary and secondary coils remain unchanged [1].

Since the supply voltage of each stage is 1 V, each transistor has to deliver significant amount of current (200 mA) to deliver the required power. The widths of the devices are $1.2\,\mathrm{mm}$ each and have been optimized to get maximum output swing and efficiency. Fig. 5 shows the simplified schematic and layout of the implemented PA. Custom finger metal-oxide-metal (“MOM”) capacitors $C_{in} = 2.6\,\mathrm{pF}$ and $C_{out} = 610\,\mathrm{fF}$ are used for matching the input and output respectively. To minimize the supply and ground bounce, large bypass capacitor are needed. A combined NMOS/finger capacitor is utilized for this function.

IV. Experimental Results

The chip was fabricated using a digital 90 nm CMOS process utilizing only thin-oxide transistors. The die photo is shown in Fig. 6. The die area is 0.9 mm×0.9 mm including the pads. The die was probed using Cascade Microtech differential probes at the input and single-ended probe at the output. The power output was measured using HP8563E Spectrum Analyzer. At a supply voltage of 1 V, the maximum power obtained from the power amplifier is 24.3 dBm with an efficiency of 27%. The cable and probe losses have been carefully de-embedded but the pad losses are included in this number. A plot of the measured and simulated output power versus input drive is shown in Fig. 7. From the plot, the 1-dB compression point is calculated at 20.5 dBm. A plot of the measured and simulated efficiency versus output power is shown in Fig. 8. As expected, because the amplifier is Class AB in nature, the efficiency drops nearly linearly with decreasing output amplitude.

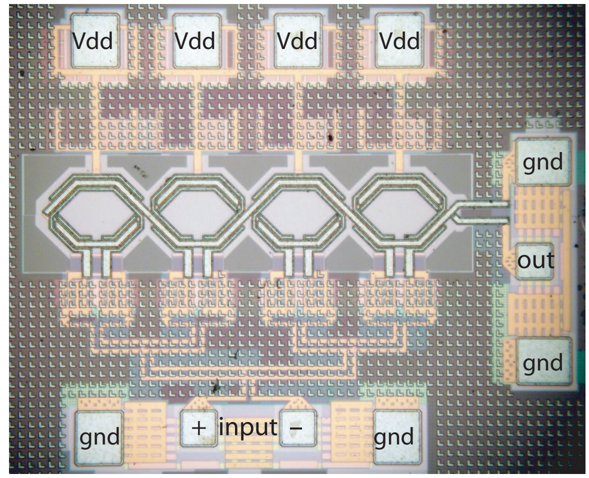

Fig. 6. Die photo of 90 nm CMOS power amplifier.

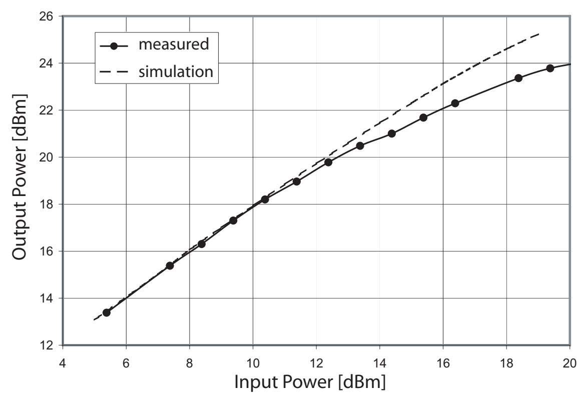

Fig. 7. Measured and simulated output power versus input power.

In order to measure the linearity of the amplifier, an IM3 two-tone test was performed. Two tones spaced at 100 MHz and generating a total output power of 20.5 dBm have been applied to the input of the PA. As shown in the spectrum of Fig. 9, the measured IM3 at 1-dB compression point is -20 dBc, while it improves to -28 dBc at 200 MHz tone spacing. While the measured 1-dB compression point, output power and efficiency of the amplifier are very close

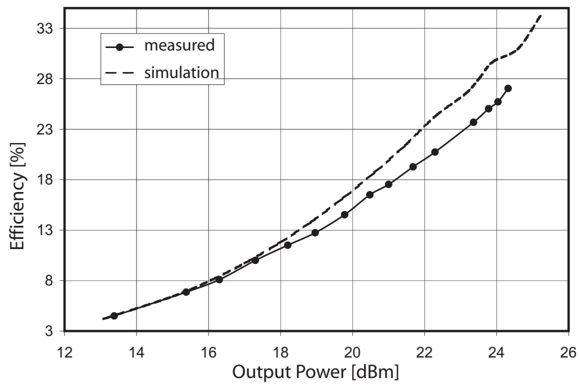

Fig. 8. Measured and simulated efficiency versus output power.

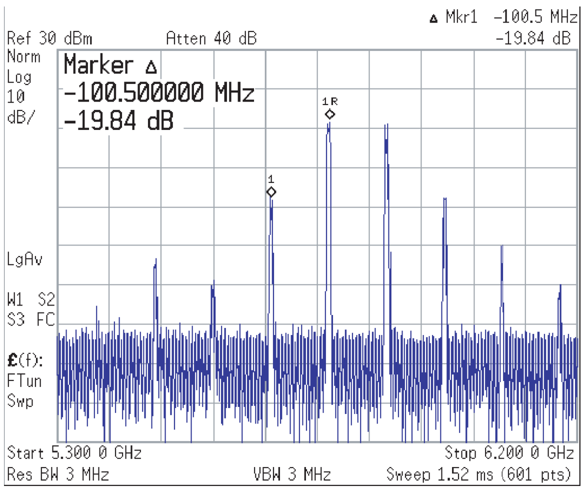

Fig. 9. Measured spectrum for a two-tone test.

to simulation results, the IM3 results are off by about 8.8 dB for 100 MHz tone spacing. The peak simulated IM3 value at a tone spacing of 100 MHz is -28.8 dBc. The discrepancy between simulation and measured results is due to the absence of off-chip decoupling capacitors for low frequency signals. In a two-tone test, the envelope of the current drawn by the Class AB amplifier varies at the rate of tone spacing. In the absence of decoupling capacitors, this current is drawn from the power supply. As a result, there is significant voltage ripple on the power supply degrading the IM3 performance of the amplifier. As this effect happens in the two tone test and not in the single tone test, the 1-dB compression point is not affected. However, the problem can be easily remedied using off-chip decoupling, which could not be realized in this version of the chip due to a layout problem. This is indeed verified in the measured results since the IM3 = -28 dBc at 200 MHz tone spacing matches simulation results more closely.

The power combiner described in Section II has nearly

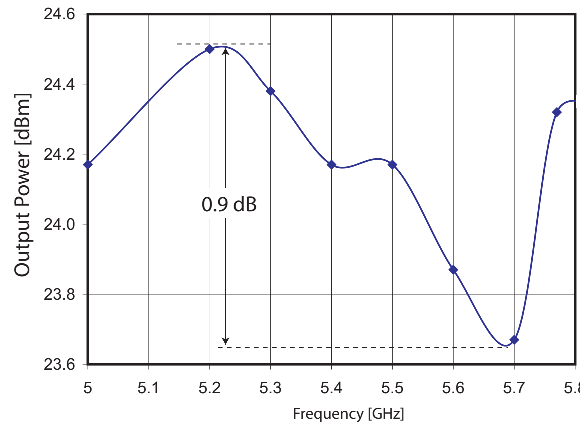

Fig. 10. Measured output power versus frequency.

constant efficiency over the band of interest. Fig. 10 shows the measured output power as a function of frequency. The power amplifier performs well over the whole band, maintaining peak output power greater than 23.5 dBm over the range of 5-5.8 GHz. Compared to state-of-the-art PAs reported in literature, despite using only 1 V power supply and a digital 90nm CMOS process, this PA's performance is comparable to many of the designs at higher supply voltage or in processes with RF enhancements.

V. Conclusion

In this paper, we have presented a CMOS 90nm power amplifier using thin oxide transistors. A transformer based power combining structure has been designed and used to build a four stage Class AB push pull amplifier. Despite the use of a single 1 V power supply and a digital CMOS process, a high output power of 24.3 dBm at a peak drain efficiency of 27% has been achieved. To the authors knowledge, this is the highest reported power obtained from a linear power amplifier using 1 V power supply and 90 nm thin oxide transistors.

Acknowledgment

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