

31.2 A 60GHz 1V +12.3dBm Transformer-Coupled Wideband PA in 90nm CMOS

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The opening up of the mm-wave band has created opportunities for high-data-rate communication, radar and medical imaging. The cost and size advantages of CMOS have motivated research on 60GHz CMOS front-end design [1]. However, very few CMOS mm-wave power amplifiers (PAs) have been reported so far. Furthermore, most of the mm-wave PAs reported use bulky transmission lines [2, 3], increasing silicon area and incurring higher substrate losses.

We demonstrate a fully integrated 60GHz transformer-coupled two-stage differential power amplifier with single-ended input and output in 90nm digital CMOS with no RF process options. This work uses on-chip transformers for a 60GHz PA as an integrated CMOS solution. Operating from a 1V supply, it achieves a 1dB compressed output power of +9dBm and saturated power of +12.3dBm. The chip occupies an area of only $660 \times 380 \mu\text{m}^2$ by taking advantage of the extensive use of small transformers.

Transformers are attractive as they can simultaneously perform impedance transformation and differential-to-single-ended conversion. In a multistage design, they also provide easy DC biasing. In this design, a 1:1 vertical transformer is built with two coupled loop inductors. The diameter of the loop inductors is an important design metric. For very small sizes, the impedance of the shunt magnetizing inductance becomes too small and most of the signal current is lost through it. A large transformer results in higher substrate losses and an increased series leakage inductance which also reduces the signal transfer to the secondary winding [4].

Transformers with different diameters and trace widths have been implemented with the top two metal layers. Figure 31.2.1 shows the simulated minimum insertion loss of 60GHz transformers, clearly indicating how the size can be optimized. Figure 31.2.2 shows the measured insertion loss versus frequency of a vertical transformer with a $42 \mu\text{m}$ diameter and $8 \mu\text{m}$ trace width. At 60GHz, the loss is below 0.9dB, showing the potential of transformers at these frequencies. The measured S_{21} shows the broadband nature of transformers, with 3dB bandwidth close to 30GHz.

The design of the PA is a simultaneous optimization of output power, power gain and efficiency while ensuring unconditional stability over all frequencies. The implemented circuit is shown in Fig. 31.2.3. It consists of two differential amplifier stages and optimized transformers for input, inter-stage, and output matching and differential-to-single-ended conversion. Note that the use of transformers eliminates the need for AC coupling capacitors and RF chokes while differential operation reduces the amount of bypass capacitance needed.

A difference in mm-wave PA design versus lower frequencies is a pronounced limitation on the maximum device width. Choosing the size of the output NMOS transistor is a compromise between maximum stable gain (MSG) and maximum output power. For high gain, the width of a finger (W_f) needs to be small enough. But for high output power, the total width (W) needs to be large. This means that a large number of fingers need to be placed in parallel; the connections to all these fingers introduce lossy parasitics, reducing gain and efficiency [2].

In order to simultaneously optimize the PA and transformers, the following systematic design algorithm is used:

(i) An appropriate NMOS device size ($W_f=1 \mu\text{m}$, $W=80 \mu\text{m}$ in our design) and bias current (22mA) are selected, ensuring that the device is biased near peak f_c current density ($0.3 \text{mA}/\mu\text{m}$). The contours for constant 1dB compressed output power and power gain (G_p) are then plotted on a Smith chart and an optimum drain load impedance (Z_{OPT}) is chosen (Fig. 31.2.6). Simultaneously, it is important to plot the load stability circle to ensure that Z_{OPT} is far from it.

(ii) The diameter and trace width of the output transformer are optimized to efficiently transform the 50Ω load impedance to the chosen value Z_{OPT} for each single-ended stage. The pad parasitics are taken into account and pad capacitance is used to tune the transformer secondary inductance. No additional tuning capacitors are used.

(iii) Besides presenting Z_{OPT} , the transformer should also have low insertion loss. Minimum insertion loss of the transformer, which assumes conjugate matching, is not the appropriate metric here. It is a good measure for the purpose of comparison between different transformers, but the more appropriate metric is the power gain (G_p) of the transformer (Fig. 31.2.2), which takes into account the fact that the load impedance is fixed to 50Ω . Thus, the design goal is to maximize transformer G_p , while simultaneously ensuring its input impedance is close to Z_{OPT} .

(iv) A similar procedure is adopted for the design of the inter-stage and input stage transformers. The driver is designed to avoid compression when the output starts to saturate.

Stability is a prime consideration in mm-wave PAs. Simulations revealed that the circuit is prone to instability in the 20-to-40GHz band, since the transistor gain increases but the losses of the transformer do not go up significantly. Therefore, an RC stabilization network [5] is added at the gate of each transistor (Fig. 31.2.3). This network is sized to ensure resistive loss below 40GHz, without significantly affecting the power gain at 60GHz. The losses also improve low-frequency common mode stability. In addition, the gate bias lines through the transformer center taps have been adequately de-Q'ed to quench common-mode oscillations. Transformers also help decouple the common-mode behavior of driver and output stages and make output-stage common-mode stability VSWR-independent.

The prototype PA is fabricated in a 90nm 1P7M digital CMOS process. The measured S-parameters are shown in Fig. 31.2.5. At a supply voltage of 1V, S_{21} at 60GHz is 5.6dB and has a peak value of 7.7dB at 48GHz. The 3dB bandwidth of the amplifier exceeds 22GHz (43 to 65GHz; upper point limited by VNA). The input match is better than -8dB from 50 to 65GHz. The amplifier is unconditionally stable at all frequencies as indicated by the measured stability factor (k) in Fig. 31.2.5.

The 60GHz power measurements are shown in Fig. 31.2.4. Using a 1V supply, the measured 1dB compressed output power is +9dBm and saturated output power is +12.3dBm, which are the highest reported for a 60GHz CMOS PA [2][3][6]. This power is also comparable to some SiGe amplifiers operating from higher supply voltages. The measured peak drain efficiency is 32% and peak PAE, including DC power consumption of the driver stage, is 8.8%. The PAE can be improved by using a smaller size cascode driver stage. The measured P_{1dB} has a peak value of +9.7dBm at 50GHz.

The chip micrograph is shown in Fig. 31.2.7. The small die size of $660 \times 380 \mu\text{m}^2$, including probe pads, clearly demonstrates the area benefit of using transformers at mm-wave frequencies.

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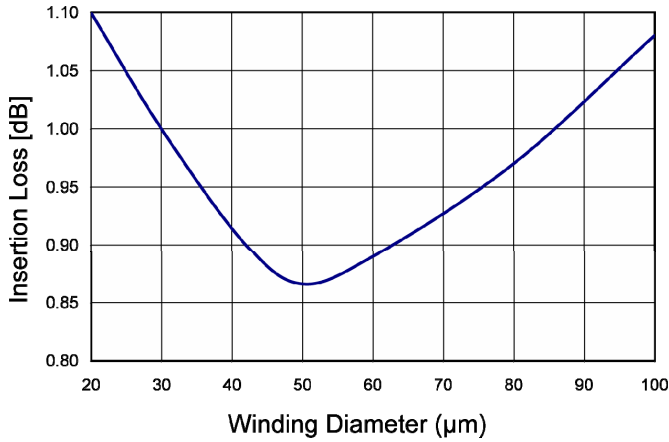


Figure 31.2.1: Simulated minimum insertion loss of 60GHz transformers as a function of diameter of the windings.

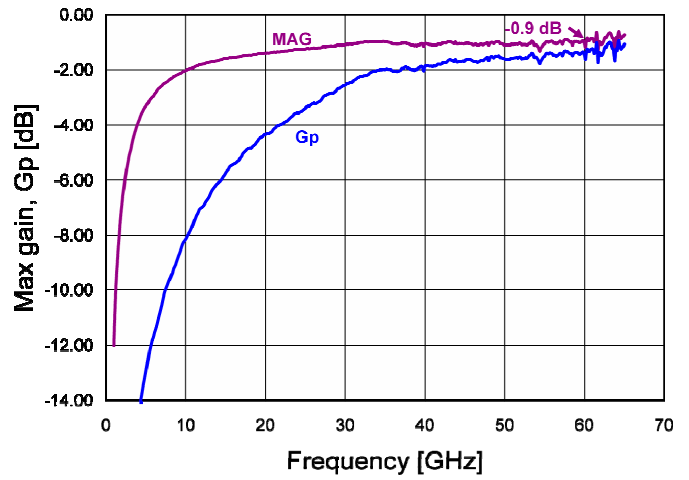


Figure 31.2.2: Measured maximum available gain (MAG) and power gain (Gp for a 50Ω load) of a 1:1 vertical transformer with an inner diameter of 42μm and trace width of 8μm.

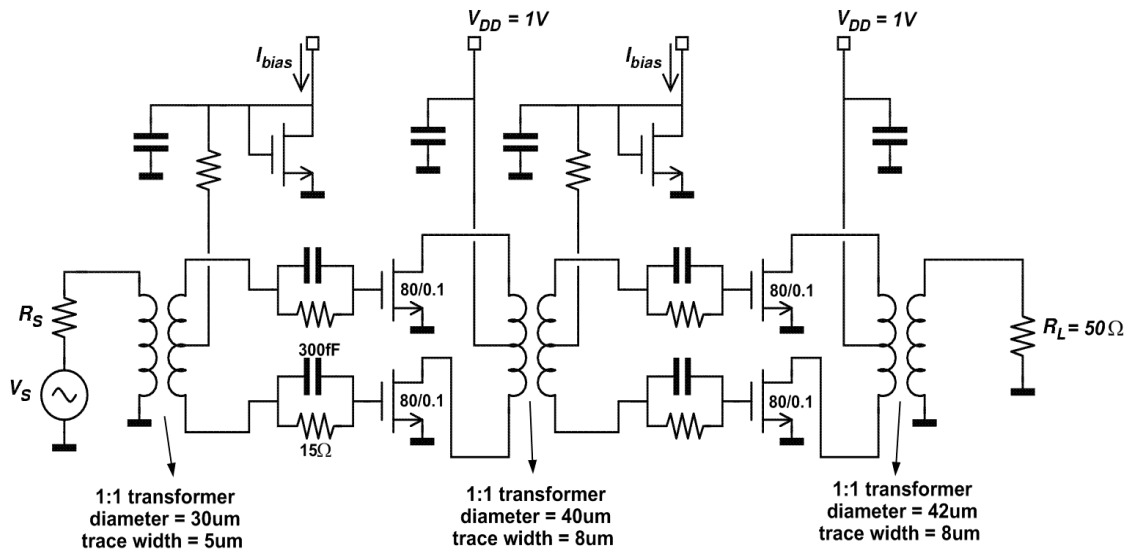


Figure 31.2.3: Schematic of the two stage differential transformer-coupled power amplifier.

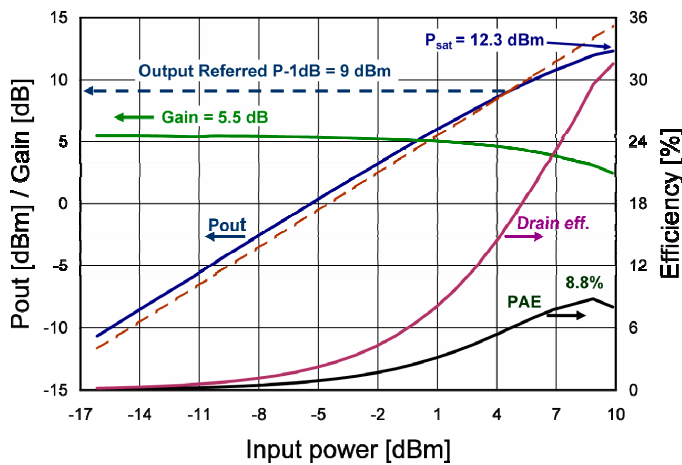


Figure 31.2.4: Large signal output power, gain and efficiency measurements.

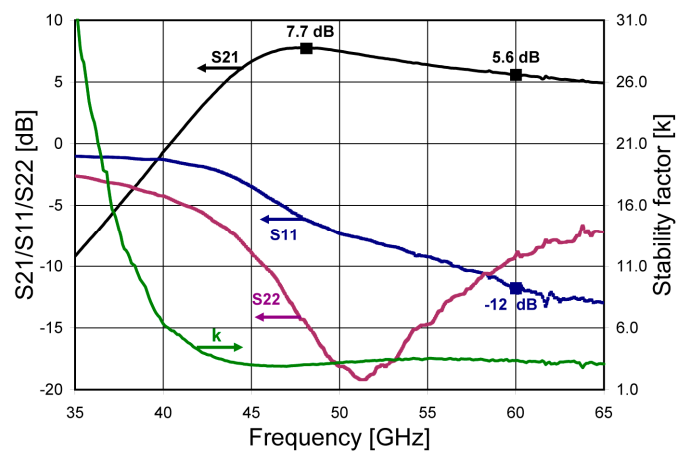


Figure 31.2.5: Measured S-parameters and k-factor of the power amplifier.

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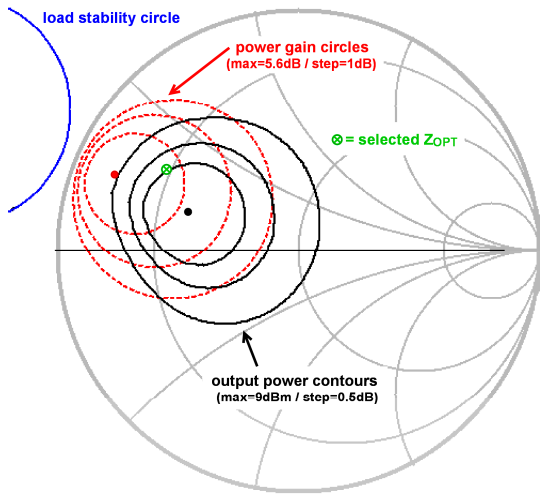


Figure 31.2.6: Load stability circle, power gain circles (G_p) and 1dB compressed output power contours at 60GHz for a single 80µm transistor with input stabilizing network.

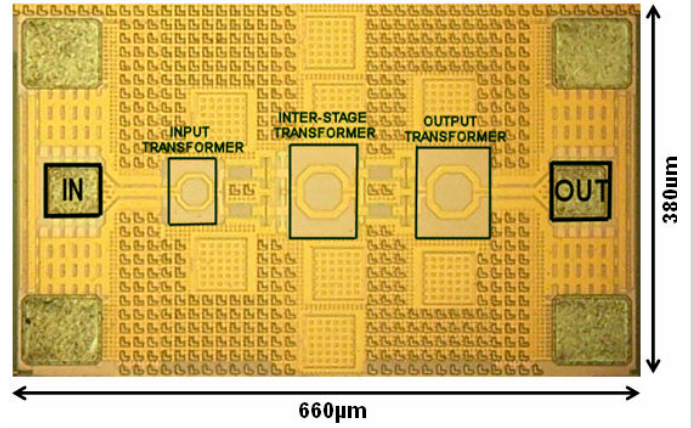


Figure 31.2.7: Chip micrograph.