

## 9.2 A Robust 24mW 60GHz Receiver in 90nm Standard CMOS

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Emerging applications for the 60GHz spectrum include extremely high-data-rate short-range communication systems. Many of these applications are expected to enter the realm of consumer electronics where low cost and mass production are prerequisites, favoring the application of digital CMOS technology. In this paper, a highly integrated receiver front-end is demonstrated that is manufactured in a digital CMOS process using a design approach amenable to mass production. Unlike many previous attempts in CMOS, the results of the design are well predicted by the simulation results, matching the desired frequency band and the simulated gain to a very high accuracy. Low noise and high gain are demonstrated with low power consumption. These factors in unison make this front-end suitable for small footprint mobile applications such as a cell phone, PDA, or laptop computer.

The design approach relies on carefully modeled building blocks such as CPW transmission lines, MOM capacitors, customized BSIM3 large signal transistor models and extensive EM simulations. An accurate and predictable modeling methodology is an integral part of low power design, as it allows one to search for the optimal topology. Robust performance in the face of process variations is a difficult feat for mm-wave circuits operating at the fringe of the technology. Overdesign is one possibility but results in a non-optimal high-power-consumption design. To illustrate the low-power design procedure for mm-wave circuit blocks, a 60GHz to baseband directconversion receiver shown in Fig. 9.2.1 is designed and fabricated as a demonstration.

Several techniques are applied to make this front-end circuitry more stable and less sensitive to modeling inaccuracy and process variations. Wideband matching networks provide more stability in the face of process and corner variations and more predictable performance especially for narrowband design techniques. Even though previous research shows that common source LNAs have excellent gain, output power, and noise [1], the amplifier is much more sensitive to process variations arising from the bilateral nature of the device. A shared junction cascode transistor model, Fig. 9.2.2, is used in the LNA to be more tolerant of process variations. Gain is sacrificed in favor of stability and two gain stages are used in the LNA which provide sufficient gain to reject the noise of the mixer. Wideband optimum Q matching networks are built from CPW transmission lines with  $Z_0=50\Omega$ . Transmission lines are preferred to spiral inductors since they provide well defined return currents and higher isolation. Inaccurate return current loops in matching networks leads to mistuned amplifiers and sub-optimal performance. The LNA has a simulated power gain of 12dB while consuming 14.5mW from a 1V supply.

An active single-balanced current-commutating mixer, as shown in Fig. 9.2.2, is employed in the system using a series transmission line filter between the  $g_m$ -stage and switching stage. This improves the conversion gain of the mixer and decreases the noise contribution of the switching stage. Compared to a shunt tuning, the series tuning network is less sensitive to the length of the transmission line. This transmission line forms a filter with parasitic source and drain capacitances of the transistors and prevents the loss of the high-frequency RF current signal into the substrate. A shunt transmission line also requires knowledge of the return current, which is more difficult to predict and depends on the details of the layout. Both the RF and LO port of the mixer receive the 60GHz band (57 to 63GHz) signals and the mixer converts the RF signal to differential output from DC to more than 2GHz. The mixer has simulated gain of 6.5dB and consumes about 6.5mW from a 1V supply.

The differential LO signal is created from an on-chip bifilar balun. The balun has a relatively small footprint at mm-wave frequencies ( $80\times 80\mu\text{m}^2$ ). Metal width, spacing, number of turns and sizing are all optimized to provide low insertion loss and maximal voltage swing at the LO port. The balun also provides input matching of the LO port to  $50\Omega$  directly, obviating the need for additional matching networks which introduce more loss to the LO port. It has been shown that asymmetric LO could severely degrade the circuit performance [2]. The symmetric balun and its performance are shown in Fig. 9.2.4. Due to low insertion loss of the balun, low LO power of  $-2.5\text{dBm}$  is needed to drive the mixer. The large-signal properties of the LO port are taken into account in the matching network. The nonlinear capacitance of the switching stage will change periodically with the LO signal and so the average large-signal capacitance is used to match the LO port using the large-signal transistor models.

The baseband VGA, as shown in Fig. 9.2.1, amplifies the signal through several stages of modified-Cherry-Hooper amplifier cells. The VGA gain range can be adjusted through a single control voltage monotonically up to 60dB. Several bandwidth enhancement techniques are used in the VGA to maintain more than 2.2GHz bandwidth at low power consumption. Inversely scaled transistors from input to output are used to increase the bandwidth of the overall amplifier. This approach reduces the power consumption considerably without degrading the noise figure. A dual-feedback amplifier is used in the design of the VGA which provides DC-offset cancellation and bandwidth enhancement for the receiver. The VGA drives an output buffer that is used for measurement purpose only. The VGA and output buffer consume 3mW and 8.5mW from a 1V power supply.

The chip is fabricated in a 90nm digital CMOS process ( $f_t=100\text{GHz}$ ) and tested using on-chip probes. A die micrograph is shown in Fig. 9.2.7 and the die area is  $1.55\text{mm}^2$  (including pads). The input matching of the receiver is shown in Fig. 9.2.3 and is approximately below  $-10\text{dB}$  for the entire 60GHz band. The overall receiver gain performances are also shown in Fig. 9.2.3. The receiver has a wide gain tuning range of about 60dB which allows the system to operate in a wide dynamic range of input signals. The VGA is also characterized separately so that the performance of the RF front-end could be determined. Measurements show that the RF front-end has a fixed gain of 18dB, very closely matching the simulated performance. Large-signal performance of the receiver at the center band and its noise figure are shown in Fig. 9.2.5. An average  $N_{\text{DSB}}$  of 6.2dB is observed over the band of interest using a 50-to-75GHz noise source. This receiver is compared to several 60GHz front-ends published recently (Fig. 9.2.6). The performance is very favorable, particularly with respect to the predictability and the low power consumption.

### Acknowledgments:

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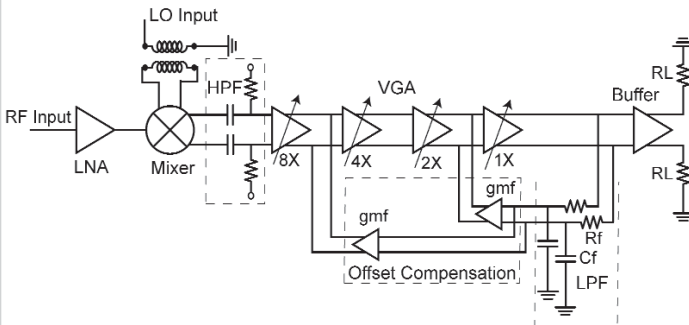


Figure 9.2.1: System-level schematic of the front-end receiver.

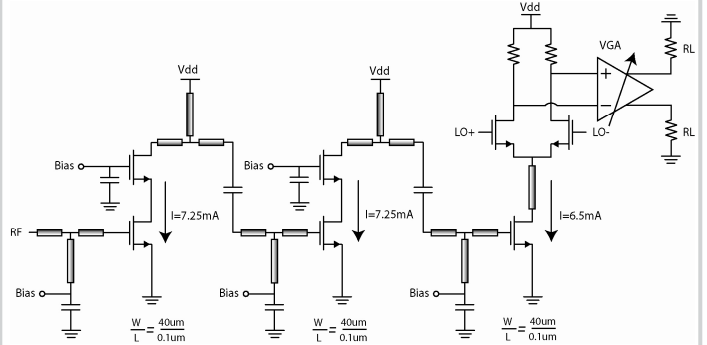


Figure 9.2.2: Circuit-level schematic of the LNA and the mixer.

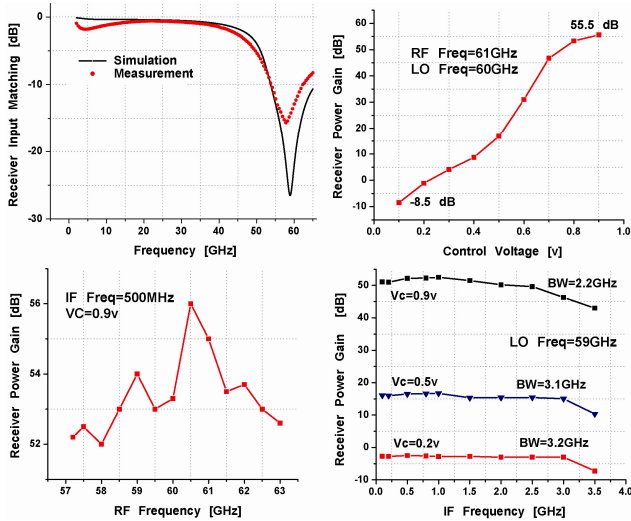


Figure 9.2.3: Receiver input matching  $S_{11}$ , differential output to single-ended input power gain and IF bandwidth.

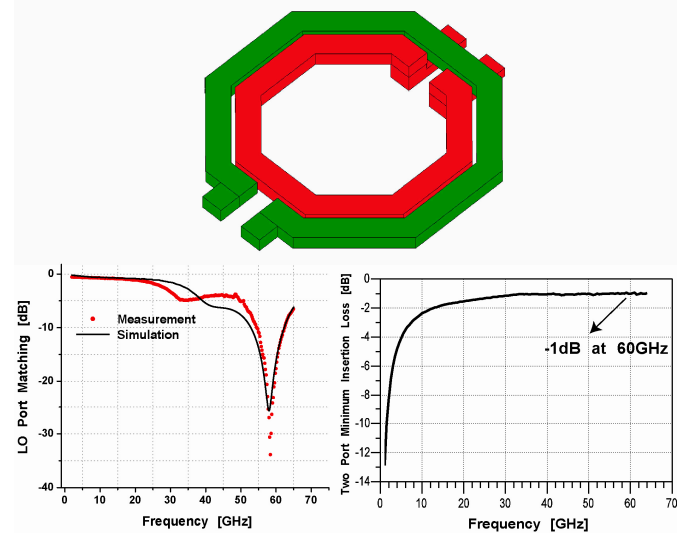


Figure 9.2.4: LO port balun structure and its performance.

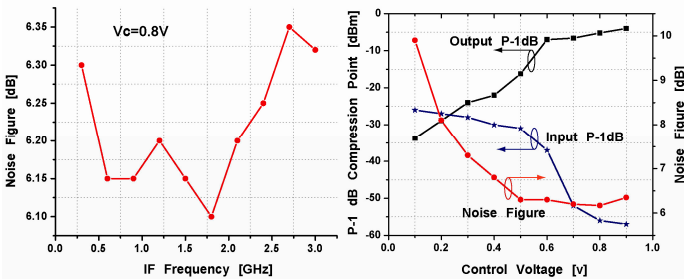


Figure 9.2.5: Receiver noise figure and large signal nonlinearity.

	[3]	[4]	[5]	This Work
Technology	90nm CMOS	90nm CMOS	200GHz 0.13um SiGe BiCMOS	90nm CMOS
Power Gain	16dB	21.8 to 22.5dB	38 to 40dB	-8.5 to +55.5dB
Noise Figure	7dB	8.4dB	5 to 6.7dB	6.1 to 6.35dB
$P_{1dB}$ (in)	-21dBm	N/A	-36dBm	-26dBm
LO to RF Leakage	< -90dB	N/A	< -77dB	< -77dB
Power Dissipation	60mW	60mW*	190mW*	24mW
Supply Voltage	1.2V	1.2V	2.7V	1V

\* These values exclude the synthesizer power dissipation and output buffer for a fair comparison.

Figure 9.2.6: Performance of 60GHz front-end receivers with less than 10dB noise figure.

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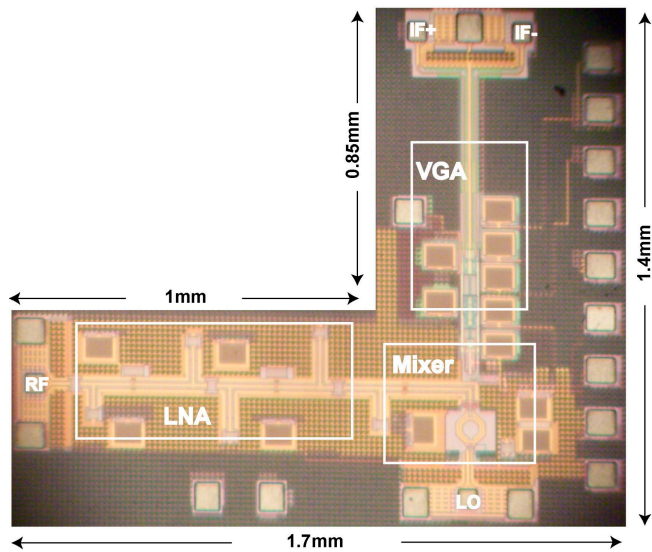


Figure 9.2.7: Die micrograph of the front-end receiver.