

# Transformer-Coupled Power Amplifier Stability and Power Back-Off Analysis

Debopriyo Chowdhury, *Student Member, IEEE*, Patrick Reynaert, *Member, IEEE*, and Ali M. Niknejad, *Member, IEEE*

**Abstract**—We present a mathematical analysis of the common-mode instability and power back-off feature of a transformer-coupled Class-AB differential power amplifier (PA). The efficient impedance matching of the transformer combiner and efficiency improvement at power back-off, a major benefit of this structure, are illustrated. In addition, an analytical model is derived to predict the common-mode oscillations in PA. The analytical results, based on a simple hand-calculation model for the transistor, show good agreement with simulation results using complete 90-nm models. Two methods to suppress the common-mode oscillations are investigated and analyzed in detail.

**Index Terms**—CMOS, power amplifiers (PAs), power combining, stability.

## I. INTRODUCTION

THE rapid growth of the wireless industry over the last decade has led to a successful development of low cost high frequency CMOS circuits. However, still today the power amplifier (PA) is often implemented in a separate technology, hindering full integration. In the last few years, considerable research effort has been invested in the development of fully-integrated CMOS PAs [1]–[3].

Stability has always been a major concern for designers of high frequency amplifiers. Although instabilities can be encountered in all RF and microwave circuits, PAs have the potential to exhibit one or more types of instabilities simultaneously. In addition to the linear feedback mechanism that creates an oscillation, the strong nonlinearity of PAs may also push them into an unstable region. The instability has been analyzed in details for a switching-mode amplifier using chaos theory and bifurcation tools [4]. In this paper, we focus on amplifiers employed in modern communication systems that employ amplitude modulation and multi-carrier signaling. For such applications, linear amplifiers such as Class-AB are mostly used and their stability analysis, taking into account both on-chip and off-chip components, needs careful consideration. Of particular importance are

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D. Chowdhury and A. M. Niknejad are with the Department of Electrical Engineering and Computer Science, University of California at Berkeley, CA 94720 USA. (e-mail: ebopriyo@eecs.berkeley.edu).

P. Reynaert was with the Department of Electrical Engineering and Computer Science, University of California at Berkeley, CA 94720 USA. He is now with the Department of Electrical Engineering (ESAT-MICAS), Katholieke Universiteit Leuven, Leuven B-3000, Belgium.

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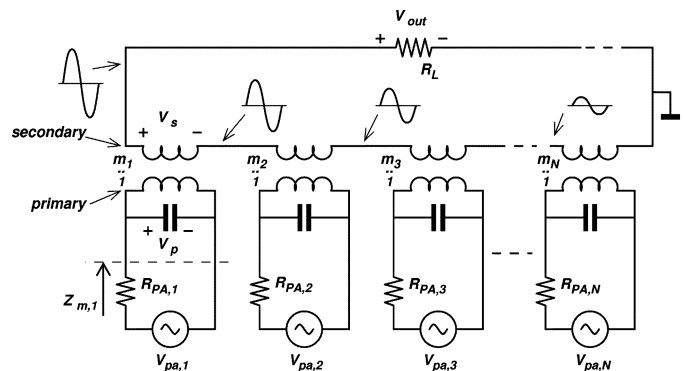


Fig. 1. PA topology using transformers for power combining.

common-mode oscillations in differential PA, which are often not captured by traditional microwave approaches (like the  $k$ - $\Delta$  criterion or the  $\mu$  test). We present a mathematical analysis of the common-mode instability of a transformer-coupled PA as well as means to suppress the oscillation.

The other important challenge for CMOS technology is to obtain sufficient output power from a PA, particularly because of the low breakdown voltage and high knee voltage of deeply-scaled CMOS transistors. Power combining is an attractive solution [2], [3], [5]. In particular, we have presented in [1] and [3] an on-chip transformer-based voltage combiner, that combines the power of four push-pull amplifiers. This type of transformer combiner has the property that individual stages can be turned off in power back-off mode to enhance efficiency at lower output power [3]. The power back-off feature is fairly general and can be applied successfully in many architectures. In this work, we present an in-depth analysis of power combining and power back-off properties.

## II. TRANSFORMER-BASED POWER COMBINING AND POWER BACK-OFF

A simplified schematic of the architecture used in [1] is shown in Fig. 1. In contrast to the distributed active transformer (DAT) approach of [2], the topology in Fig. 1 also allows power control since each stage works independently and can be turned off. In what follows, the power combining and power back-off properties of this architecture are analyzed in greater detail.

### A. Power Combining and Impedance Transformation

When calculating the transformed load impedance  $Z_{m,j}$  as seen by PA  $j$ , it is important to realize that the secondary winding of each transformer carries the same current  $V_{out}/R_L$ .

As such, all PAs are coupled to each other. Using superposition, the transformed load impedance can be obtained as

$$Z_{m,j} = \frac{\left( R_L + \sum_{i=1}^N m_i^2 \cdot R_{PA,i} \right) \cdot V_{pa,j}}{m_j \cdot \sum_{i=1}^N m_i \cdot V_{pa,i}} - R_{PA,j} \quad (1)$$

with  $N$  being the number of transformers,  $m$  the transformer turn ratio,  $R_{PA}$  the output impedance and  $V_{pa}$  the complex output voltage of each PA. It can clearly be seen that the transformed load impedance  $Z_{m,j}$  depends on both the output impedance and output voltage (both magnitude and phase) of each PA, which can be considered as a form of *load-pull*.

When all PAs have the same output impedance, generate the same output voltage, and all transformers use the same winding ratio  $m$ , (1) simplifies to a resistive value of

$$R_m = \frac{R_L}{N \cdot m^2}. \quad (2)$$

The impedance seen by each amplifier is now determined by two factors only: the turn ratio  $m$  of each transformer and the number of parallel stages  $N$ . Note that it is independent of output impedance of the other PAs. Under the same conditions, the total output power, delivered to the load, equals

$$P_o = N^2 \cdot m^2 \cdot \frac{V_p^2}{2R_L} \quad (3)$$

and the impedance transformation ratio is defined as

$$r = \frac{R_L}{R_m} = N \cdot m^2. \quad (4)$$

From (3), it can be seen that the output power can be increased either by increasing  $m$  or  $N$ . On the other hand, (4) shows that the impedance transformation ratio increases only linearly with  $N$  but quadratically with  $m$ . It is well known that practically a higher turn ratio, i.e., a high  $m$ , also results in a high insertion loss [2]. Therefore, it is far more efficient to increase the number of stages  $N$ , rather than increasing  $m$ . Such an approach achieves a high output power with a rather moderate impedance transformation ratio. This is an important aspect in low-voltage PA design.

### B. Power Control and Power Back-Off

When one or more amplifiers in Fig. 1 are *turned off*, the output power will decrease. Let us assume that the topology consists of four identical stages coupled using four 1:1 transformers. When all four stages are active, the transformed impedance seen by each stage is  $R_m = R_L/4$  and the gain of each stage is  $g_m R_L/4$ . If  $V_i$  is the input voltage, the output voltage of each stage ( $V_p$ ) and the total output voltage ( $V_{out}$ ) across the load are given by

$$V_p = \frac{g_m R_L}{4} \cdot V_i = \frac{1}{4} g_m R_L \cdot V_i \quad (5)$$

$$V_{out} = 4V_p = g_m R_L \cdot V_i. \quad (6)$$

This is the case when peak output power is being generated and all the amplifiers are designed to operate at maximum efficiency at this power level.

Now suppose that the input voltage reduces from  $V_i$  to  $V_i/2$  and two of the parallel stages are turned off. The impedance

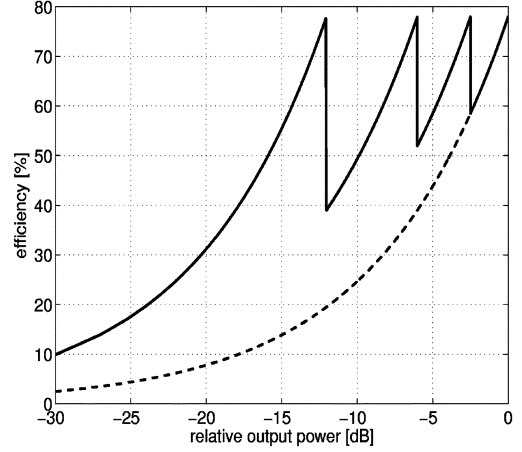


Fig. 2. Efficiency versus output power for Class-B amplifier.

transformation ratio changes from 1:4 to 1:2 and each stage sees an effective resistance  $R_m = R_L/2$ . The output voltage of each stage and the total output voltage are now given by

$$V_p = \frac{g_m R_L}{2} \cdot \frac{V_i}{2} = g_m R_L \cdot \frac{V_i}{4} \quad (7)$$

$$V_{out} = 2V_p = \frac{g_m R_L V_i}{2}. \quad (8)$$

Thus, we see that in spite of turning off 2 stages (6-dB power back-off), because of dynamic load variation, the output swing of each active stage ( $V_p$ ) is still the same and hence it operates at peak efficiency even at a lower power, an important feature in systems having high peak-to-average power ratio (PAPR). The same is true even if one or three stages are turned off to get 2.5- or 12-dB power back-off, respectively.

Let us now analyze the effect of power back-off on the different classes of amplifiers. The efficiency of a single Class-B amplifier is given by

$$\eta_B = \frac{\pi}{4} \frac{V_p}{V_{DD}} \quad (9)$$

where  $V_{DD}$  is the supply voltage. From the previous analysis, we have seen that when we turn off stages, due to dynamic load modulation, the output swing of each of the remaining active devices ( $V_p$ ) returns to the maximum value at 2.5-, 6-, and 12-dB power back-off. Thus, even at reduced output power, each active Class-B amplifier, and thus the whole structure operates at peak efficiency. This is illustrated by Fig. 2.

For Class-A amplifiers, the efficiency is given by

$$\eta_A = \frac{V_p^2}{2R_m I_Q V_{DD}} \quad (10)$$

where  $I_Q$  is the bias current of each stage. At a specified back-off, when a stage is turned off,  $V_p$  returns to the maximum value, but since  $R_m$  increases, the efficiency of a Class-A amplifier does not return to peak value, unlike Class-B amplifiers. Thus, this scheme of average efficiency enhancement works best for Class-B amplifiers. However, if one dynamically adjusts the bias current ( $I_Q$ ) of the remaining active PAs, the efficiency of Class-A can further be increased and peak efficiency can again be achieved at power back-off.

In the ideal analysis shown above, we have neglected the loading effects of the “off” amplifier. It can be shown that if



where  $B$  represents the network currents and voltages shown in Fig. 4 and  $S_i$  is the input matrix and are given by

$$B = \begin{bmatrix} I_1 \\ I_2 \\ I_3 \\ V_{gs} \\ I_4 \end{bmatrix}, \quad S_i = \begin{bmatrix} V_i \\ V_i \\ 0 \\ V_i \\ 0 \end{bmatrix}.$$

The matrix  $[A]$  is as shown in (12) at the bottom of the previous page, where  $L = j\omega L_p + R_p$  ( $R_p$  is due to finite  $Q$  of on-chip transformer winding) and  $C = R_1 + 1/j\omega C_b$ .

For the system to oscillate, there must be finite current flow in the circuit, meaning that matrix  $B$  must be nonzero, even in the absence of any applied signal [6], [7]. This can be true only if  $A$  is a singular matrix

$$\det[A] = 0. \quad (13)$$

The complete expression for  $\det[A]$  is shown in Appendix. In general, the determinant has a real part as well as an imaginary part and thus we have two equations. Setting the real part equal to zero gives us the oscillation frequency, while setting the imaginary part equal to zero gives us the start-up condition. However, if we make a high  $Q$  approximation and neglect the losses in the system, (13) can be simplified as

$$\begin{aligned} 0 = & L_p L_v L_g \omega^6 \\ & + \left[ \frac{L_g L_p}{C_{gs}} + \frac{L_g L_v}{C_{gs}} + L_g \left( \frac{L_p}{C_b} + \frac{L_v}{C_b} + \frac{L_v}{C_{gd}} \right) + \frac{L_v L_p}{C_{gs}} \right] \\ & \times \omega^4 - \left[ \frac{L_g}{C_{gd} C_{gs}} + \frac{1}{C_{gs}} \left( \frac{L_p}{C_b} + \frac{L_v}{C_b} + \frac{L_v}{C_{gd}} \right) \right] \\ & \times \omega^2 + \frac{1}{C_b C_{gs} C_{gd}}. \end{aligned} \quad (14)$$

A solution of (14) gives the potential oscillating frequencies for the designed PA. From (14), we see that there are three positive solutions of  $\omega$ , meaning that the amplifier can exhibit multimode oscillations. In a general case, the three frequency components can exist simultaneously and thus the voltage at any node, ignoring nonlinearities, can be written as

$$V = V_1 \cos(\omega_1 t + \theta_1) + V_2 \cos(\omega_2 t + \theta_2) + V_3 \cos(\omega_3 t + \theta_3). \quad (15)$$

For analysis of oscillating frequency, we set the input matrix  $S_i$  [in (11)] to zero. However, if now a voltage  $V_i$  is applied at the oscillating frequency, the matrix equation can be re-solved to obtain the port input impedance ( $Z_i = V_i/I_1$ ). For oscillation to occur, the real part of this port impedance must be negative. Having already determined the possible oscillation frequencies, it becomes very easy for us to calculate the input impedance of the amplifier and determine if start-up conditions are satisfied or not.

As an example, if  $L_p = 200$  pH,  $L_v = 1$  nH,  $L_g = 100$  pH,  $C_b = 20$  pF, then the three solutions are  $\omega_1 = 1.02$  GHz,  $\omega_2 = 11.39$  GHz and  $\omega_3 = 35$  GHz. Time-domain simulation results for this combination shows that only the mode at 11.39 GHz exists. The frequency  $\omega_3$  being very high, the losses of the system are high enough to suppress this mode. The tone at 1.02 GHz cannot sustain, because the real part of the input

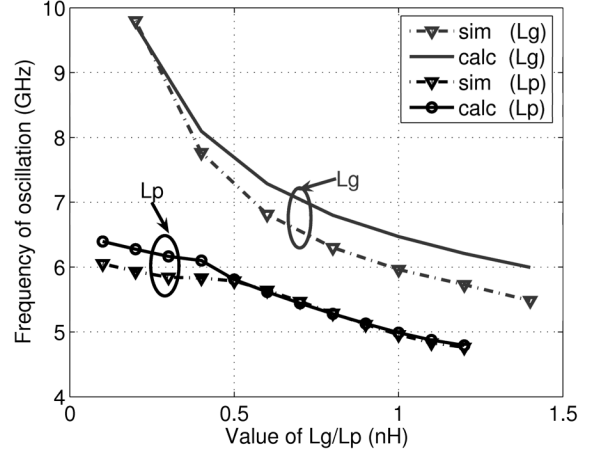


Fig. 5. Simulated and calculated oscillation frequency as a function of  $L_p$  and  $L_g$ .

impedance at that frequency is positive. On the other hand, the resistance being negative at 11.39 GHz, we observe the oscillation tone in simulation. Multimode oscillations are possible in general although they require a system nonlinearity that is higher than cubic [8].

The analysis in this paper accurately predicts the existence of common-mode instability in a linear PA. It is interesting to observe that because of the presence of ground bond-wire, the bypass capacitor is not connected to a perfect ground and hence it can indeed cause instability.

### C. Verification With Simulation Results

The concept developed in the previous section is verified using the designed PA in 90-nm 1P7M CMOS process. A transient analysis was performed and a Fourier transform of the output voltage was used to obtain oscillation frequency. Fig. 5 shows a comparison of the simulated and analytically calculated values of the frequency of oscillation as a function of the primary inductance  $L_p$  ( $L_g$ ,  $L_v$  and  $C_b$  are held fixed at 1 nH, 1 nH, and 20 pF) and also as a function of  $L_g$  ( $L_p$ ,  $L_v$ , and  $C_b$  are held fixed at 100 pH, 1 nH, and 20 pF). The predicted value of oscillation from matrix analysis is a little higher than the simulated value due to the extra capacitance present in the complete 90-nm transistor model. However, in spite of this, we can see that for various combinations of component values, the analytical method proposed in this paper can predict the instability of the amplifier with a good degree of accuracy.

### D. Stabilization of the Amplifier

1) *Adding a Gate Resistance:* A PA needs to be stable for passive load and source terminations. A common way to achieve this in microwave amplifiers is to insert a gate resistance (labeled  $R_g$  in Fig. 4), so that the losses in the system compensate for any negative port resistance. However, adding gate resistance impacts power gain of the amplifier and we would like to use the smallest possible value, or design an appropriate bypass network, to realize the best performance, especially at high frequency.

Fig. 6 shows the variation in the real part of input impedance as a function of frequency, which can be obtained from the solution of (11) ( $Z_i = V_i/I_1$ ). At the oscillation frequency, this resistance will be negative and as a first guess we can use this value as the gate resistance. However, it is important to note that

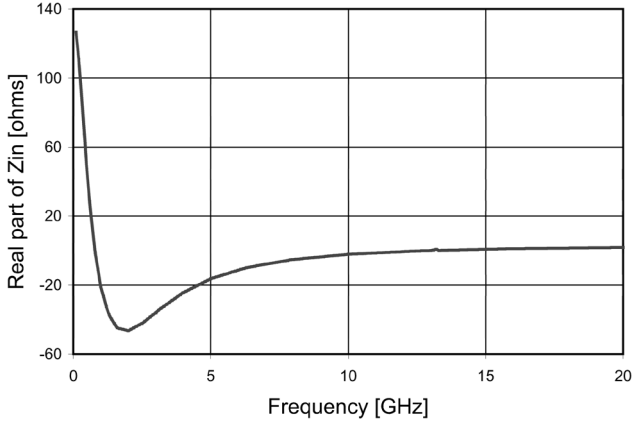


Fig. 6. Real part of the input impedance versus frequency.

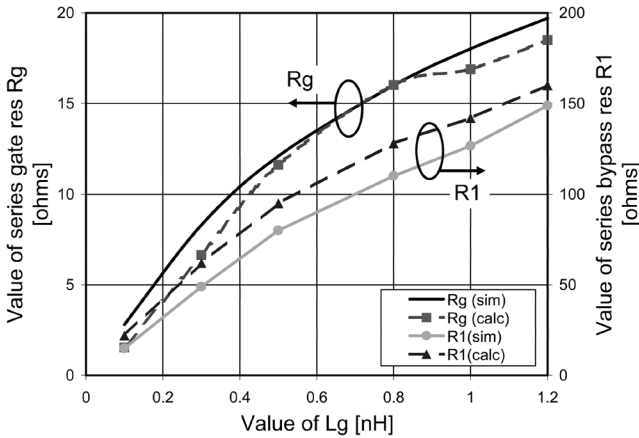


Fig. 7. Comparison of gate resistance and series bypass resistance required to kill oscillation.

as soon as we add an  $R_g$  to the system, the oscillation frequency changes and should be re-evaluated using (14). This is where it becomes necessary to use the complete equation described in Appendix . Once the new oscillation frequency is calculated, we can recalculate the negative resistance at that frequency and update the value of  $R_g$ . In practice, the iteration converges within two or three attempts. Fig. 7 shows a comparison of analytically calculated value of gate resistance and simulated value required to suppress all oscillations, for different values of the ground line inductance  $L_g$ . Similar tests were also performed by varying different component values of the PA circuit. It is seen that the proposed method can accurately determine the required loss and also gives insight to its variation with different component parameters, so that we may account for process variations.

2) *De-Q Bypass Capacitor*: Another stabilizing option is to insert a resistance  $R_1$  in series with the bypass capacitor, as shown in Fig. 3. The matrix equation formulated in this work already includes the effect of  $R_1$  and hence we may calculate the oscillation frequency and the negative resistance at that frequency, exactly as before, but this time using a finite value for  $R_1$ . As  $R_1$  increases, the input impedance becomes more positive. Fig. 7 compares the simulated and analytically obtained value of  $R_1$  required to suppress oscillation. From the graph, we see that for larger values of  $L_g$ , the value of  $R_1$  required is large, making this method alone unsuitable. However, we may easily extend this idea to design a bypass network with multiple

$RC$  networks in parallel, in such a way that it is low  $Q$  over a wide frequency range (for stabilization), as well as moderately low impedance. The matrix method described in this paper can be directly extended to include such a network.

#### IV. CONCLUSION

Power combining and novel transformer architectures are becoming more important as a means to implement fully integrated CMOS PAs. This paper has described the basic operation of transformer based power combining and impedance transformation. Furthermore, it is shown that by using the correct class of operation in the core PA, efficiency boost at power back-off is obtainable. An analytical analysis of common-mode oscillations was described and the results are compared with transient simulations. A good comparison between the two is achieved which clearly demonstrates the usefulness of this approach. Two techniques to suppress the common-mode oscillations were investigated using the proposed analysis technique.

#### APPENDIX DETERMINANT OF A

$$\begin{aligned}
 0 = & -\frac{R_{L1}}{C_{gd}}\Sigma L - \frac{R_g}{C_b}\Sigma L - \frac{C_{gs}R_g}{C_bC_{gd}}\Sigma L - \frac{r_o}{C_{gd}}(L_g + L_v) \\
 & - \frac{C_{gs}L_g}{C_bC_{gd}}(r_o + R_p) - \frac{r_o}{C_b}(L_p + L_v) - \frac{g_mL_gR_1r_o}{C_{gd}} \\
 & - \frac{g_mR_gr_o}{C_b}\Sigma L - \left( R_1R_g + \frac{C_{gs}R_1R_g}{C_{gd}} \right) \\
 & \times (r_o + R_p) - \frac{r_oR_p}{C_b}(g_mL_g + C_{gs}R_g) \\
 & - \frac{L_gR_p}{C_b} - \frac{R_p}{C_{gd}}(L_g + L_v) - R_1r_oR_p \\
 & \times (1 + g_mR_g) + \frac{1}{C_bC_{gd}\omega^2}(r_o + R_p) \\
 & + L_gL_p\omega^2(R_1 + R_g + r_o) \\
 & + L_gL_v\omega^2(r_o + R_1 + R_p) + L_vL_p\omega^2(R_g + r_o).
 \end{aligned}$$

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