

A Tapered Cascaded Multi-Stage Distributed Amplifier with 370GHz GBW in 90nm CMOS

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Abstract—A tapered cascaded multi-stage distributed amplifier (T-CMSDA) has been designed and fabricated in a 90nm digital CMOS process. The amplifier achieves a 3-dB bandwidth of 73.5 GHz with a pass-band gain of 14dB. This results in a gain-bandwidth (GBW) product of 370 GHz. The realized zero-dB BW is 83.5 GHz and the input and output matchings stay better than -9dB up to 77 and 94 GHz, respectively. The chip consumes an area of 1.5mm by 1.15mm while drawing 70mA from a 1.2V supply.

Index Terms—CMOS DA, Cascaded Multi-Stage Distributed Amplifier, Tapering, Elevated Coplanar Waveguides.

I. INTRODUCTION

Wideband circuits find applications in various fields such as high speed links, broadband radio transceivers, high frequency instrumentation circuitry, high resolution radar and imaging systems. With the scaling of CMOS technology and transistor cutoff frequencies in excess of 100GHz, considerable research effort is invested in CMOS broadband circuits. CMOS is a low cost alternative to more exotic III-IV technologies that are currently the main option for millimeter-wave components. CMOS technology provides many advantages as flexibility in number and topology of active devices and disadvantages mainly related to the passive components on the lossy substrate. Mainstream CMOS technology does not provide additional options for RF and microwave circuits and this results in excessive conductive (series) and dielectric (shunt) losses in passive components. Also, lower intrinsic gain from the devices decreases the margin for modeling errors and requires careful prediction of device characteristics.

Here we present a new methodology to pick the optimal device size and topology for use in the distributed amplifier (DA). We map this device to the custom library of devices to find the closest match. Additional device modeling is performed to take into account specific topological layout issues in a multi-stage DA and to pinpoint the crucial traces for stability and gain roll-off prevention. This combination of concurrent device modeling and circuit design with careful custom layout optimization allows for an achievable large BW. To realize a high characteristic impedance, elevated transmission lines are used for the synthesized segments. Impedance tapering with filter-design based sizing mitigates the effect of gain droop at the high end of the frequency band. Design and measurement results of a prototype tapered cascaded multi-stage distributed amplifier (T-CMSDA) will be described.

II. PASSIVE ELEMENTS

With the scaling of CMOS technology, f_t and f_{max} of the devices have exceeded the 100-200 GHz range. Still, it is difficult to design wideband circuits that achieve the theoretical limits close to the cutoff frequency of the devices. This is mainly because of lossy passive elements that limit the performance of the active devices, and in the case of DAs, limit the BW through severe roll-off effects. This roll-off effect is seen in many wideband DA designs including [1]-[2]. The cutoff frequency of an artificial transmission line is determined by the inductance and capacitance of the segments ($f_c = \frac{1}{\pi\sqrt{LC}}$). These parameters are determined by the length of the segments as well as the size of the devices. To achieve a 50Ω transmission line at the input and output lines, the initial Z_0 needs to be considerably higher than 50Ω . This is because the segments get loaded by the transistor capacitances and therefore their impedance is lowered. As shown by [3] the required segment length which determines the BW can be derived as follows (assuming short segments):

$$l_{seg} = \frac{C_{tran} \times v_{line} \times Z_{line}}{\left[\frac{Z_{line}}{Z_0}\right]^2 - 1} \quad (1)$$

where C_{tran} is the loading capacitance of the transistors, v_{line} is the wave velocity in the line and Z_{line} is the initial impedance of the line that would lead to a $Z_0=50\Omega$. As shown in Fig. 1, it is apparent that we require high impedance line segments for the transmission lines, so that the limiting components in the BW of the amplifier are determined by other factors. Accuracy and issues with pinpointing the exact value of inductance with the extra layout-dependent leads limits the use of spiral inductors for high BW DAs.

CMOS transmission lines, on the other hand, can be accurately modeled. Our approach has been to use a set of

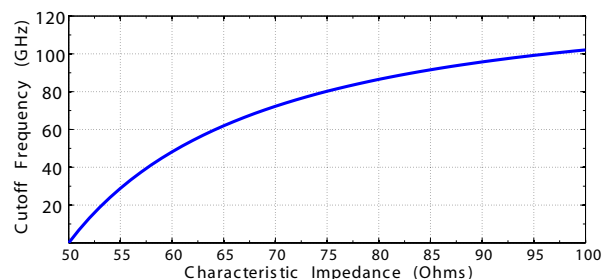


Fig. 1. Line bandwidth limitation due to the initial Z_0 of transmission line.

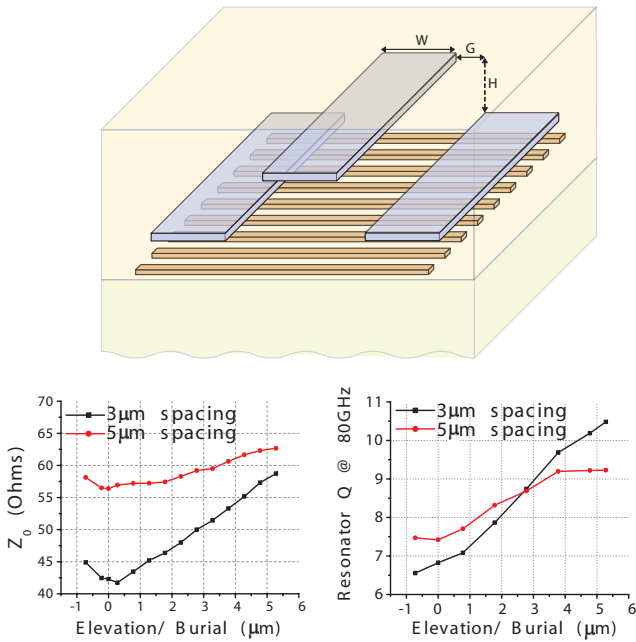


Fig. 2. Conceptual layout of the shielded elevated CPW (SE-CPW) with simulated Z_0 and resonator Q of elevated lines without shields.

measurement based data to calibrate the loss parameters in the EM simulator and to verify this with measurements from various passive components (transmission lines, inductors and transformers). This allows for dependable data from the EM solver and makes accurate modeling of transmission lines possible. However, achieving high impedance transmission line on-chip remains to be a challenge. For a coplanar waveguide (CPW), the impedance is a function of $\frac{W}{W+2G}$ where W is the line width and G is gap spacing. The line impedance decreases with the increase of this ratio and is in the 30-80 Ω range for silicon CPWs. Higher or lower impedances are difficult to achieve with conventional CPW lines. For low- Z_0 lines, the wide signal conductor and narrow gap increase the series losses that result from high current density at the edges. For high- Z_0 lines, the opposite conditions result in high shunt losses from substrate penetration.

To alleviate the loss issues while achieving a reasonably high impedance, we propose the use of elevated transmission lines in which the signal line is situated higher than the ground traces in the CPW [6]. Lower loss is achieved as more fields are “captured” by the ground line and also the current is more evenly spread across the signal conductor. To further reduce losses, shielding metal filaments could be added underneath the transmission line. This would “slow down” the wave and hence require shorter length lines for the same inductance. Line elevation on the other hand, leads to minor decrease in the effective dielectric constant of the line. Although the two effects are opposite, the final wave-velocity could remain lower than a conventional CPW with the right choice of elevation and spacings. Simulation results of the un-shielded elevated line are shown in Fig. 2. In the simulations, both positive and negative elevation (burial) values for a fixed signal conductor height have been shown. Resonator Q has been chosen for

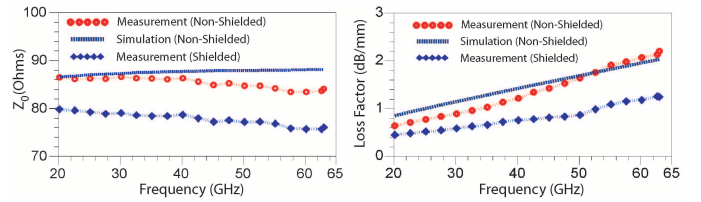


Fig. 3. Measured Z_0 and loss of the elevated line with and without shielding in 90nm digital CMOS process.

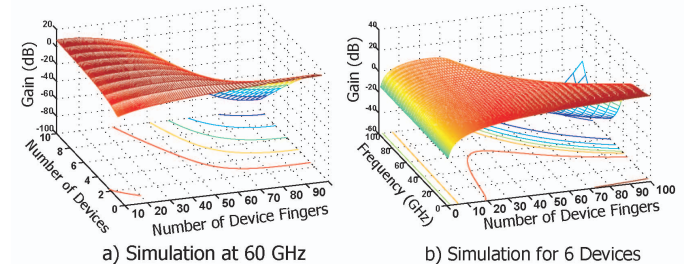


Fig. 4. Simulated DA gain (a) at 60GHz with varying device size/ number of devices and (b) for 6 devices with varying frequency/ device sizes.

loss comparisons since it takes the effect of velocity change into account. As shown in this figure, for the two spacings of 3 and 5 μm the line impedance increases with the loss decreasing. For larger spacings the required impedance in the order of 90-100 Ω will be achieved. This also shows that even for impedances in the range of 40-70 Ω where conventional CPW is adequate, elevated CPW could provide higher quality factors.

Fig. 3 shows the measured characteristics of the elevated CPW lines. Measurements were performed on both the shielded and non-shielded cases. The Z_0 of SE-CPW is slightly lower due to the extra capacitive loading from the metal filaments.

III. DEVICE SIZE AND TOPOLOGY SELECTION METHODOLOGY

An issue concerning DA design in CMOS is the selection of the optimum device size. Conventional microwave DA design does not provide optimal design when applied to CMOS. This is because in CMOS technology, device sizing and exact topological layout (number of fingers) are free parameters and should be exploited for DA design. In order to exploit the extra degrees of freedom available in CMOS technology, we exported first-order scalable device model parameters into Matlab. Using this and also CPW line models that were extracted from measurements, parametric expression for the gain of a conventional DA stage was derived and optimized for a given bandwidth. The gain function has different sensitivities to various design parameters in our design space. For a well chosen line Z_0 and finger width, it is seen that device topology, number of devices and number of fingers are the three most significant factors determining the gain. For design topology, cascodes and common-source topologies are the two main candidates. The cascode device provides a higher stable gain at lower frequencies limited by a pole at approximately half the device cutoff frequency.

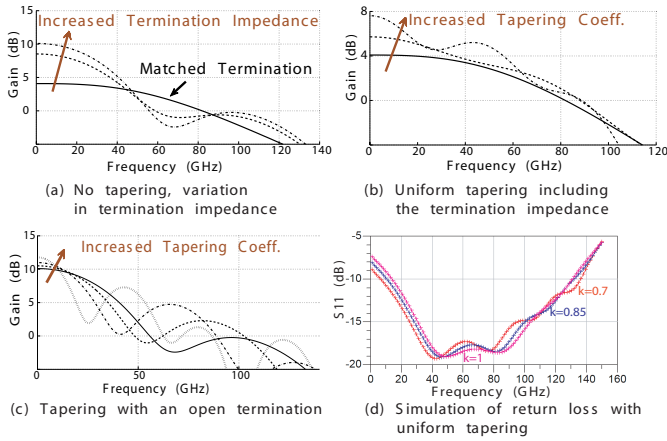


Fig. 5. Simulated gain with (a) no tapering, (b) uniform tapering, (c) tapering with an open termination and also (d) the return loss from uniform tapering.

Fig. 4 shows the simulated gain of the DA in terms of number of devices, number of device fingers (finger width=1.2 μ m) and frequency. As these device models are approximate scalable models, after this step, the closest transistors to the candidates are chosen from the custom library and accurate, in-house models are used in the optimization process. It is observed that the gain is not constant for a constant “total width” of all devices. Nor is the sensitivity to each parameter constant for different decompositions of total width. Larger devices provide more gain with the same total width but are more sensitive to various parameters as well as showing more parasitics in their structure. For our design, the 40 μ m cascode device provides the optimal gain with 3-5 devices (depending on the required BW).

For cascode devices, the maximum stable gain is higher at lower frequencies but is limited by the parasitic pole. This could be somewhat remedied by placement of a series stub between the two devices [9]. Layout is extremely important for cascode devices, specifically with regards to the impedance at the gate of the cascode device. Careful layout and EM simulations were performed to capture the inductive part at the gate of the cascode to reduce it below what is safe for stability.

IV. TAPERING IN THE TRANSMISSION LINE SEGMENTS

The multi-stage DA has the advantage of having an extra degree of freedom in the choice of internal idle termination impedances. For a cascade of single stage DAs, [4] suggests open terminations for maximizing the gain. However, this comes with the cost of limitations on the BW from destructive combinations of forward and backward going signals and limits the number of stages. This results in poor input and output return losses as well as high noise figure. Also, the idle termination technique cannot be used on the input and output lines since the return loss is not acceptable.

We propose tapering the impedance of the line segments which can also be used on the input and output sections if the tapering coefficients are not very large. In this tapering, the line segment impedances is tapered starting from the load/source impedance of 50 Ω and increasing by \sqrt{K} (the

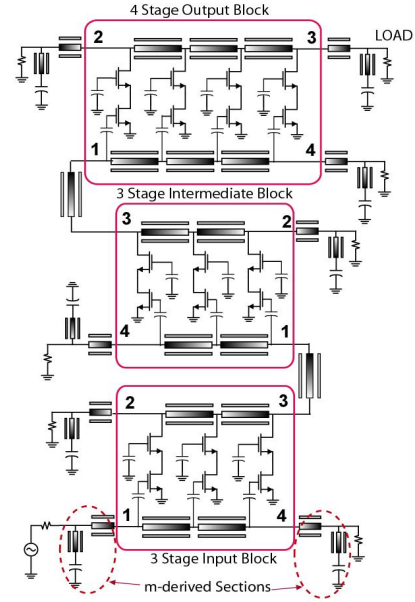


Fig. 6. Schematics of the T-CMSDA.

tapering coefficient). This could be achieved by the change in line lengths (and hence in the inductances) or by varying the spacing/height of the elevated-CPW to change the Z_0 of the transmission lines. Here, we have emphasized using the change in line lengths. The active elements are kept identical in size and hence reflections occur. Fig. 5 illustrates the effect of tapering by first order simulations. Here, a simple model of DA neglecting higher order reflections, that are mitigated by loss, has been utilized to provide intuitive results. Fig. 5a shows the effect of having no tapering and terminating a DA drain line with various large loads. Fig. 5b uses tapering all the way to the terminating resistance (with the same coefficient). Fig. 5c uses an open termination with various tapering coefficients for the segments. Here, there is a relatively large mismatch between the last segment and the termination element. In Fig. 5d, first order circuit simulations have been used for the case of uniform tapering (as in part b of this figure) to verify possible application in the input and output stages. As observable in this figure, tapering provides means of extending the gain while having control over different local gain variations (similar to conditions with pole/zero placement).

Filter-design approaches have been used to size the segments in the DA [5]. Poles could be placed closer to the imaginary axis in the complex plane to provide local peaks in the vicinity of gain roll-off frequencies. To achieve the required frequency response, both line segment sizes and input capacitance at the intersection nodes are varied. Series capacitors are used to control the equivalent input capacitance. A combination of filter-design based response selection (pole-placement) with the described tapering method is used to achieve BW extension by mitigating the severe gain roll-off at the higher end of the band.

V. EXPERIMENTAL RESULTS OF THE T-CMSDA

The schematic of the T-CMSDA is shown in Fig. 6. The chip is implemented in a 90nm 1P7M digital CMOS process.

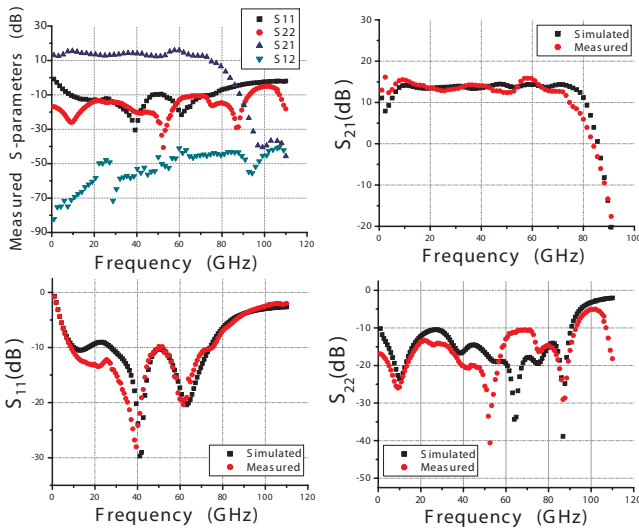


Fig. 7. S-parameter simulation and measurements of the T-CMSDA.

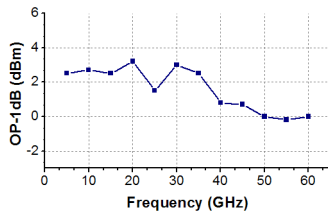


Fig. 8. Output compression point measurements of the T-CMSDA.

A large series capacitor is used to AC-couple the input of the amplifier for low frequency stability and biasing issues. M-derived matching sections are used to improve matching to required impedances. Intermediate terminations as well as the input and output terminations are tapered (with different coefficients) according to the descriptions in section IV.

Measurements were taken directly using wafer probes. The measured s-parameters are shown in Fig. 7. The amplifier has an average pass-band gain of 14dB with a 3dB bandwidth of 73.5 GHz. The zero-dB bandwidth of the amplifier is at 83.5GHz. The S11 and S22 of the T-CMSDA below -9dB up to 77GHz and 94GHz, respectively. The GBW product of this amplifier is 370GHz. The zero-dB gain-bandwidth is 419GHz. The output referred 1-dB compression point is shown in Fig. 8. The output power remains higher than -0.2dBm up to 60GHz. The amplifier draws 70mA from a 1.2V supply. Comparison to other published CMOS DAs is given in Table I.

The chip micrograph is shown in Fig. 9. The chip consumes an area of 1.15mm by 1.5mm.

VI. CONCLUSION

A 73.5 GHz CMOS distributed amplifier was implemented in a standard digital 90nm CMOS process. The design consists of the proposed device sizing and topology optimization methodology, concurrent device level layout optimization and modeling, elevated CPW lines for high impedance on-chip transmission lines and impedance tapering with filter-based response synthesis (pole placement) on the input/intermediate/output lines for increased BW and

| Ref. | This Work | [2] | [1] | [7] | [8] |
|-------------------------|------------|--------------|-----------|------------|-------------------|
| Process | 90nm CMOS | 90nm RF CMOS | 90nm CMOS | 130nm CMOS | 0.18 μ m CMOS |
| GBW (GHz) | 370 | 190 | 157 | 136 | 394 |
| S21 (dB) | 14 | 7.4 | 7 | 9.8 | 20 |
| BW (GHz) | 73.5 | 80 | 70 | 43.9 | 39.4 |
| S11/S22 (dB) | -9/-9 | -10/-8 | -7/-12 | -14/-8 | -10/-20 |
| OP1dB (dBm) | 3.2 @20GHz | 6-8 | 10 | N/A | 6.5 |
| Vdd (V) | 1.2 | 2.4 | N/A | N/A | N/A |
| Power (mW) | 84 | 120 | 122 | 103 | 250 |
| Area (mm ²) | 1.72 | 0.72 | 1.28 | 1.5 | 2.24 |

TABLE I
COMPARISON TO OTHER PUBLISHED DISTRIBUTED AMPLIFIERS

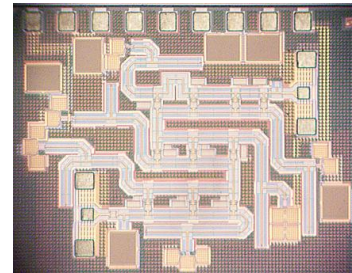


Fig. 9. Chip micrograph of the of the T-CMSDA.

immunity to gain roll-off. The fabricated amplifier achieves 390GHz/419GHz of -3dB/0dB GBW product. The whole circuit consumes 84mW power from 1.2V supply.

VII. ACKNOWLEDGEMENTS

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