

Broadband Variable Passive Delay Elements Based on an Inductance Multiplication Technique

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Abstract—A new technique for making broadband and variable passive delay elements is described. By introducing a variable inductance structure and using it along with available varactors, synthesized transmission lines are implemented with variable delay while maintaining a constant Z_o over the line bandwidth. Inductance tuning is realized through the effect of mutual inductance. As a demonstration prototype, a single unit cell and two cascaded unit cells were implemented in 90nm digital CMOS process. Delay values ranging from 14ps – 40ps were obtained from DC to 8GHz while maintaining matched condition over the bandwidth with delay variations of less than $\pm 5\%$. These delay cells could be used in broadband impulse-based beamforming systems to provide variable delays in each RF path.

Index Terms—Phase shifter, passive delay element, variable delay, synthesized transmission lines, inductance tuning, inductance multiplication.

I. INTRODUCTION

Delay elements are important building blocks of numerous circuits and systems such as broadband beamforming antenna arrays, delay locked loops, delay based oscillators, and equalizers. Accuracy, tunability and immunity to process-voltage-temperature variations are key performance metrics in designing delay cells.

Various forms of active and passive delay elements have been used previously [1]- [3]. In systems using active delay elements, the delay accuracy is maintained through a feedback system and accurate external reference. Active delay cells could be realized in small footprints but they dissipate power and have limited bandwidth whereas passive delay lines could be accomplished with high bandwidth and good accuracy determined by inductances and capacitances that are highly accurate compared to active delay elements.

The inductance value is mainly a function of lateral dimensions of an inductor which is determined by a precise lithographic process. Inter-digitated MOM (Metal-Oxide-Metal) finger capacitors using multiple layers of metals and exploiting intermediate via capacitances are quite precise. These structures are immune to process variation due to the large amount of inherent averaging done on small local capacitances in comprising the desired capacitor. Unlike active delay cells, passive elements are largely independent of voltage and temperature variations.

A new method to obtain broadband and tunable delay out of synthesized transmission lines based on an inductance multiplication technique is introduced in this paper. In section

II we discuss different types of passive delay structures. Section III focuses on the inductance multiplication technique. Implementation and measurement results are presented in section IV.

II. PASSIVE DELAY LINES

As shown in Fig. 1a, the most straightforward way to implement a delay element is to use a transmission line. To create a variable delay, multiple transmission lines of different length can be switched into the signal path. On-chip transmission lines are highly accurate, completely linear and very broadband. However they consume large amount of chip area, and are therefore too costly for commercial applications below 10GHz.

To decrease the size, artificial transmission lines can be used. In these synthesized transmission lines, lumped inductors and capacitors mimic the role of distributed inductance and capacitance in a real transmission line. The conventional way to make the delay of a synthesized transmission line tunable is by means of varactor loading (Fig. 1b). Varying the line capacitance changes the wave velocity and hence the delay ($T_D = \sqrt{LC}$) of the line. However this comes at the expense of changing the line's characteristic impedance ($Z_o = \sqrt{\frac{L}{C}}$). To maintain good return loss, delay variations of only a small fraction of the nominal delay is acceptable.

To overcome the Z_o variation problem, in [4] a variable capacitor is added in series with the inductor (Fig. 1c). By varying this capacitance, the effective reactance of the series LC circuit is altered. This effective reactance tunability compensates for the Z_o variation caused by the change of capacitance values in shunt varactors. Since in this technique a series LC network is emulating the effect of a variable inductor, its functionality is limited to a small bandwidth, and therefore is suitable for narrowband signals. To make an artificial varactor loaded transmission line work with wideband signals, the actual inductance value should be adjusted instead of the effective series reactance, as shown in Fig. 1d. If both series inductance and shunt capacitance are tunable, the delay could be varied while maintaining constant Z_o . In the next section, various techniques to realize tunable inductors are described and their advantages and disadvantages are highlighted.

III. INDUCTANCE MULTIPLICATION

Inductance is determined by the geometry of a closed path of current and the permeability (μ) of the surrounding

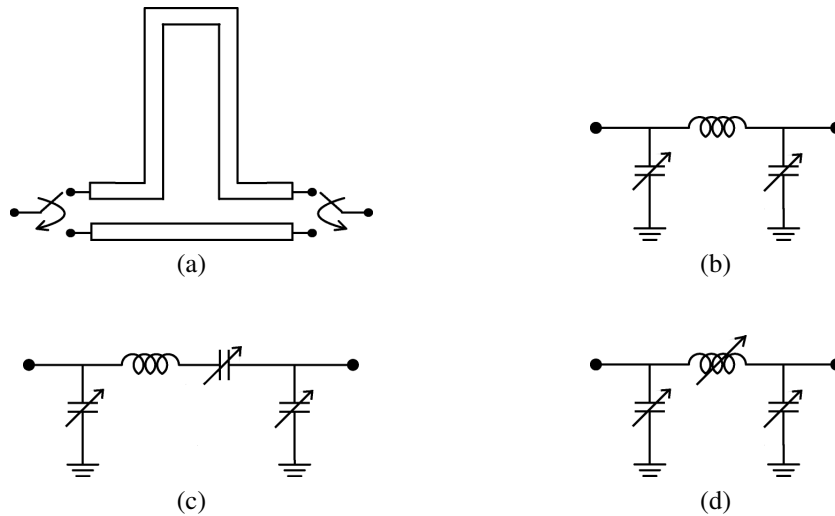


Fig. 1. (a) Switched transmission lines (large footprint). (b) Varactor loaded artificial transmission line (Z_o variation). (c) Modifying the effective series reactance by adding a varactor in series with the inductor (narrowband network). (d) Broadband solution for tunable synthesized transmission lines presented in this paper.

material. In traditional IC processing, magnetic materials of high permeability are not available and therefore the only way to change the self inductance of a single loop is to change the geometry, which implies that the path of the current or return current flow should be reconfigured. It is not trivial to change the geometry of a an inductor electronically and efficiently since switches incur substantial loss.

The other way to change the effective inductance is to change the net magnetic flux passing through a loop via the flux generated by another loop. This could be done via a transformer if the current passing through the secondary loop is controlled. As depicted in Fig. 2, if the current passing through the secondary is a multiplicative copy of the primary current ($I_2 = n \cdot I_1$), then the effective inductance seen through the primary is $L_{eff} = L_1 + n \cdot M$. Therefore either the secondary current or the mutual inductance should be adjustable in order to have a variable inductance at the primary.

In Fig. 3 several methods to change the magnetic flux of the primary loop are depicted. In Fig. 3a-c, signals are single-ended, and therefore an input balun is used to convert the signal from single-ended to differential and to produce a copy of the current flowing in the primary. A multiplication of this current will be routed into the secondary to change the net magnetic flux crossing the primary loop.

The structure depicted in Fig. 3a uses a current amplifier to adjust the current at the secondary. In this structure, the secondary current could be varied over a wide range but it comes at the price of DC power consumption and limited bandwidth due to the fact that the operation frequency should be reasonably below $f_t/(N + 1)$. Furthermore, if the current amplifier is implemented with reasonable power consumption, its input impedance ($1/g_{m1}$) will be high and it needs a matching network to lower it down to the characteristic impedance of the top path. Otherwise if the impedance looking into the current amplifier is much higher than the impedance of delay cell (Z_o), the voltage will appear mostly on the current amplifier side rather than at the input of the delay cell. This

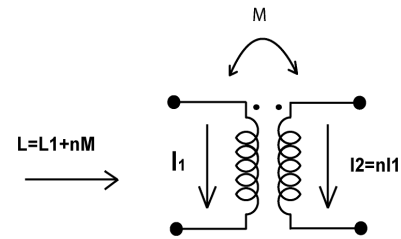


Fig. 2. Inductance tunability, net magnetic flux crossing a loop is altered via the flux generated by another loop.

results in a significant attenuation for the signal that appears at the output of the delay cell.

Fig. 3b demonstrates another structure that modifies the magnetic field induced in the primary by changing the number of turns of the secondary inductor. Since $M = k\sqrt{L_1 \cdot L_2}$, changing the inductance of the secondary modifies the mutual inductance and as a result the effective inductance of the primary loop. Unlike the previous configuration, this structure does not consume any DC power, however large inductance in the bottom path lowers the bandwidth. Furthermore, changing the inductance at the bottom path alters its impedance, which loads the input balun. Variable loading results in variable voltage levels that appears at the input of the delay cell, and this causes the signal to experience variable gain from input to the output depending on the inductance needed for each delay setting.

In the structure shown in Fig. 3c, the magnitude of the current and the inductance of the secondary loop stay unchanged. However with the aid of switching network, current will change direction in the secondary and in one switching condition it totally bypasses the secondary and directly goes into the termination resistor. Hence the effective inductance of the primary will take on values of $L_1 - M$, L_1 , and $L_1 + M$. If the mutual inductance is designed to be half the value of self inductance, then the effective inductance

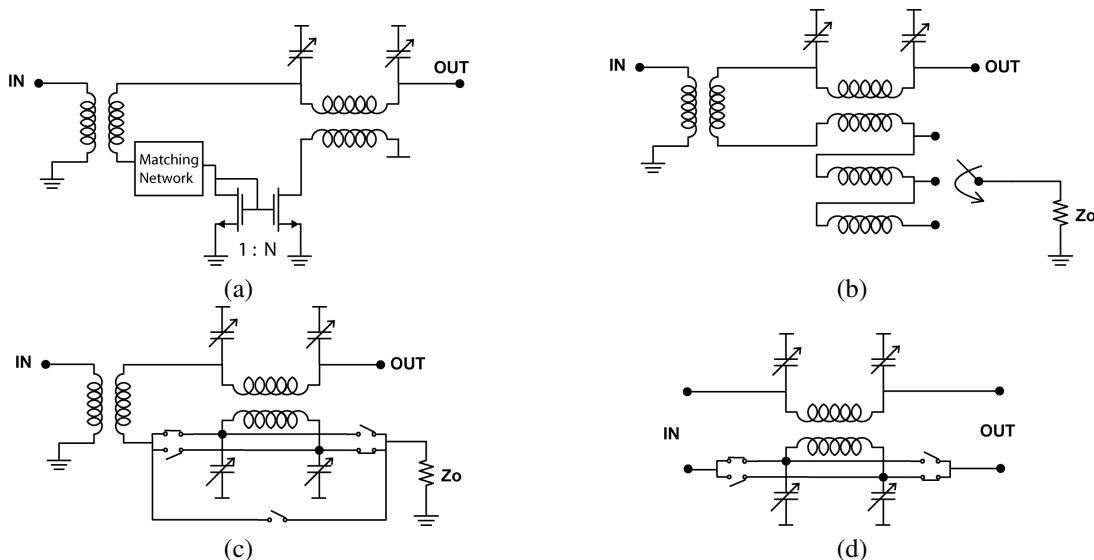


Fig. 3. Four different ways to realize inductance tuning: (a) Using a current amplifier, (b) varying the mutual inductance, or by rerouting the current in the secondary in a (c) single-ended or (d) differential manner.

looking into the primary will have a ratio of $L_{max}/L_{min} = (L + M)/(L - M) = 3$. To have a constant Z_o , the same tuning range should apply to the capacitors: $C_{max}/C_{min} = 3$, yielding a delay variation factor of three while maintaining constant Z_o , which is considerably higher than the achievable delay variation of a varactor loaded synthesized transmission line.

The circuit in Fig. 3c has no DC power consumption, and the bottom path does not impose bandwidth limitations on the top (delay) path, and there are no matching requirement in the bottom path. But still an input balun is used to convert the signal from single-ended to differential. This means that under the desired matched condition, half the signal power will be lost. On the other hand, if a differential delay line is adopted, with a configuration illustrated in Fig. 3d, a fully symmetric structure is realized with the same L_{max}/L_{min} ratio as the previous single-ended version. The effective inductance can take on two values ($L - M$ and $L + M$) in the differential version rather than three values ($L - M, L, L + M$) obtained in the single-ended configuration. Being fully differential and not having the 3-dB inherent loss make this structure the preferred one. The next section describes the implementation and experimental results of this differential delay element.

IV. IMPLEMENTATION AND EXPERIMENTAL RESULTS

The delay element is a fully differential LC structure. As depicted in Fig. 3d, inductors are realized through the primary and secondary inductances of a 1:1 transformer. A switching network changes the direction of current flow in one of the loops and varies the effective inductance from $L - M$ to $L + M$. Transformers are overlaid structures using two top metal layers and they are designed to have a coupling factor of $k = 0.5$. Varactors are realized by a bank of switched capacitors in which interdigitated MOM finger capacitors are switched in and out of the signal path depending on the required delay

settings. $W = 50\mu\text{m}$ wide NMOS transistors with 7Ω of on-resistance was used as a switch. This transistor's parasitic capacitance was absorbed in the design.

The self-inductance of each loop of the balun is 300pH and capacitors are chosen to have differential characteristic impedance of 50Ω . The worst case cut-off frequency ($\omega_c = 2/\sqrt{LC}$) is around 18GHz that is associated with the high delay mode cut-off.

For demonstration purposes, a unit-cell and two cascaded unit cells were fabricated in 90nm CMOS process (Fig. 5). For the cascaded version, the first switching network was placed in the bottom path and the second one in the top path to maintain the symmetry. To be able to do single-ended measurements, two baluns were added at the input and output of the structure and their effects were de-embedded after the measurement.

Measurement results of fabricated delay lines are shown in Fig. 4. In a single delay cell structure, by moving from a low delay mode to a high delay mode, T_D increases by a factor of 3, or from 7ps to 20ps . For the cascaded version, delay values of 14ps , 27ps and 40ps are obtained for low-low, low-high and high-high delay modes. Since both the inductance and capacitance change correspondingly, Z_o stays constant and the structure is well-matched while the delay varies significantly. Delay variation for this implementation is less than $\pm 5\%$ up to 8GHz for the highest delay mode.

V. CONCLUSION

An inductance multiplication technique for making broadband and variable passive delay elements is described. By varying both the inductance and capacitance of a synthesized transmission line, the delay value can be altered significantly while keeping the Z_o constant. Two prototypes, a single unit cell and a cascade of two unit cells were implemented in 90nm digital CMOS process. Delay values ranging from 14ps – 40ps were obtained from DC to 8GHz while maintaining matched condition over the bandwidth.

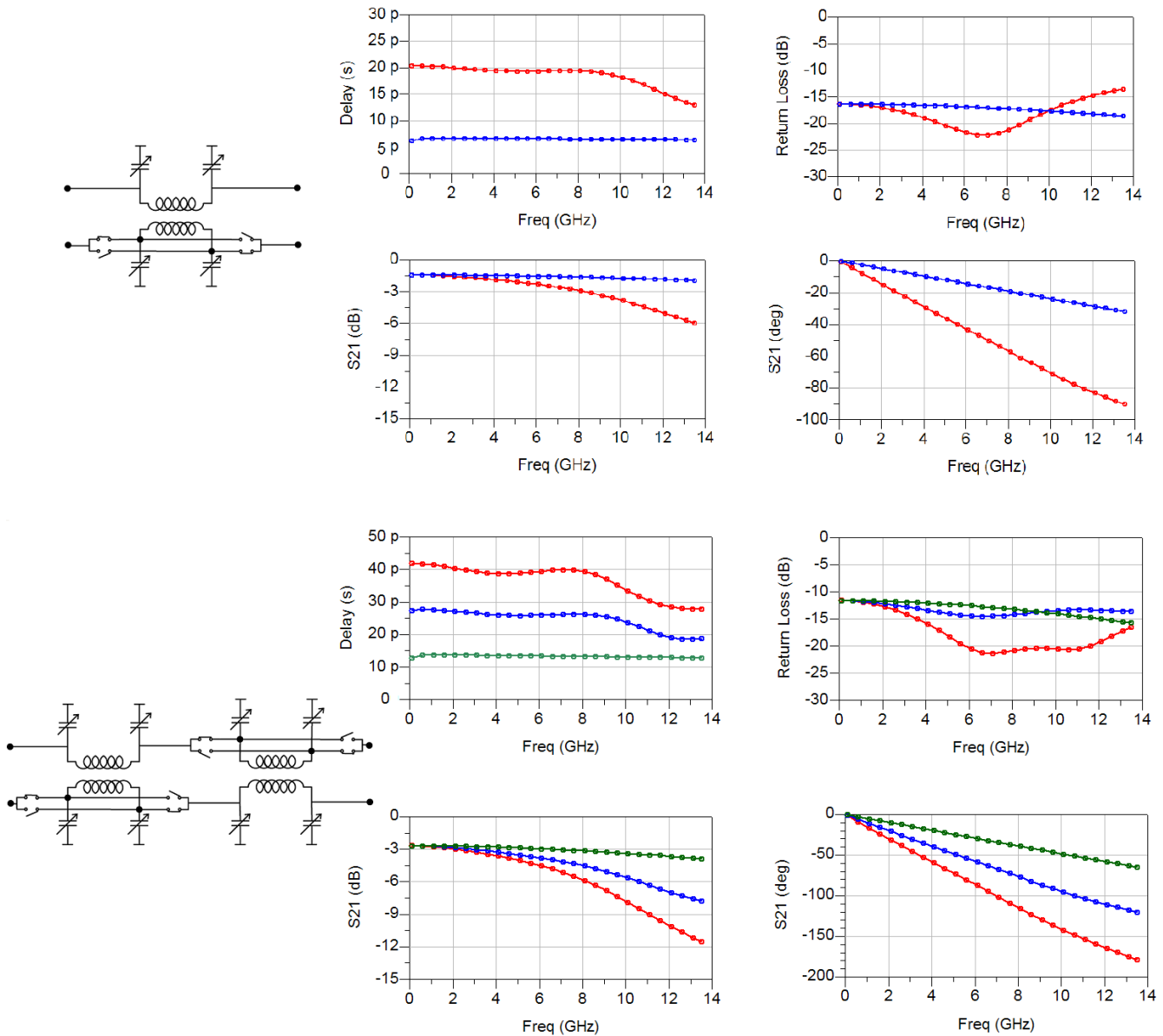


Fig. 4. Performance results of a unit-cell delay element (top) and two cascaded delay cells (bottom).

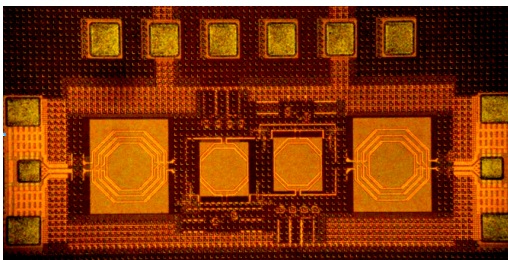


Fig. 5. Die Microphotograph

VI. ACKNOWLEDGEMENT

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