

# A 2.5mW Inductorless Wideband VGA with Dual Feedback DC-Offset Correction in 90nm CMOS Technology

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**Abstract-** A low power inductorless wideband variable gain control amplifier (VGA) for baseband receivers has been designed in a standard digital 90nm CMOS technology. The VGA was implemented using four-stage modified Cherry-Hooper amplifier with a dual feedback DC-offset canceling network, which simultaneously corrects DC offsets and extends bandwidth without a peaking inductor resulting in saving the chip space significantly. The proposed VGA has been measured using on-chip probing and achieves a 3-dB bandwidth of more than 2.2GHz with 60dB gain tuning range. It consumes 2.5mW through a 1V supply (excluding the output buffer), and occupies only 0.01mm<sup>2</sup> active area.

## I. INTRODUCTION

Recent advances in nanometer CMOS technology have made it possible to build low-cost radio transceivers operating around 60GHz mm-wave frequencies as well as multi-Gb/s wireline receiver systems. Fig. 1 shows a block diagram of a 60GHz receiver front-end. A baseband VGA is an essential building block to maximize the dynamic range of receiver systems and adjust the received signal amplitude. To be practical for high-volume, low-cost applications, the chipset should achieve as high an integration level as possible and avoid using on-chip inductors. A VGA with wide bandwidth, large gain tuning range, DC offset correction, small chip area, and low power consumption is highly desired.

VGA design is faced with many challenges including bandwidth, flat gain response over PVT, high linearity, large gain tuning range, and DC-offset correction while keeping the chip area and power consumption minimal. Several CMOS VGAs have been reported recently [1]-[5]. Many of them are operating below 1GHz [2]-[5] which is not suitable for this application. On-chip peaking inductor has been utilized to extend the bandwidth up to 2GHz but occupies a large chip area [1]. In this paper we present a novel design of an inductorless differential VGA using dual negative feedback network to cancel the DC-offset and extend the bandwidth through peaking effects with small chip area. The paper is organized as follows, the system architecture of the proposed VGA is illustrated in Section II and the detail design approach of the VGA are described in Section III. The measurement results are shown in Section IV. Finally the paper concludes with a brief summary in Section V.

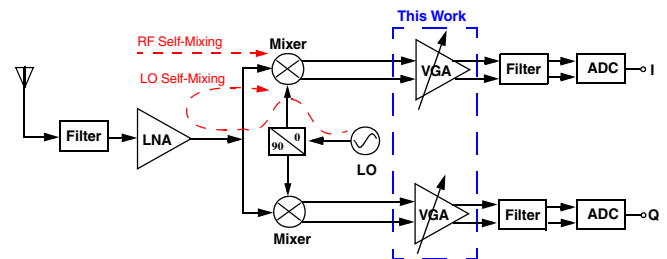


Figure 1. Block diagram of a 60GHz receiver front-end.

## II. VGA SYSTEM ARCHITECTURE

Fig. 2 depicts the system architecture of the proposed variable gain amplifier using differential topology for better noise performance. It consists of a high-pass filter, a four-stage modified Cherry-Hooper amplifier gain cell, a DC-offset cancellation network, and an output buffer.

A 100Ω resistor is placed across the differential inputs to provide standard 50Ω input impedance matching for RF testing. The high-pass RC filter is designed to eliminate the input offsets from preceding stages, such as self-mixing offsets from the LNA, Mixer, and LO as shown in Fig. 1 and provides the desired input DC level for the input stage of VGA1 as shown in Fig. 2. The four-stage VGA provides wide gain tuning range, namely having sufficient voltage gain for small signal inputs and attenuating the signals when the signal levels are strong enough to saturate the system in high gain mode. The offset cancellation network is composed of a RC low-pass filter to extract the dc-offset voltage due to device mismatch of the four-stage VGA, and dual negative feedback amplifiers to correct the offset and provide peaking to extend the bandwidth simultaneously. A high-speed  $f_T$  doubler output buffer is employed at the output for testing purposes only.

## III. CIRCUIT DESIGN APPROACH

### A. VGA Gain Cell

The VGA gain cell is structured as a modified Cherry-Hooper amplifier [6] as shown in Fig. 3(a). Compared to a traditional Cherry-Hooper amplifier, the resistive shunt-feedback  $R_f$  is replaced by a pair of PMOS transistors M3a/M3b working in the triode region, acting as a tunable resistance by

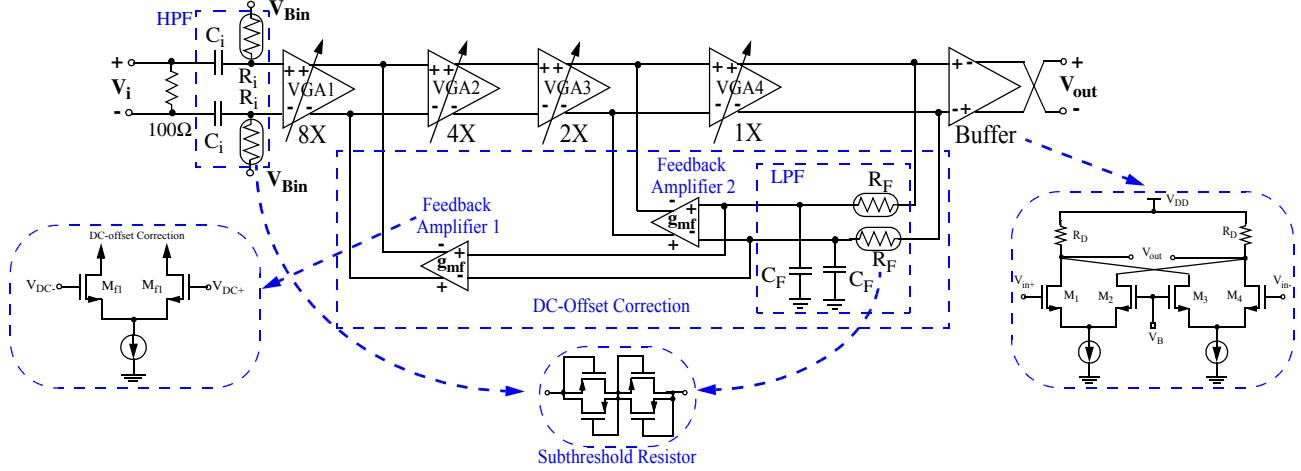


Figure 2. Proposed VGA architecture and subcircuit schematic.

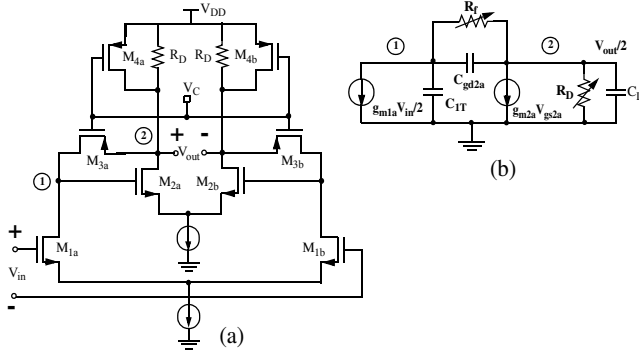


Figure 3. Modified Cherry-Hooper amplifier gain cell, (a) schematic, (b) simplified small signal half circuit.

a control voltage  $V_C$  at the gate. However, there are two major limitations in the Cherry-Hooper amplifier. First, it requires large voltage headroom to make all transistors work in the saturation region, which makes it difficult to operate under a 1V supply. A low-threshold voltage process is employed for all CMOS transistors to relax the voltage headroom problem. Furthermore, the minimum gain is limited by  $R_D$  which normally is a large fixed value. Therefore, PMOS transistors  $M4a/M4b$  with a control voltage  $V_C$  are added in parallel with  $R_D$  to lower the gain when the input signal is too strong, consequently increasing the gain tuning range.

From the simplified small signal half circuit as shown in Fig. 3(b), the differential small signal gain  $A_v$  of the gain cell is given by,

$$A_v = A_{v0} \frac{1 - s(C_{gd2a}/g_{m2a})}{s^2 B(R_f/g_{m2a}) + sD + 1} \quad (1)$$

$$B = C_{1T}C_{gd2a} + C_{1T}C_L + C_{gd2a}C_L \quad (2)$$

$$D = C_{gd2a}R_f + C_{1T} \frac{R_f + R_d}{g_{m2a}R_d} + \frac{C_L}{g_{m2a}} \quad (3)$$

where  $A_{v0} = g_{m1a}R_f$  is the DC gain of the gain cell if  $g_{m2a}R_f \gg 1$ ,  $g_{m2a}R_d \gg 1$ , and  $R_d \gg R_f$ .  $C_{1T}$  is the total parasitic capacitance at node 1.  $C_L$  is the total load capacitance at the output node 2.

To achieve wider bandwidth, an inductive load is widely used [1,8] to resonate the load capacitance at the cost of large chip size. A cascode structure with active inductive load is also employed [3,7] to extend the bandwidth. Besides the voltage headroom problem for cascoded transistors, this technique requires an extra high bias voltage for active inductors.

### B. DC-Offset Correction Network

There are two options for DC offset correction: interstage AC coupling high pass filter (HPF) in feedforward path and low pass filter (LPF) in feedback path. In this design, both filters have been utilized based on rejecting very low frequencies using sub-threshold transistors to emulate very large resistor reducing the chip size [2]. The input-stage HPF with a lower cut-off frequency of 200kHz blocks the offsets from preceding stages and provides correct bias for VGA1. Several subthreshold PMOS transistors are cascaded to realize a 1.6MΩ resistance and a finger capacitance of 0.5pF is implemented for the trade-off between input offsets blocking and settling time. The LPF with a lower cut-off frequency of 500kHz in the feedback path detects the DC information from the output of VGA4 and connect to a negative feedback transconductance amplifier  $g_{mf}$  to generate a correction current to the input of VGA chain.

Most of the reported dc-offset canceling circuits in the feedback path use a single feedback amplifier to correct the offset error only at the input stage [1], [3-7]. However, for

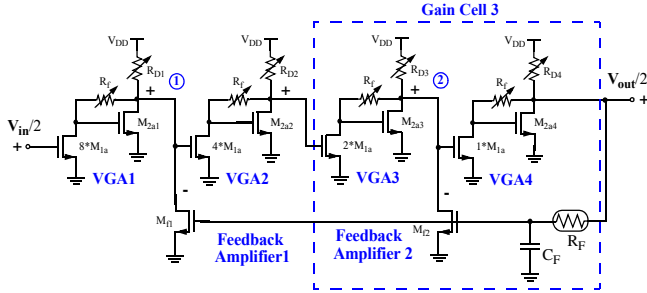


Figure 4. Simplified VGA half circuit with dual-feedback offset correction.

the cascaded VGA with high gain of each stage, the offsets at the internal stages not only limit the voltage swing for the following stages but also may cause saturation before signals reach the output.

The proposed VGA employs two techniques that substantially increase the bandwidth without compromising voltage headroom, chip area and provide inter-stage offset correction. First, the dominant pole of the Cherry-Hooper amplifier is located at the drain of transistor  $M_{2a}$  as shown in Fig. 3 and is determined by output load capacitance  $C_L$ , which is approximately given by  $g_{m2a}/C_L$ . Inversely scaling [7] the input transistor sizes of each VGA cell by a factor of two reduces the load capacitance  $C_L$  of the next VGA stage and results in broadening the overall bandwidth of the VGA and reducing the power consumption without degrading noise and offset performance. Second, the second feedback amplifier of the dual-feedback dc-offset cancelling network acts like active negative feedback loads connecting between VGA3 and VGA4. It combines VGA3 and VGA4 into a gain-cell3 with a higher GBW [8] as shown in Fig. 4. Fig. 5 shows the simulated frequency responses with different sizes of the feedback transistor  $M_{f2}$ . By adjusting the size of the feedback transistor  $M_{f2}$ , the peaking of the VGA can be controlled to balance the trade-off between GBW and flatness.

Using this gain peaking technique, the overall gain-bandwidth product is increased by approximately 70% with little extra area and power, and the inter-stage offsets can be cancelled by the second feedback amplifier with overall offset correction improvement of 5% compared to conventional single-feedback amplifier correction circuitry.

#### IV. MEASUREMENT RESULTS

The proposed VGA was fabricated in 90nm digital CMOS technology and measured using on-chip probes. Fig. 6 shows the die micrograph of the chip. The VGA including output buffer occupies only  $270\mu\text{m} \times 50\mu\text{m}$  and the total chip area with pads is  $1.0\text{mm} \times 0.7\text{mm}$ .

Fig. 7 shows the measured frequency response with control voltage  $V_C$  ranging from 0V to 0.9V in 0.1V steps. The mea-

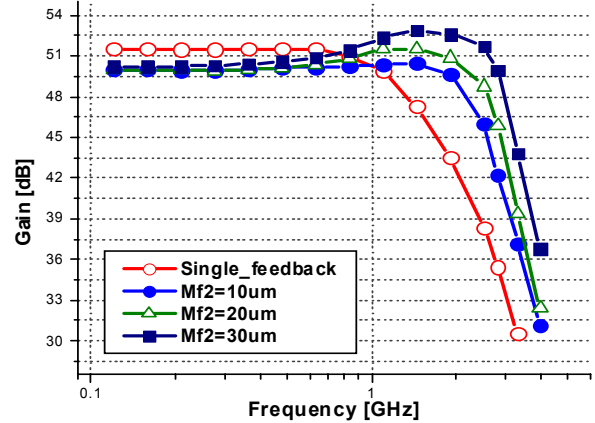


Figure 5. Simulated frequency response with different  $M_{f2}$  sizes.

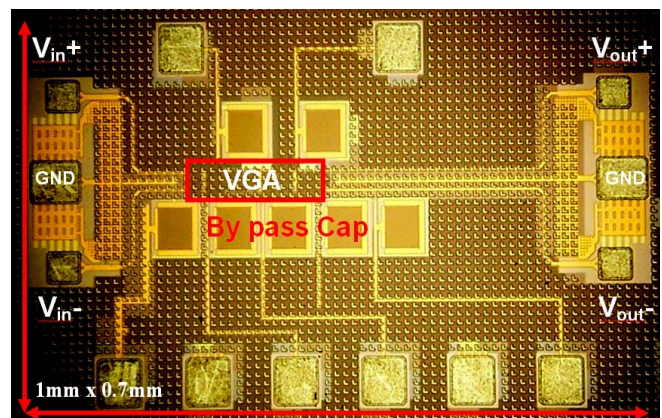


Figure 6. Die micrograph of the VGA.

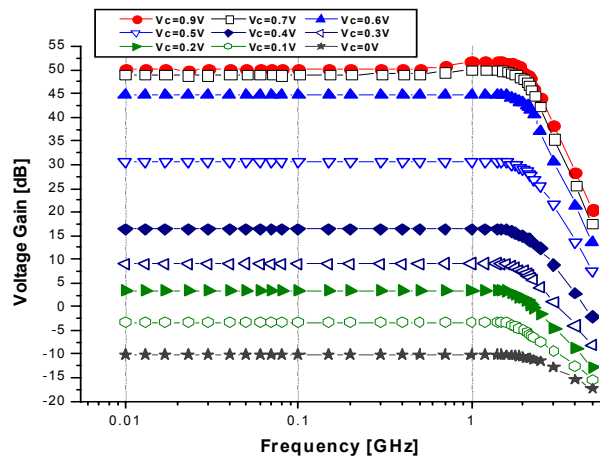


Figure 7. Measured frequency response vs. various control voltage  $V_C$ .

asured voltage gain varies from -10dB to 50dB, and the upper 3-dB bandwidth is 2.2GHz. The measured input 1dB compression point (IP-1dB) and voltage gain as a function of control voltage  $V_C$  are plotted in Figure 8, revealing input P-1dB of -13dBm at -10dB minimum gain, and -55dBm at

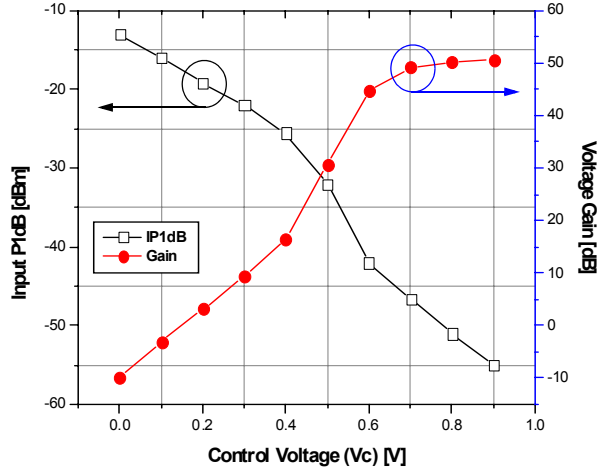


Figure 8. Measured input P-1dB and voltage gain vs. various control voltage  $V_c$ .

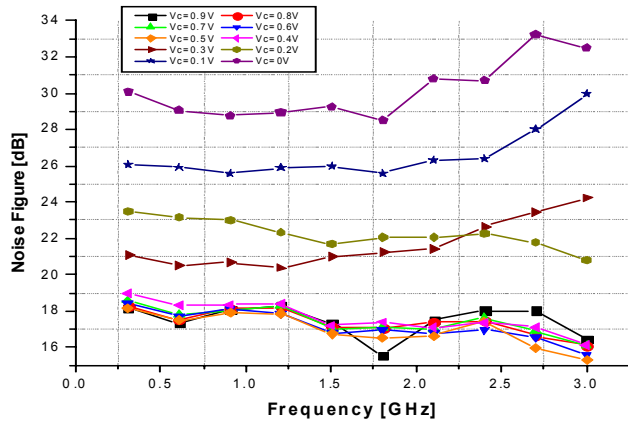


Figure 9. Measured noise figure response vs. various control voltage  $V_c$ .

50dB of maximum gain. Fig.9 shows a noise figure of 17dB with control voltage  $V_c$  from 0.4V to 0.9V and 30dB noise figure with control voltage  $V_c$  of 0V.

TABLE I MEASURED PERFORMANCE OF REPORTED VGAs

References	[1]	[2]	[3]	[4]	[5]	This work
Process	0.18 $\mu$ m CMOS	90nm CMOS	0.18 $\mu$ m CMOS	0.18 $\mu$ m CMOS	0.35 $\mu$ m CMOS	90nm CMOS
BW (GHz)	2	0.1	0.9	0.018	0.02	2.2
Gain (dB)	-16~34	13.5~67.5	-39~55	-8~32	-30~50	-10~50
IP-1dB (dBm)	N/A	-8	-11~-59	N/A	N/A	-13~-55
NF (dB)	N/A	43.2	6.8~N/A	N/A	30	17~30
Power (mW)	40	13.5	11.4	11.6	7	2.5
Supply (V)	1.2	1.8	2.7	1.6~2.0	3	1
VGA area (mm <sup>2</sup> )	0.26	0.55	0.19	0.56	0.289	0.01

Table I summarizes the measured performance of the proposed VGA, which achieves a 3-dB bandwidth of 2.2GHz and 60dB gain control range. The VGA dissipates 2.5mA under a 1V power supply and the output buffer uses 8.5mA current to drive the output. Due to application-specification requirements, it is unfair to compare to other VGAs. However, we list the performance of reported VGAs with this work to highlight favorable aspects of the design.

## V. CONCLUSION

A novel dual feedback DC-offset correction network is introduced as an inductorless solution for VGA system in baseband receivers and has been implemented and measured successfully in ST90nm CMOS technology. The VGA has achieved small chip size and low power consumption. The VGA achieves 2.2GHz bandwidth with 60dB gain tuning range and consumes only 2.5mW through a 1V power supply.

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