29.2 A 2GHz 52µW Wake-Up Receiver with -72dBm Sensitivity Using Uncertain-IF Architecture

Nathan M. Pletcher, Simone Gambini, Jan M. Rabaey

University of California, Berkeley, CA

A wake-up receiver (WuRx) is used in wireless sensor networks (WSN) to detect wireless traffic directed to a node's receiver and activate it upon detection, improving network latency and energy dissipation by maximizing data transceiver sleep time. The always-on nature of the WuRx sets a power dissipation floor for the entire system. In realistic WSN scenarios, the adoption of a WuRx leads to energy savings only if it can be realized with about 50µW of power dissipation [1], testing the limits of low-power receiver design. While diode detectors provide for the simplest detector structure, such receivers are strongly gain-limited due to the thresholding effect of the nonlinear detector [2] and adding gain at RF to improve sensitivity only increases power consumption. A more attractive approach is to adopt a heterodyne architecture, where the extra gain needed for robust energy detection can be obtained at an intermediate frequency (IF) with a much lower power cost. However, a survey of previous receiver designs for WSN reveals that the power requirements of the required local oscillator (LO) exceed the total power budget of the WuRx [3,4].

In modern CMOS processes, the low quality of integrated inductors means that the impedance of on-chip resonant networks is considerably less than the input impedance of small transistors. In order to generate the LO with minimum power, this observation leads to the choice of a CMOS ring oscillator. Unfortunately, the poor phase noise and frequency accuracy of the ring oscillator typically prohibit its use as the LO. The receiver presented overcomes this fundamental disadvantage at the architectural level. The architecture is shown in Fig. 29.2.1, and can be considered superheterodyne with uncertain IF. The on-off keyed input RF signal is down-converted by the mixer and ring oscillator LO, which has been calibrated to lie within a known frequency range, in this case between 1.9 and 2.1GHz. After calibration the LO is allowed to free-run. Following broadband amplification across the IF bandwidth (BW_{IF}), the signal is subsequently converted to DC using envelope detection. Front-end filtering, performed by a passive structure based on high quality-factor (Q) MEMS resonators, is required to eliminate interfering signals that lie within BW_{IF} of the desired channel. The use of a low quality ring oscillator to generate the LO, combined with wideband IF amplification instead of tuned RF gain, results in major power savings. Since the envelope detector converts any input frequency to DC, the IF need not be precisely defined. Furthermore, by realizing large gain in the receive chain, the noise contribution of the envelope detector is reduced, and the receiver sensitivity improved compared to previous work [2]. For the scheme to work, it is important for the imprecise LO to be digitally tunable to within $\pm BW_{IF}$ of the desired signal. Periodic re-alignment of the LO to a stable reference (available in the main data receiver) using well-known techniques [5] accommodates frequency offsets or drift due to temperature variation. The wide IF bandwidth allows this operation to be performed infrequently and with negligible average power consumption. A block diagram of the system is shown in Fig. 29.2.2.

To reduce power consumption, the entire receiver is optimized for low voltage and operates from a 0.5V supply. A single-ended dual-gate mixer topology is utilized to minimize LO drive requirements (Fig. 29.2.3). The on-chip matching network embeds a BAW resonator [6] to implement the front-end high-Q filter. A system-level noise calculation shows that noise performance in the mixer should be traded for higher conversion gain because overall noise figure is dominated by the envelope detector at the sensitivity limit. The mixer design is therefore optimized for low power and high conversion gain (+15dB in simulation).

The IF amplifier provides gain over the IF bandwidth from 1 to 100MHz and comprises a chain of 5 simple differential-pair gain stages. Three of the stages are implemented with a split-source topology in order to mitigate accumulated offset voltage without sacrificing AC differential performance. The use of resistive loads simplifies biasing and provides reasonable gain using minimal voltage headroom. Each stage provides 8dB of gain for optimal gain-bandwidth product. The IF amplifier is ac-coupled to the mixer, causing a small dead band ±1MHz around the LO frequency, but this is unlikely to lie directly on the input frequency and the LO could be re-calibrated if necessary. Following the IF amplifier, a differential-input envelope detector uses subthreshold FETs to perform the final downconversion to DC with a bandwidth of about 400kHz.

The digitally-tunable LO is a current-starved ring oscillator using CMOS inverters for both the ring and LO buffers (Fig. 29.2.4). Five bits of frequency tuning are programmable through an on-chip serial interface. The tuning range of the oscillator is determined using Monte Carlo simulations to ensure that the frequency may be set in the desired range across process and temperature variation. Figure 29.2.4 shows the measured oscillator frequency versus temperature, illustrating that the frequency can always be tuned within the range.

As pictured in Fig. 29.2.7, the prototype receiver was fabricated in 90nm CMOS with MIM capacitors, occupying an active area of approximately 0.1mm^2. The normalized gain response of four different chips after LO calibration is shown in Fig. 29.2.5, along with measured $|S_{11}|$ for a typical sample. Each die displays a slightly different frequency response due to natural variation in LO frequency, and hence different image frequencies landing within the IF bandwidth. The gain response quantifies the receiver's blocker tolerance, since selectivity depends only on the ability of the front-end filter to attenuate interferers. Figure 29.2.6 displays the measured BER of the receiver for different data rates; at 100kb/s the sensitivity for 10^{-3} BER is -72dBm. During measurements over more than one hour, receiver performance remained constant without LO re-calibration. The wide IF bandwidth allows the LO to drift without leaving the desired range and improves tolerance of LO supply pushing. The 2GHz ring LO and buffers dissipate 20µW, about 10 times less than the LC oscillator in [4]. The mixer, IF amplifier, and envelope detector consume 8, 22, and 2µW respectively, leading to a total of 52µW from the 0.5V supply. The wake-up receiver prototype demonstrates that the use of high-Q RF filters enables architectures with drastically simplified frequency synthesis, resulting in substantial power savings. Higher Q resonators or multi-resonator filters can provide smaller RF bandwidth and further reduce susceptibility to interferers.

Acknowledgments:
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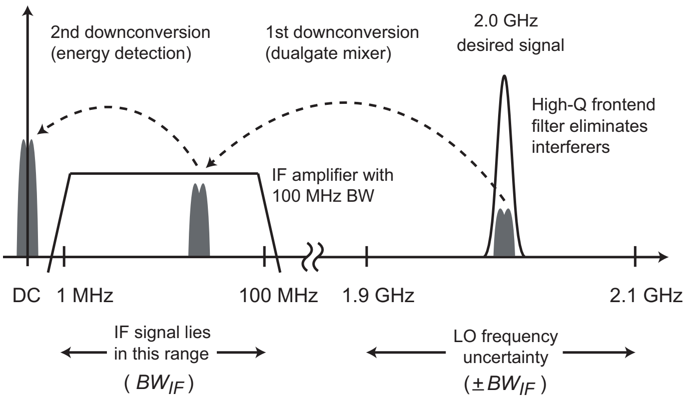

Figure 29.2.1: Method of operation and frequency plan.

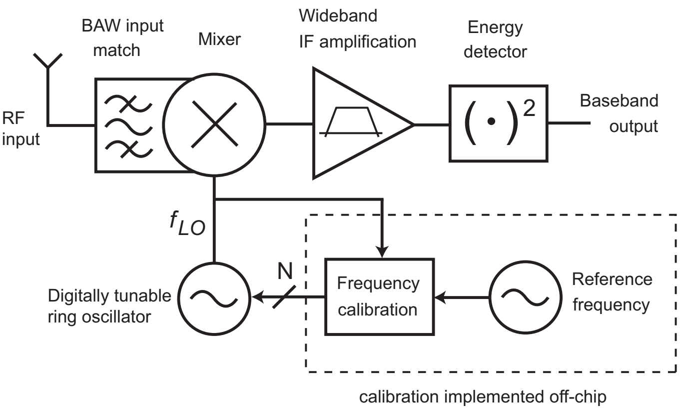

Figure 29.2.2: Receiver block diagram.

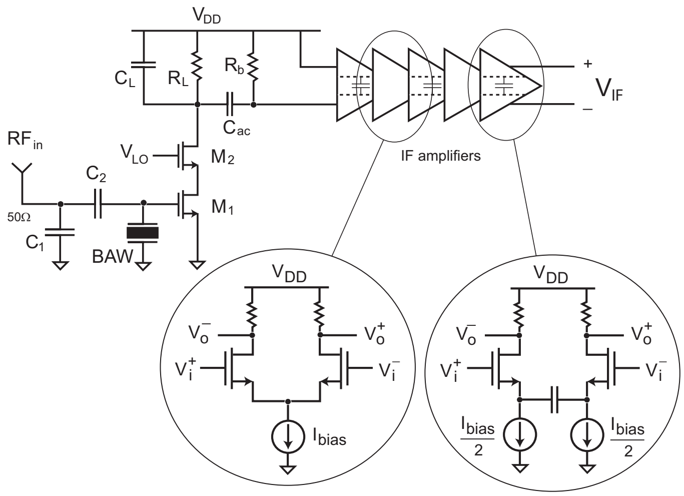

Figure 29.2.3: Circuit schematic of RF front-end and IF section.

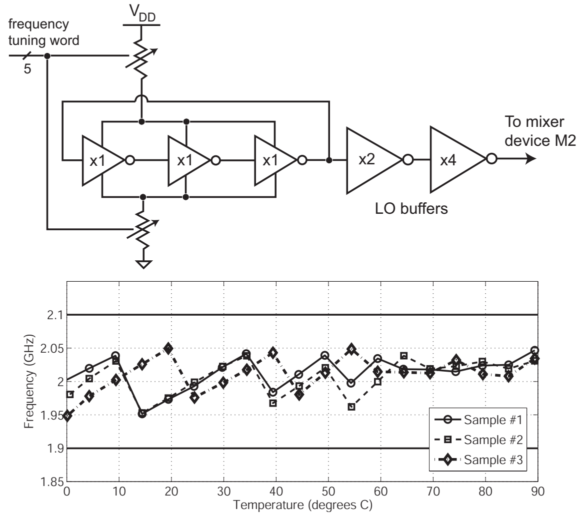

Figure 29.2.4: Ring oscillator schematic and frequency calibration across temperature. Calibration is triggered whenever the frequency exceeds a preset limit.

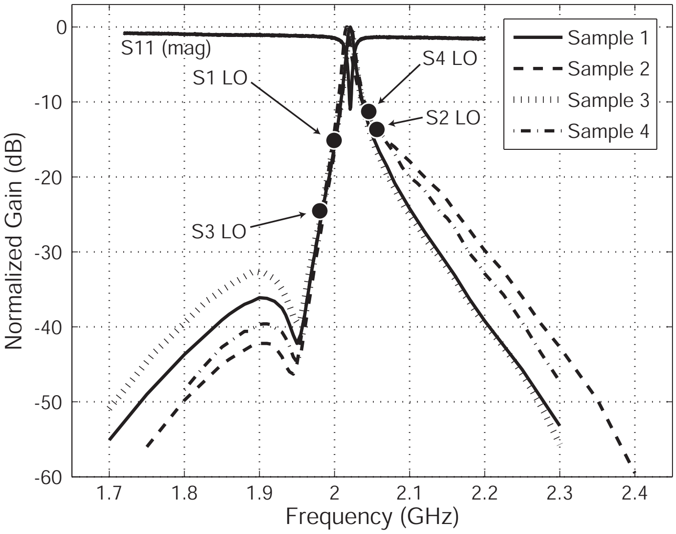

Figure 29.2.5: Normalized receiver gain and *S11* magnitude with annotated LO frequencies.

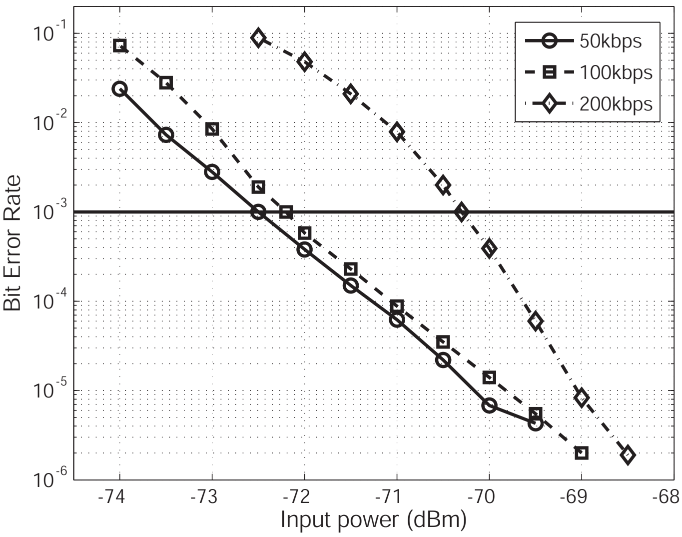

Figure 29.2.6: Measured BER for different data rates.

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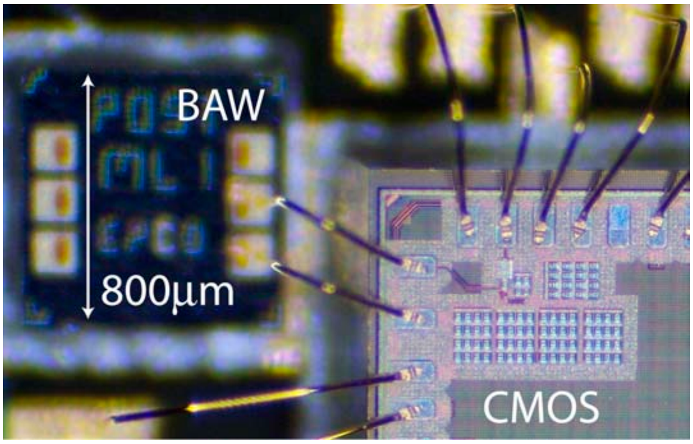

Figure 29.2.7: Die micrograph with BAW resonator directly bonded on the left side.

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