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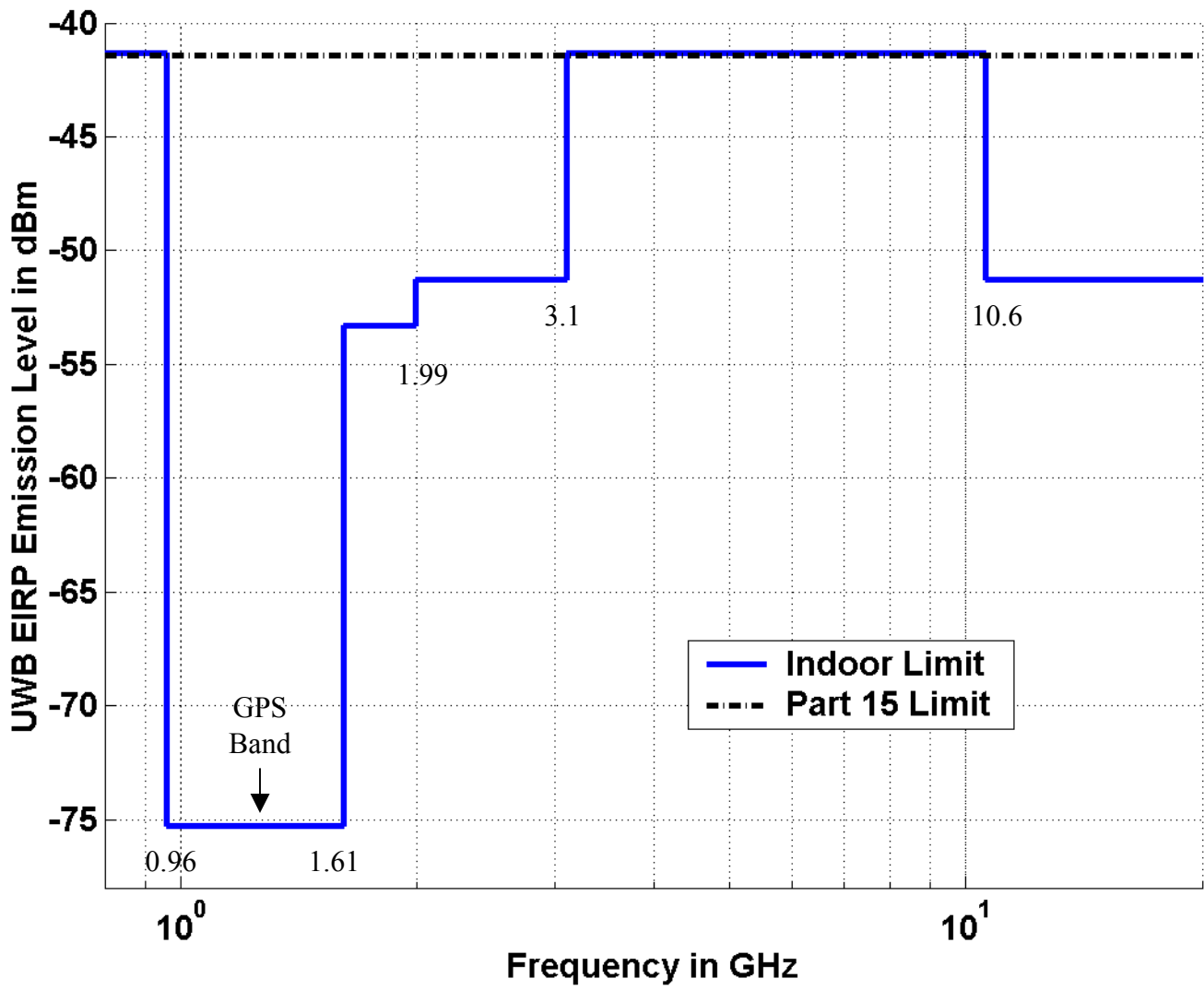
An Integrated, Low-Power, Ultra-Wideband Transceiver Architecture for Low-Rate Indoor Wireless Systems

Ian O'Donnell, Mike Chen, Stanley Wang,
Bob Brodersen

Berkeley Wireless Research Center
Univ. of California, Berkeley

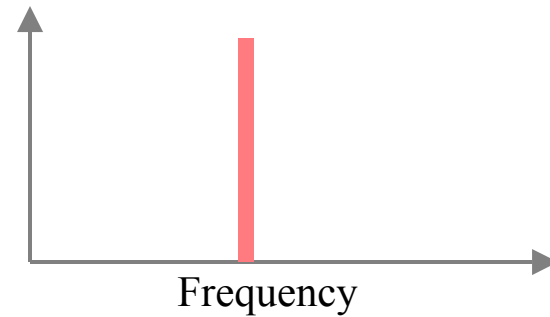
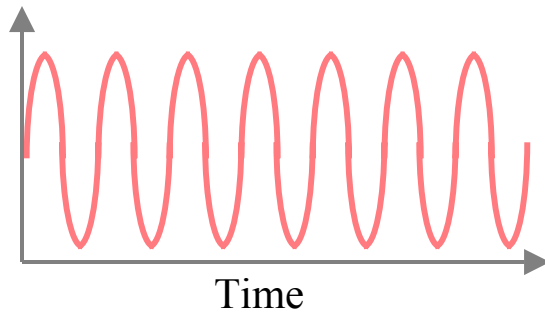


UWB Emission Limit for Indoor Systems [FCC]

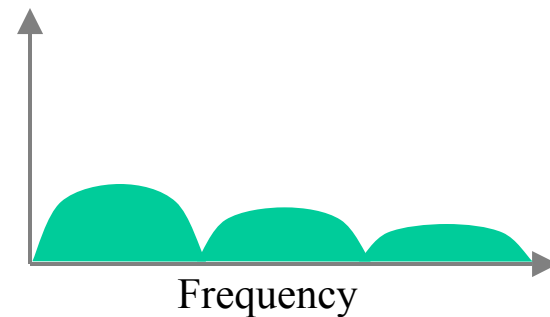
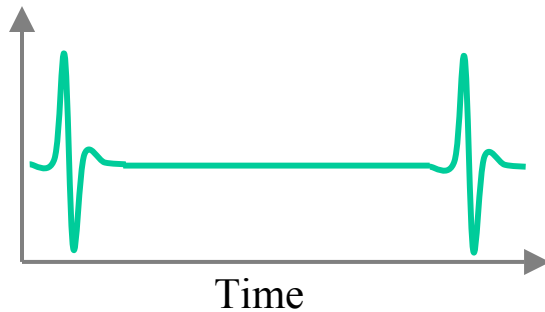


Signaling Approach

Sinusoidal, Narrowband



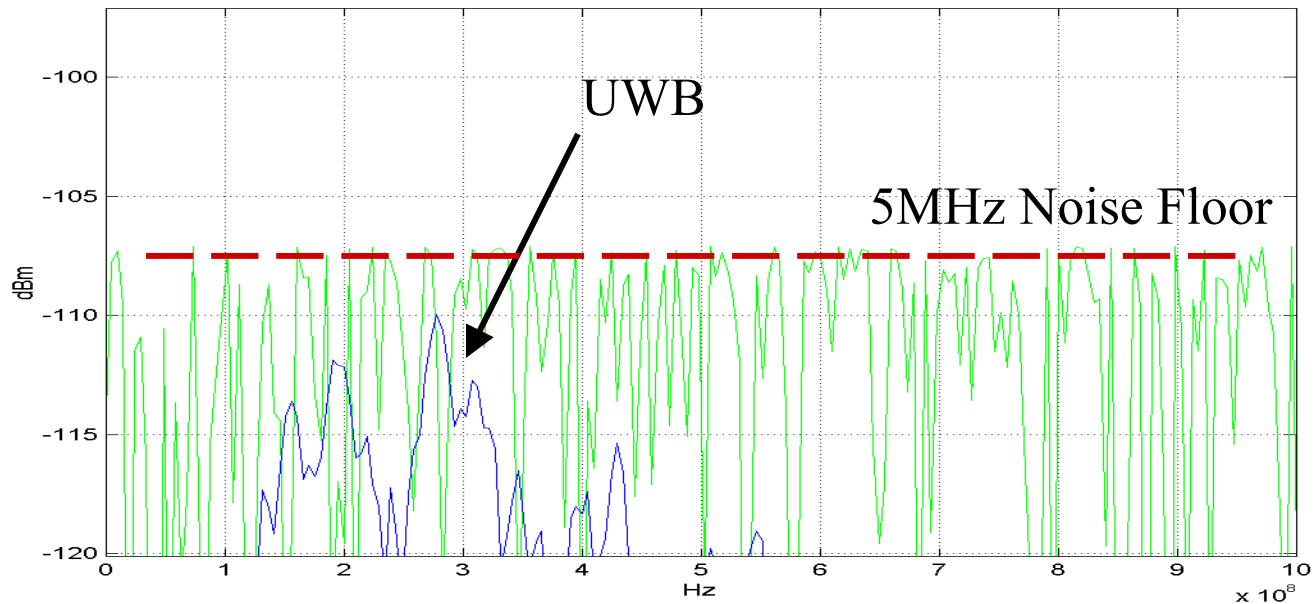
Impulse, Ultra-Wideband



Idea: “Imperceptible” UWB

“Polite” Co-existence with Licensed Operators:

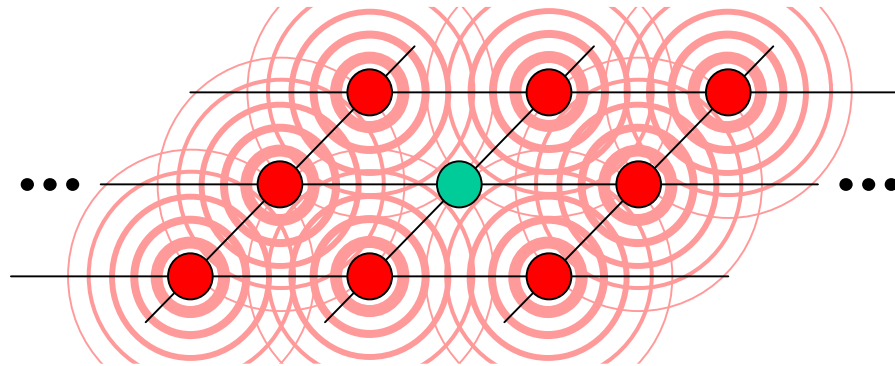
Aggregate Interference from UWB Transmissions is “Undetectable” (or Has Minimal Impact) to Narrowband Receivers, I.e. Power Spectral Density is at Narrowband Thermal Noise Floor or Below.



UWB Interference vs. Density

What is a “polite” Transmit Power?

- Infinite 2-D Grid of UWB Jammers:



- Assume Path Loss Model: $P_R = P_{1m}(1m/d)^n$
with $n=2.4$ [Cassoli, Win, Molisch, '02]

Aggregate Interference:

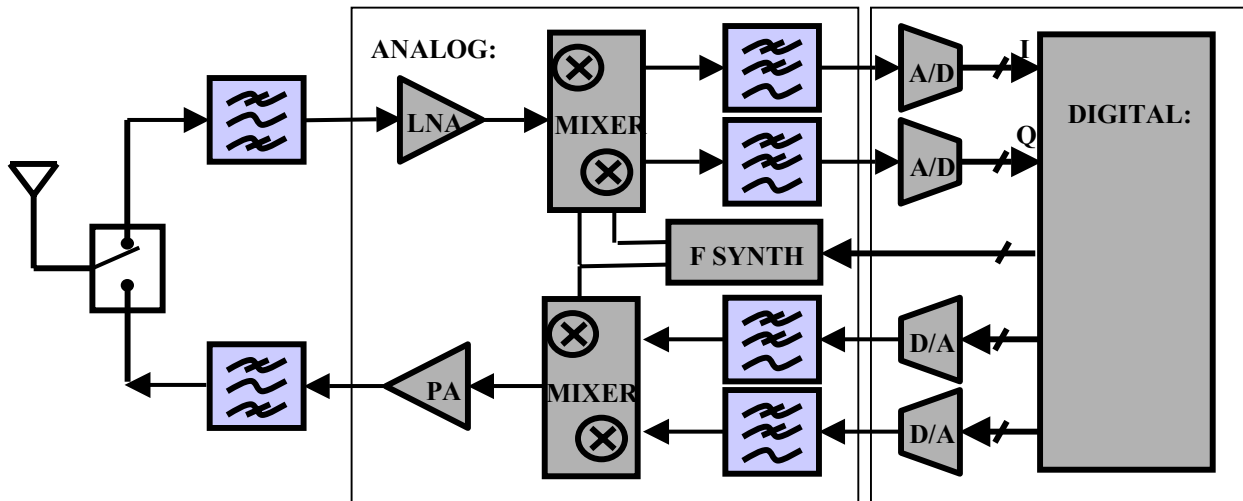
At 1m Grid Spacing, $P_R \sim 12.6P_{1m}$

At 3m Grid Spacing, $P_R \sim 0.9P_{1m}$

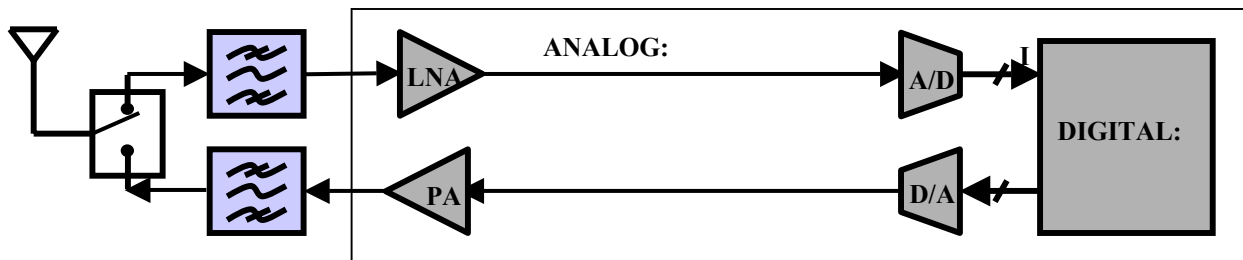
- Set P_R is Around Thermal Noise Floor

Towards a Digital Radio

Conventional Integrated, Narrowband Transceiver:

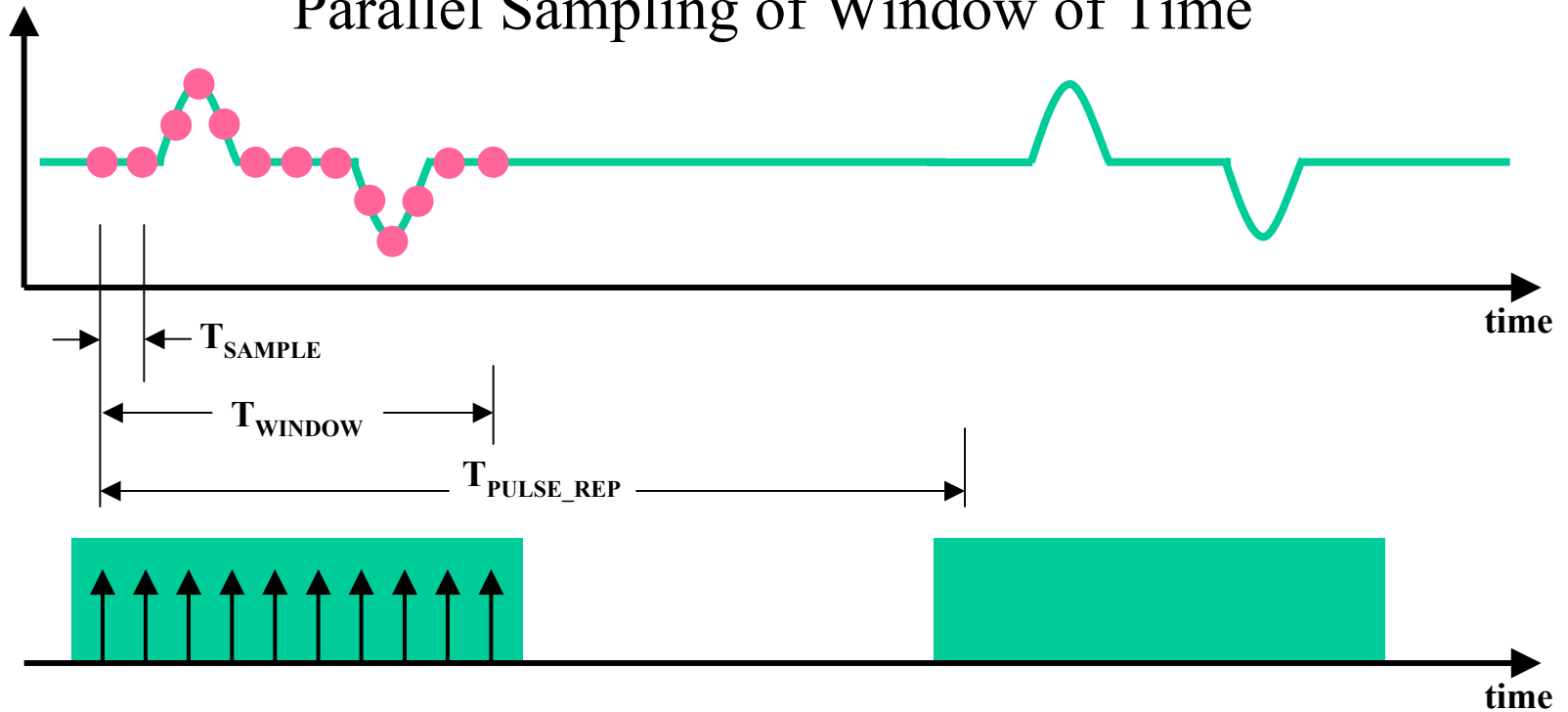


A “Mostly Digital” Radio:



Pulse Reception

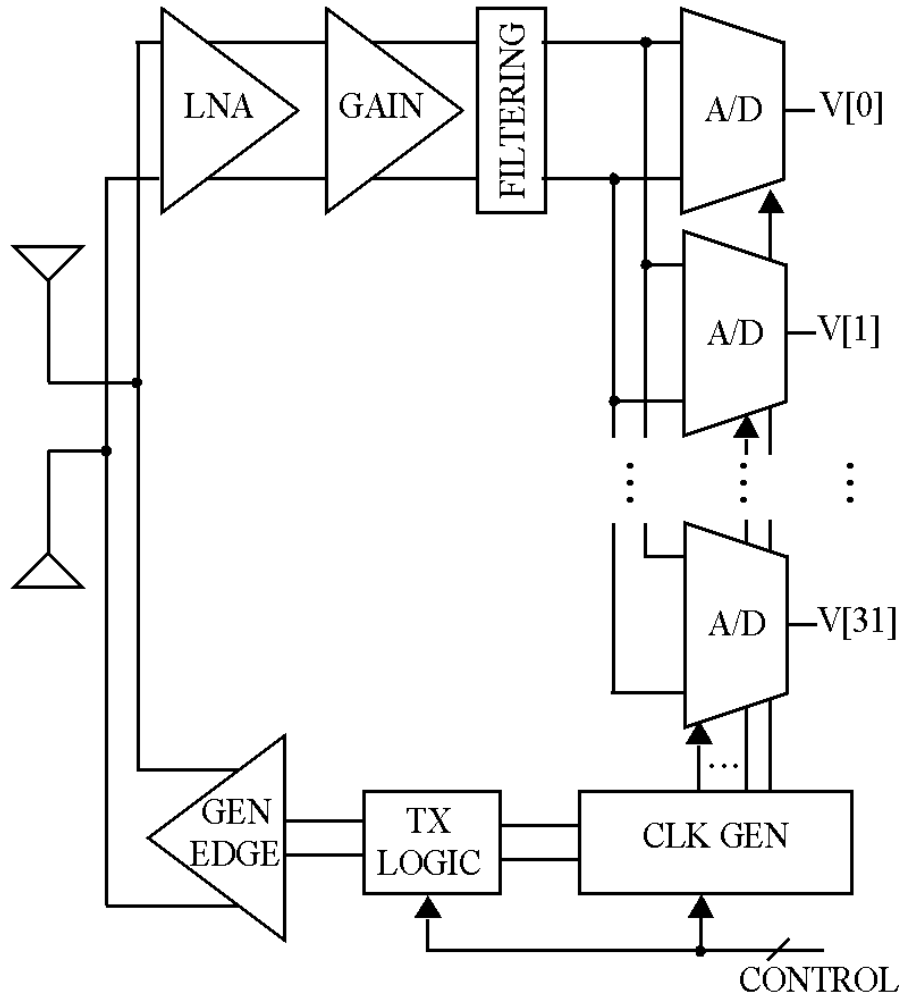
Parallel Sampling of Window of Time



Three Clocking Timescales:

T_{SAMPLE} (<ns) T_{WINDOW} (~10's ns) $T_{\text{PULSE_REP}}$ (~100's ns)

Architecture: Analog Frontend



Simple Architecture

Reception:

Gain

Filtering

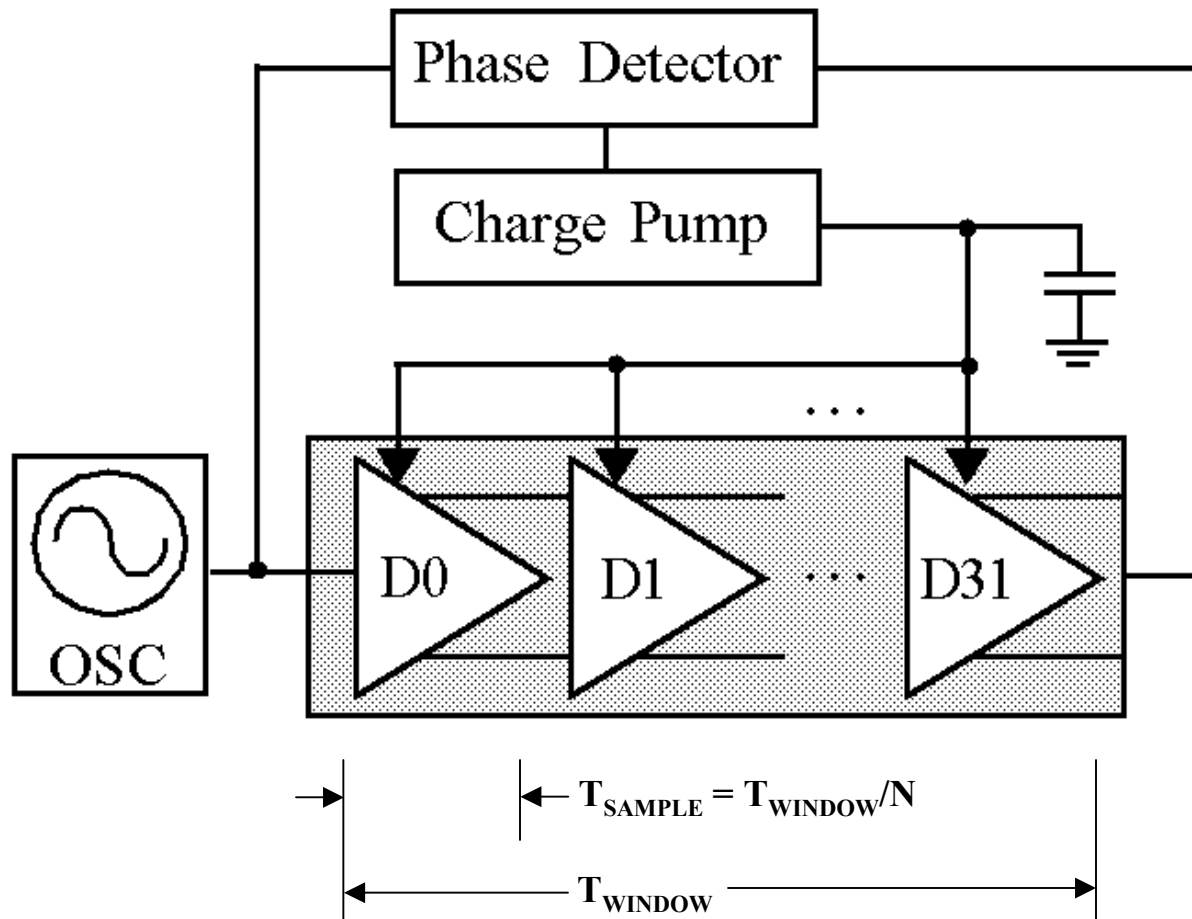
Sampling

Transmission:

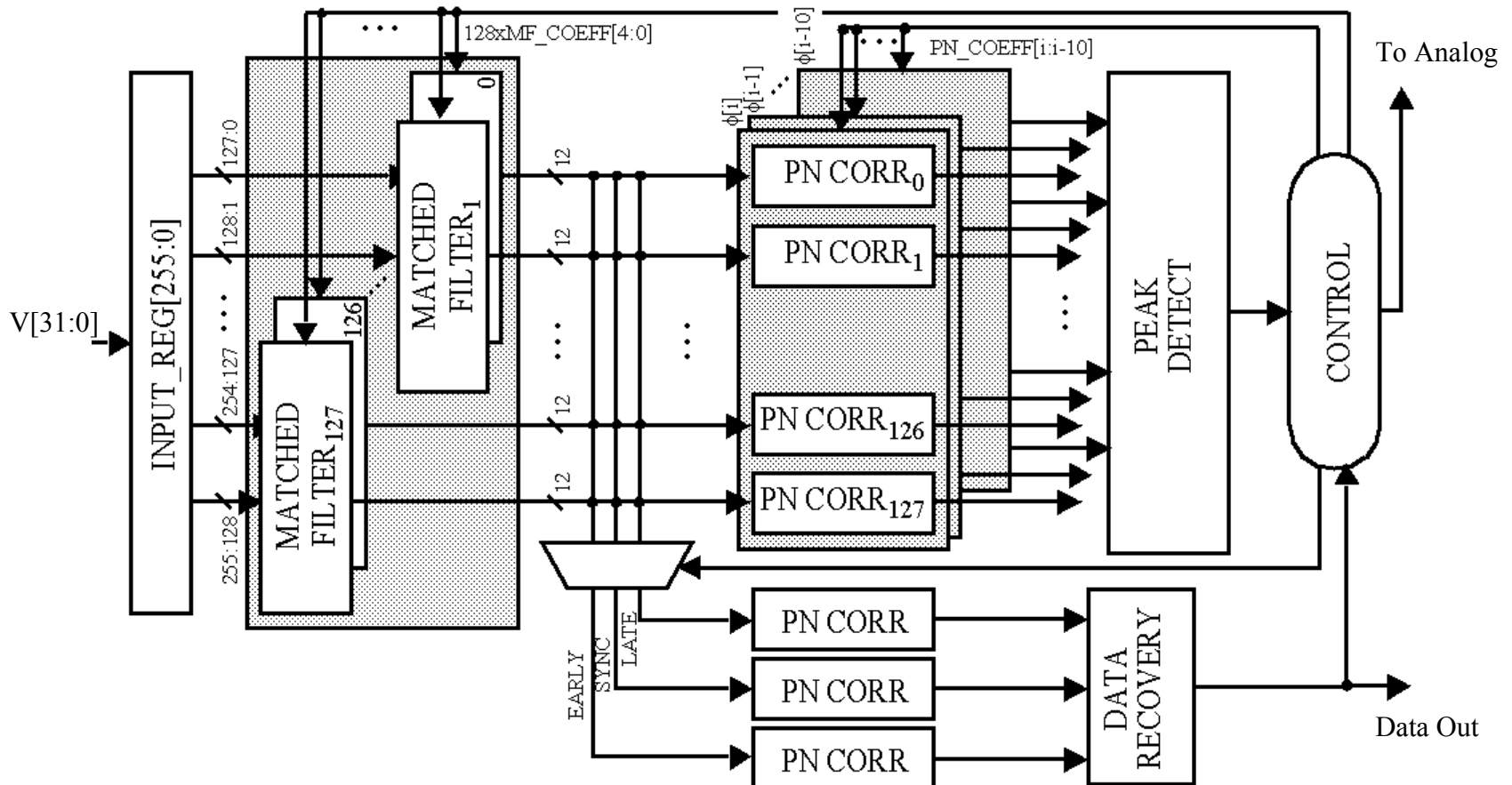
Digital Pulse

Clock Generation

Architecture: Clock Generation



Architecture: Digital Backend



Main Area Contributors: Matched Filter & Correlators

Circuit Design Constraints

Explore Implementation Issues for UWB Transceiver:

- A/D Bitwidth
- Matched Filter Coefficient Bitwidth
- Pulse Rate Considerations
- Gain Considerations
- Noise Figure
- Oscillator Accuracy Requirement
- Oscillator Phase Noise Requirement
- Digital Computation (Area)
- Acquisition Time vs. Area

System SNIR

Calculate SNIR of Matched Filter Output (per Pulse)

Include Effects of:

Received Pulse Shape

A/D Quantization

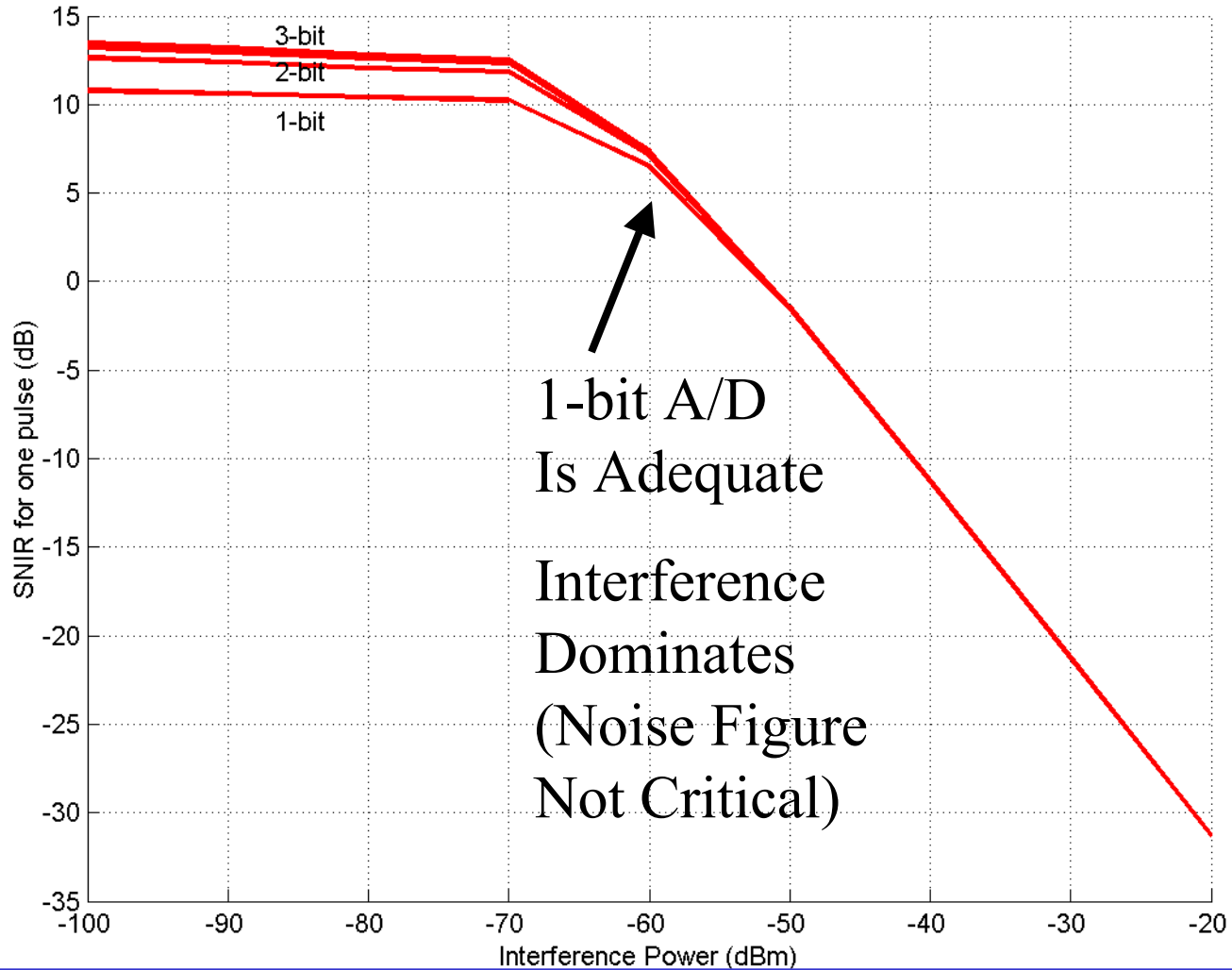
Noise Figure

Interference

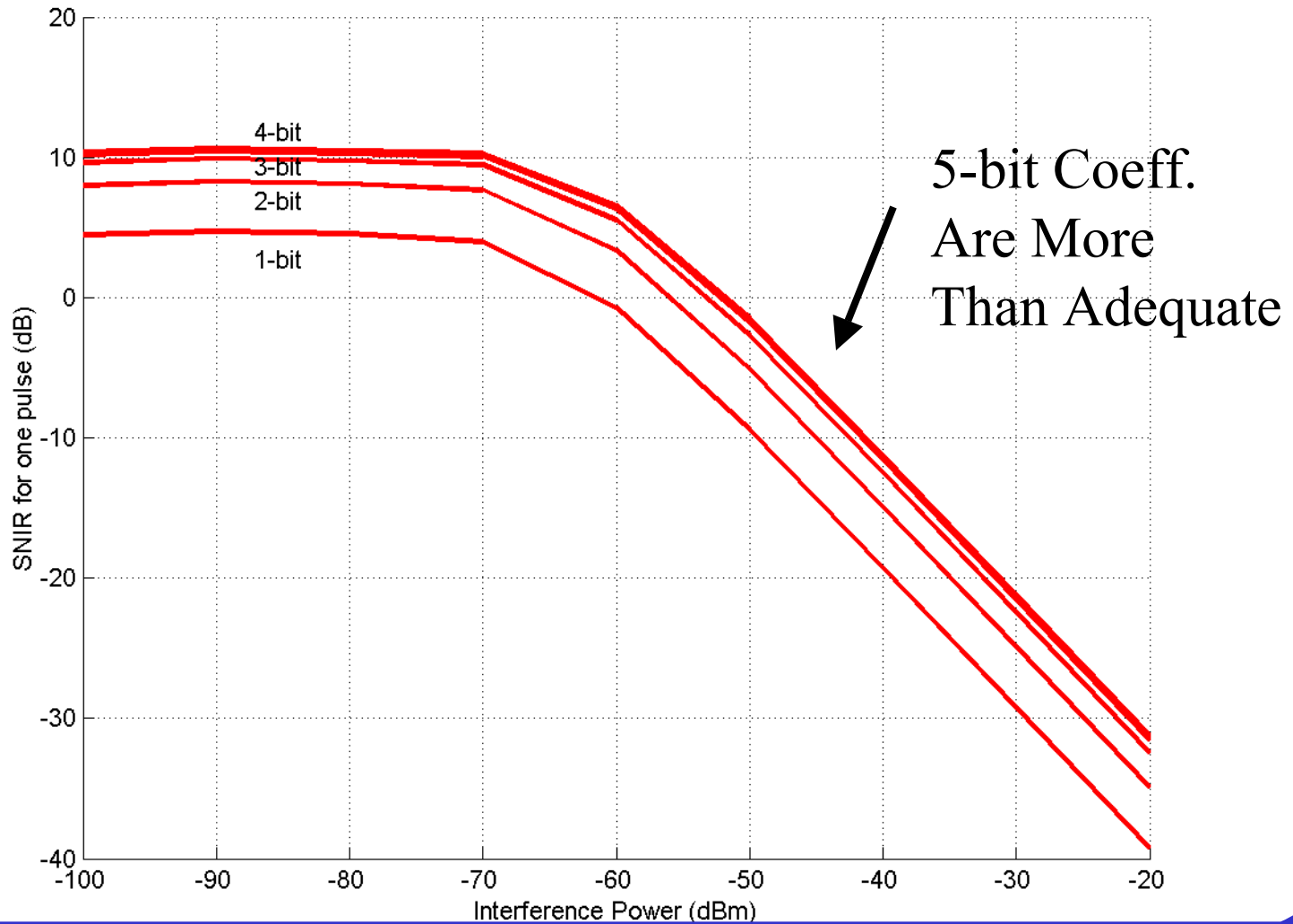
Matched Filter Coefficient Quantization

$$SNIR = \frac{P_S^2}{P_S(\sigma_{NX}^2 + \sigma_Y^2) + (S_{RII} S^t) + \sigma_Y^2 \left(K\sigma_{NX}^2 + \sum_{n=0}^{N-1} \frac{A_n^2}{2} \right)}$$

A/D Bitwidth



Matched Filter Bitwidth



Pulse Rate Considerations

Pulse Amplitude vs. Pulse Rate

Simple Example: Continuous Pulse Train

$A * p(t)$ with Fourier Transform $A * P(\omega)$

$$F(\omega) = 2\pi f_{REP} A P(\omega) \sum_k \delta(\omega - 2\pi f_{REP} k)$$

For Constant Power Spectral Density
(FCC Requirement)

$$|F(\omega)|^2 = \text{Constant}$$

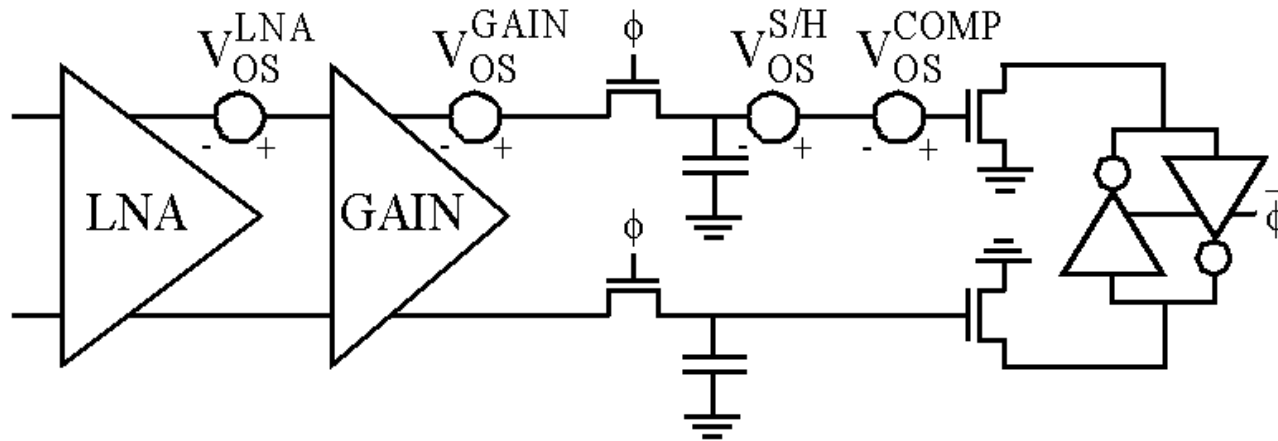
$$A * f_{REP} = \text{Constant}$$

Can Directly Trade-off Amplitude for Rate

Pulse Rate vs. Throughput



Gain Considerations



For 1-bit A/D:

Minimum Gain Set by Offset Seen at Comparator.

For 10mV Offset, Minimum Detectable Input:

Need 80dB of Gain

Primary LNA Constraint: Impedance Matching

Oscillator Accuracy

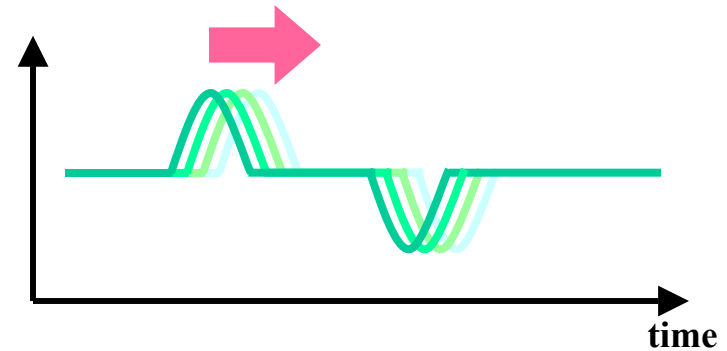
Frequency Mismatch Causes Drift

Slide ΔT over 1 Symbol:

$$\frac{\Delta f}{f_c} \approx \frac{1}{2} f_{symbol} \Delta T$$

$$f = (f_{TX} + f_{RX})/2$$

$$\Delta f = (f_{TX} - f_{RX})$$



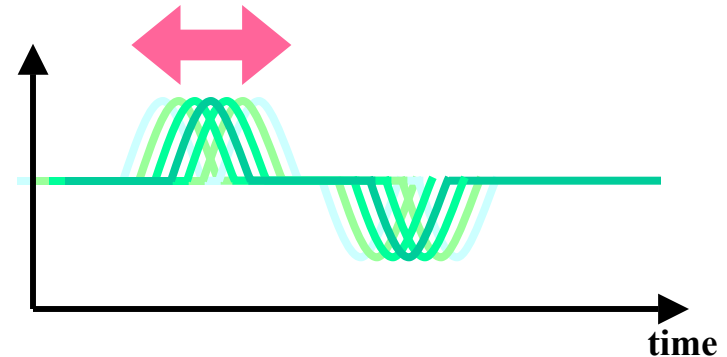
$$\Delta T = 100\text{ps}$$
$$f_{symbol} = 20\text{kHz}$$

$$\Delta f/f = 1.0 \text{ PPM}$$

Oscillator Jitter

Map Jitter to Phase Noise Requirement:
For Phase Noise Proportional to $1/f^2$

$$\mathcal{L}(\Delta f) \approx 2\pi^2 \sigma_T^2 \left(\frac{f_c}{\Delta f}\right)^2 \frac{1}{T_{symbol}}$$



$\sigma_{\Delta T} = 100\text{ps}$ $T_{\text{SYMBOL}} = 50\mu\text{s} (20\text{kHz})$

$$L\{100\text{kHz}/1\text{MHz}\} = -84\text{dBc}/\text{Hz}$$

Digital Backend

Large Amount of Computation:

Fully Parallel Search >> 1cm² Die Size

Searching 64ns and 11 Phases in Parallel:

128 Programmable Matched Filters

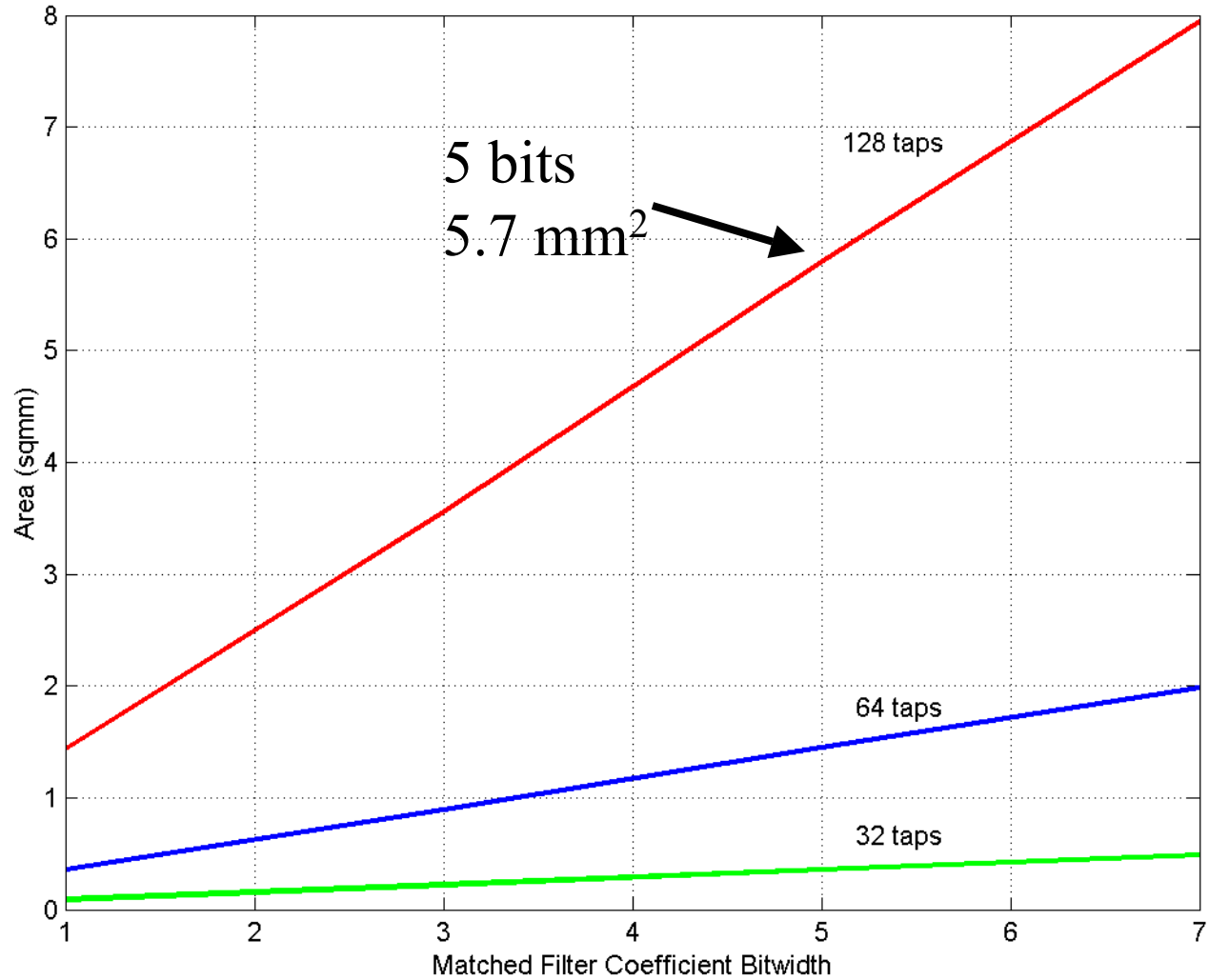
(128 5-bit Taps Each)

1,411 Spreading Sequence Correlators

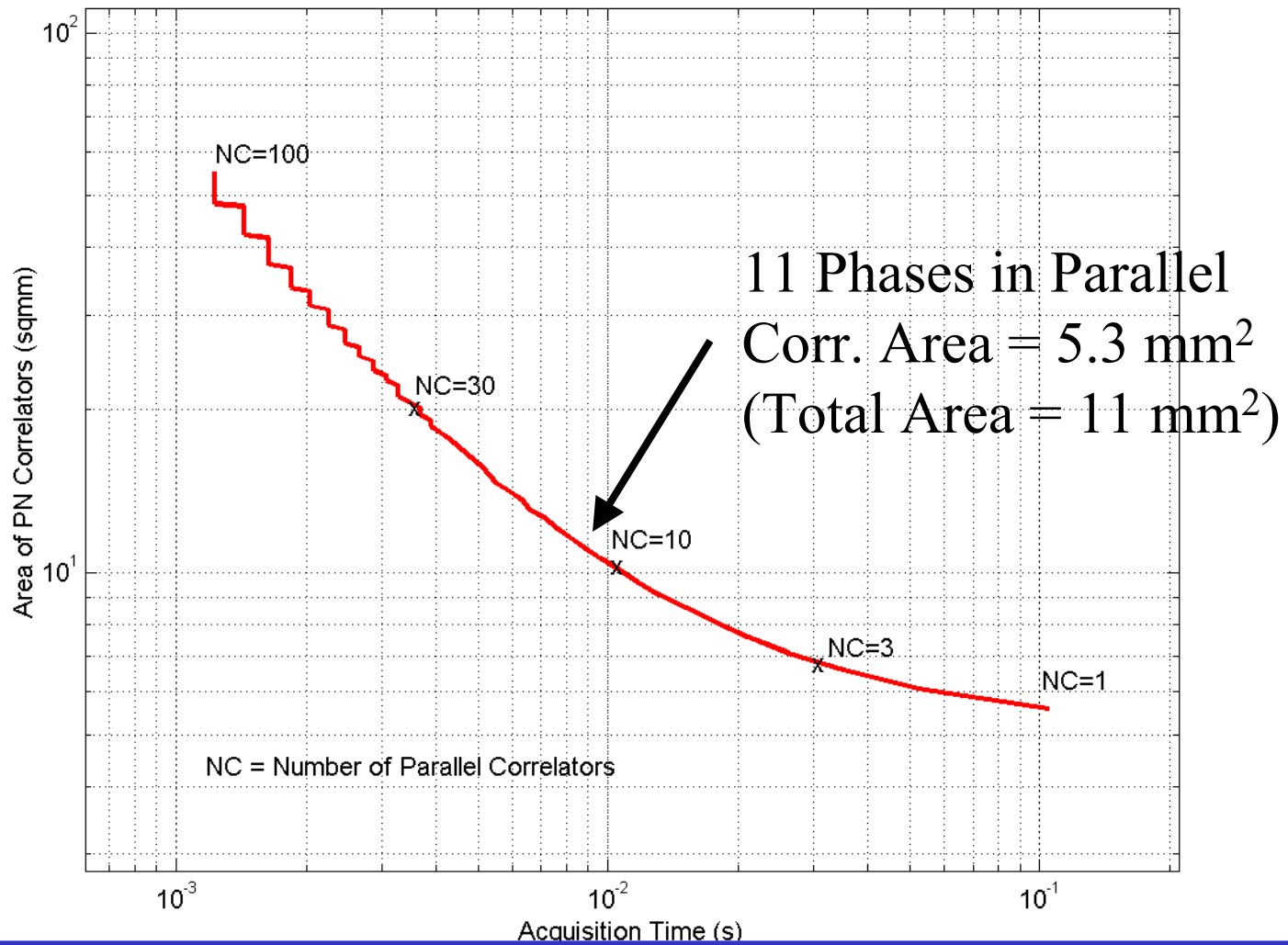
(11 Phases in Parallel)

Area vs. Acquisition Trade-off

Matched Filter Area



Correlator Area vs. Acquisition



Conclusion

- UWB Low Power Transceiver Architecture Presented
- Circuit Design Requirements Discussed
- “Imperceptible” Operation Explored
- Data Rates $\sim 100\text{kb/s}$ to 1Mbps Possible
- Suitable for Indoor Wireless Sensor Network
- Plan to Send Design Out for Fabrication by Dec. 2002.