

Research Proposal

Problem:

How to Design and Implement an UWB Transceiver for a Highly-Integrated, Low-Power, Indoor, Network Radio Application?

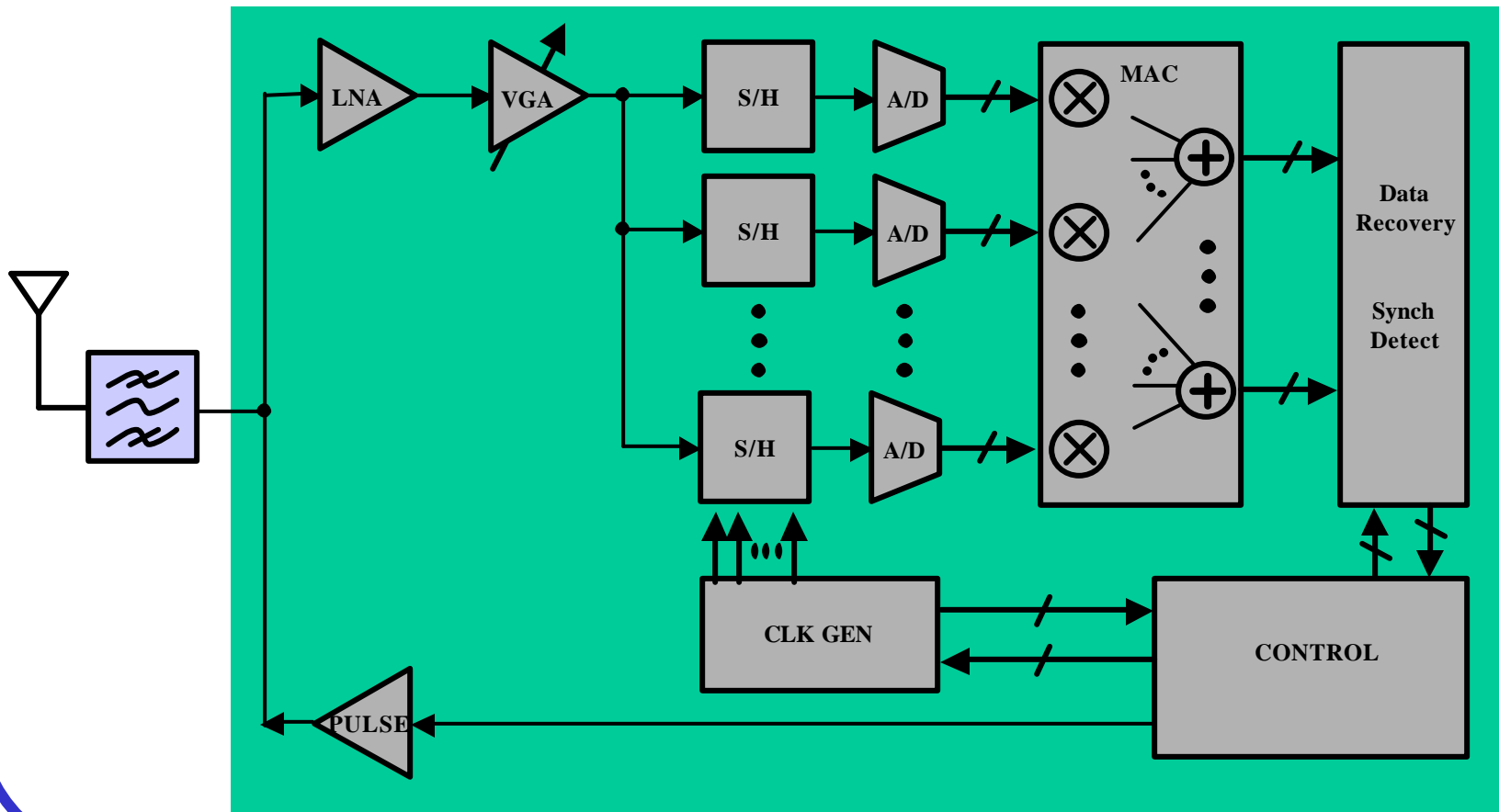
Solution:

Establish a Framework to Evaluate Trade-offs Between System Performance and Implementation Issues by:

- Investigating Nature of UWB Communications
- Modeling and Exploring System Architecture Options
- Identifying Low Power Design Techniques for CMOS Circuits

Proposed System Architecture

Based on Digital Sampling/Acquisition Oscilloscopes



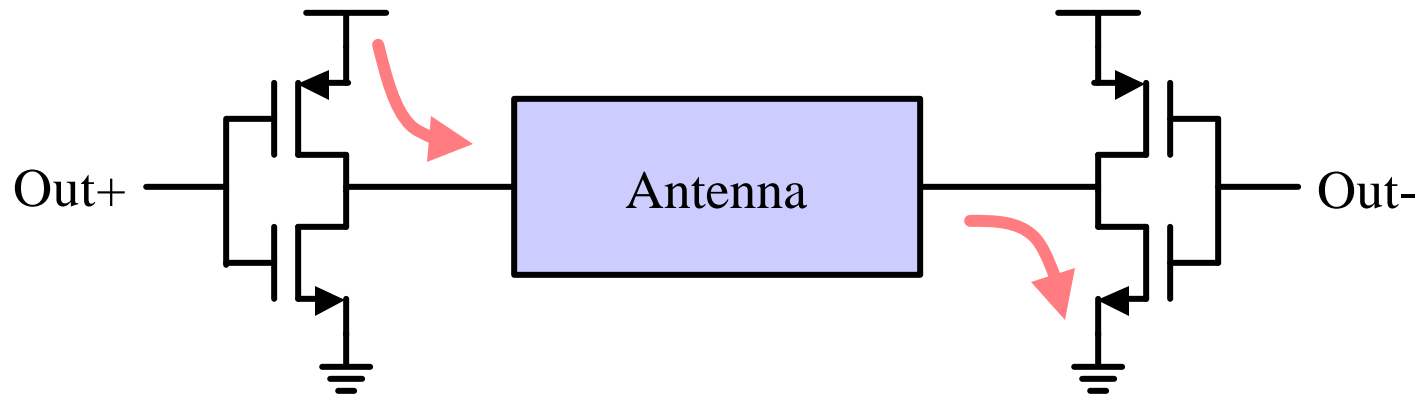
Power Budget

Block	Duty Cycle	Power (Always On)	Power (Per Period)
Low Noise Amp	T_{win}/T_{rep}	600 μ W	60 μ W
Variable Gain Amp	T_{win}/T_{rep}	1.8mW	180 μ W
Sample/Hold	100%	1 μ W	1 μ W
A/D Converter	100%	100 μ W	100 μ W
Oscillator	100%	100 μ W	100 μ W
Sampling Clock Gen	100%	400 μ W	400 μ W
TX: Pulse Generation	2ns/ T_{rep}	10mW	100 μ W
Digital Logic	100%	60 μ W	60 μ W
Total Power Per Period:			= 1001 μ W

Pulse Generation

Desire low voltage (and hence easily integrated) approach:

Use H-Bridge Configuration to Switch +/- Current



Issues:

Radiation Efficiency

Peak Current

Antenna DC Bias

E.g. $I_{\text{peak}}=8\text{mA}$ for $2\text{ns}/5\text{MHz}$ -- $P=100\text{mW}$ ($V_{\text{dd}}=1.2\text{V}$)

Clock Generation

Oscillator Requirements: (5MHz)

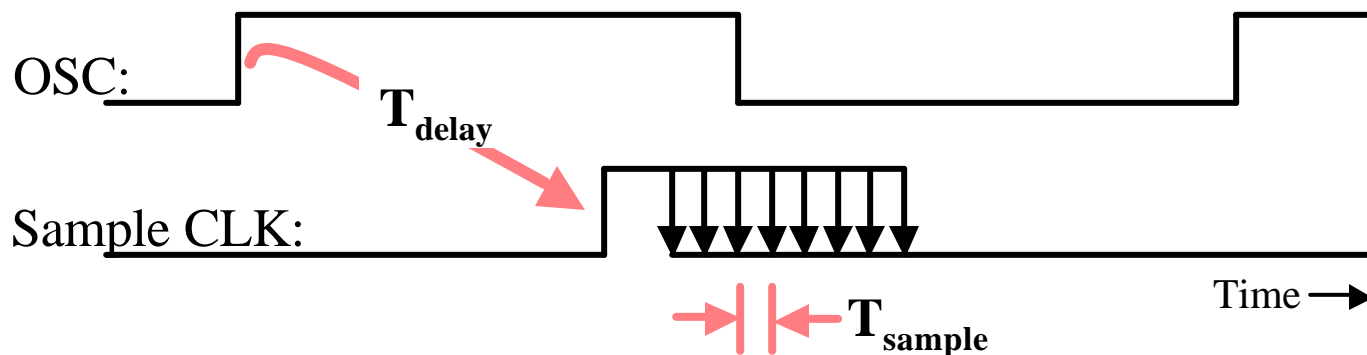
Drift (100 Chips/0.5ns Bin) → Crystal Accuracy (+/- 20ppm)

Jitter (0.1ns) → Phase Noise (-100 dBc/Hz @ 100kHz)

Clock Generation:

Precise Delay: T_{delay}

Sampling Clock Spacing: T_{sample}



Sample/Hold

Would Like To Use Passive Sampling

- Tracking Bandwidth = 1GHz
- Sources of Error:

Clock Feed-through
Channel Charge
Thermal Noise

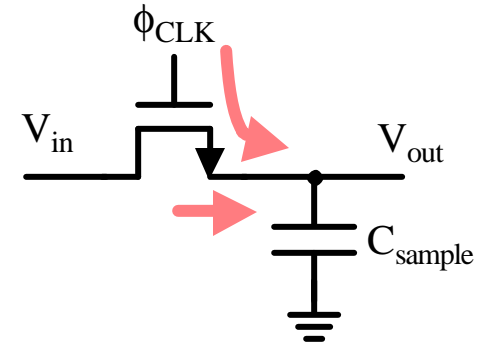
Constrain C_{sample} Relative To Switch Size:

$C_{\text{sample}} = 70\text{fF}$ for $< 1/2$ LSB Error

Then,

$R_{\text{ds}} = 2\text{k}\Omega$ for 1GHz Tracking

Can Use a $1\mu\text{m}/0.3\mu\text{m}$ Switch (1.2V, 0.15 μm Process)



A/D Conversion

Primary Issue: Low Power, Low Area

Rate (5MHz) and Width (4bits) Are Not Aggressive

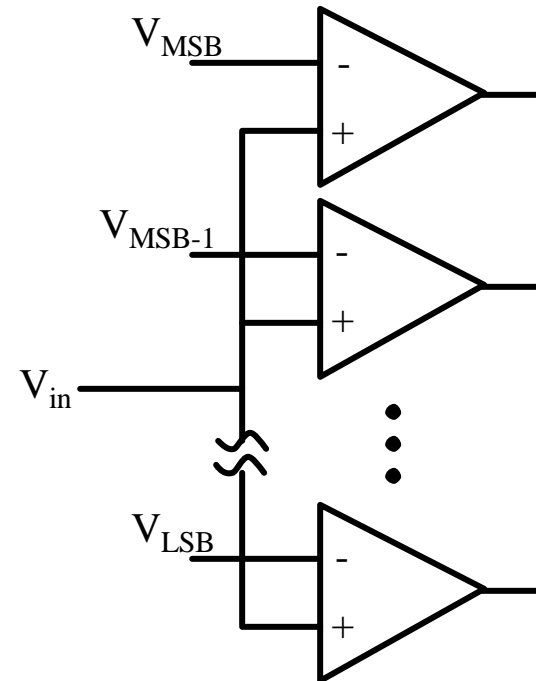
Low-Power Approach:

- Use Dynamic Comparators
- Integrate Into Sample/Hold
- No Interstage Amplifiers
- No Static Currents

Architecture: Flash

Issues: Area, V_{ref} Generation,
Comparator Offset

$$\text{Power Est.} = N * C_{\text{sample}} * V_{\text{dd}}^2 * f_{\text{clk}}$$



Digital Backend

Order of Magnitude Power/Area Estimates

Multiply-Accumulate (12x 4b x 4b MAC's)	0.252mm ² (13,967 INV)	150μW
Data Recovery (RX) (~ 4-bit MAC)	0.004mm ² (222 INV)	0.6μW
Synch Detector (24 4-bit Thresh+Logic)	0.049mm ² (2722 INV)	5μW
PN Generator (32-bit Shift Reg/XOR)	0.002mm ² (112 INV)	0.2μW
Data Spreading (TX)	<0.001mm ² (<56 INV)	<0.1μW
Total	0.308mm ² (16,722 INV)	156μW

STMicro CMOS Lib 0.25μm: 2V, 5MHz, $p_{\text{activity}}=1/2$